NCP156

LDO Regulator - Dual, Camera Modules, Low Iq, Very Low Dropout, Ultra Low Noise

500 mA, 250 mA

The NCP156 is Dual Output Linear Voltage Regulator optimized for camera module application. The device offers unique combination of High Current Low Voltage Bias Rail Topology for supplying digital block and very precise second output for powering analog sensor block. This combination allows achieving the best performance and power efficiency.

Features

- High Current Bias Rail Topology for OUT1
- High PSRR, Ultra Low Noise LDO for OUT2
- Output voltage range: OUT1 – 0.8 V to 1.8 V (Factory trimmed) OUT2 – 1.8 V to 3.6 V
- Low I_Q of typ. 90 μA
- Slow V_{OUT} Slew Rate for Camera Modules (Optional) typ. ≤30 mV/ms
- Ultra−Low Dropout: OUT1 typ. 70 mV @ 1.2 V/500 mA OUT2 typ. 95 mV @ 2.8 V/250 mA
- ±1% Typical Accuracy
- High PSRR: OUT1 typ. 70 dB at 1 kHz OUT2 typ. 92 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Stable with a Small Ceramic Capacitor
- Available WLCSP−6 1.2x0.8 mm Package
- Active Output Discharge for Fast Output Turn−Off
- These are Pb−free Devices

Typical Applications

- Camera Modules
- Smartphones, Tablets

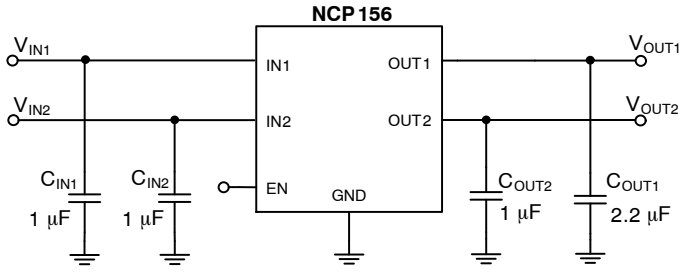

Figure 1. Typical Application Schematic

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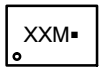
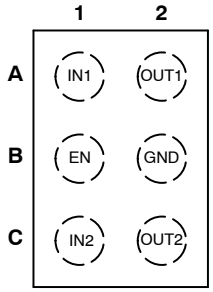
WLCSP6, 1.2x0.8
CASE 567MV

MARKING DIAGRAM



XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

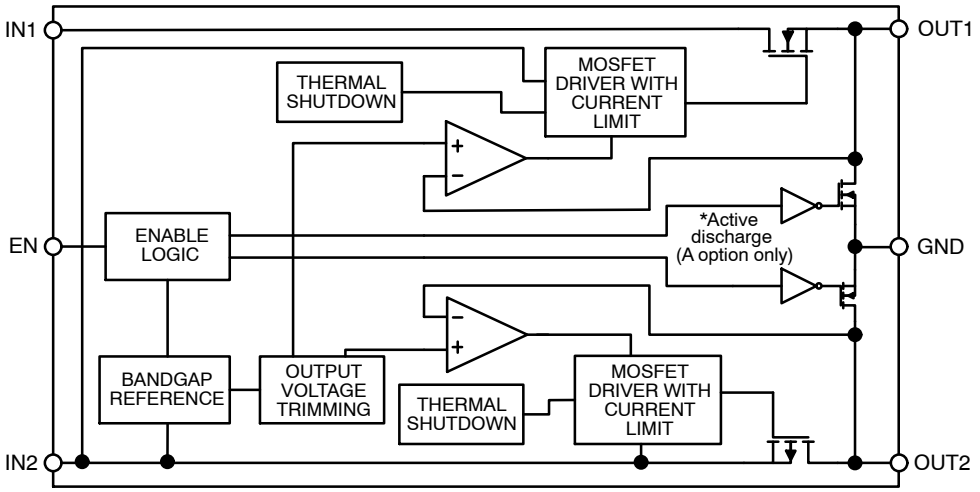


Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
A1	IN1	Output 1 – Power Supply pin
A2	OUT1	Regulated Output 1 Voltage pin
B1	EN	Applying V_{EN} < 0.4 V disables the regulator; Pulling V_{EN} > 0.9 V enables both voltage outputs.
B2	GND	Common ground connection
C1	IN2	Output 2 – Power Supply pin, Output 1 – Control Supply pin
C2	OUT2	Regulated Output 2 Voltage pin

Table 2. THERMAL CHARACTERISTICS (Note 1)

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP6 1.2x0.8mm, Thermal Resistance, Junction–to–Air	θ_{JA}	90	°C/W

1. Single component mounted on 1 oz, FR4 PCB with 645mm2 Cu area

Table 3. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage 1 (Note 2)	V_{IN1}	–0.3 to 6	V
Input Voltage 2 (Note 2)	V_{IN2}	–0.3 to 6	V
Output Voltage 1	V_{OUT1}	–0.3 to V_{IN1} + 0.3	V
Output Voltage 2	V_{OUT2}	–0.3 to V_{IN2} + 0.3	V
Enable Input	V_{EN}	–0.3 to 6	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	–55 to 125	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 3)	ESD_{MM}	200	V
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC–Q100–002 (EIA/JESD22–A114)
   ESD Machine Model tested per AEC–Q100–003 (EIA/JESD22–A115)
   ESD Charged Device Model tested per EIA/JESD22–C101, Field Induced Charge Model
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 4. ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; $V_{IN1} = V_{OUT1(NOM)} + 0.3$ V, $V_{IN2} = 2.7$ V or ($V_{OUT1} + 1.6$ V) or $V_{OUT2(NOM)} + 0.3$ V whichever is greater, $I_{OUT1} = I_{OUT2} = 1$ mA, $V_{EN} = 1$ V, unless otherwise noted. $C_{IN1} = C_{IN2} = 1$ μF, $C_{OUT1} = 2.2$ μF, $C_{OUT2} = 1$ μF. Typical values are at $T_J = +25°C$. Min/Max values are for $-40°C \le T_J \le 125°C$ unless otherwise noted.

Parameter	Test Conditions			Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range				V_{IN1}	V_{OUT1} + V_{DO}		5.5	V
				V_{IN2}	V_{IN2} = (V_{OUT1}+1.5) ≥ 2.4 or $V_{OUT2(NOM)}$+V_{DO}, whichever is greater		5.5	
Output Voltage Accuracy	$T_J = 25°C$			V_{OUT1}		±1		%
				V_{OUT2}				
Undervoltage Lock−out	V_{IN2} Rising			UVLO		1.5		V
	Hysteresis					0.2		
Output Voltage Accuracy	$V_{OUT1(NOM)} + 0.3$ V ≤ V_{IN1} ≤ $V_{OUT1(NOM)} + 1.0$ V, $V_{OUT2} = 2.7$ V or ($V_{OUT1(NOM)}$) + 1.6 V), whichever is greater, 1 mA < I_{OUT1} < 500 mA		V_{OUT1} < 1.2 V	V_{OUT1}	−18		+18	mV
			V_{OUT1} ≥ 1.2 V		−1.5		+1.5	%
	V_{IN2} = ($V_{OUT2(NOM)}$ + 0.3 V) to 5.5 V, 0 mA ≤ I_{OUT2} ≤ 250 mA			V_{OUT2}	−2		+2	%
Line Regulation	V_{OUT1}	$V_{OUT1(NOM)} + 0.3$ V ≤ V_{IN1} ≤ 5.5 V		$Line_{REG}$		0.01		%/V
	V_{OUT2}	$V_{OUT2(NOM)} + 0.3$ V ≤ V_{IN2} ≤ 5.5 V				0.02		
	V_{IN2} to V_{OUT1}	(2.7 V or ($V_{OUT1(NOM)}$ + 1.6 V), whichever is greater) < V_{IN2} < 5.5 V				0.01		
Load Regulation	OUT1	I_{OUT1} = 1 mA to 500 mA		$Load_{REG}$		5		mV
	OUT2	I_{OUT2} = 1 mA to 250 mA				1		
Dropout Voltage (Note 5)	OUT1	I_{OUT1} = 500 mA		V_{DO}		70	150	mV
	OUT2	I_{OUT2} = 250 mA	$V_{OUT2(NOM)}$ = 2.8 V			95	160	
V_{IN2} to V_{OUT1} Dropout Voltage	I_{OUT1} = 500 mA, $V_{IN1} = V_{IN2}$ (Notes 5, 6)			$V_{DO(IN2)}$		1.1	1.5	V
Output Current Limit	OUT1	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	550	850		mA
	OUT2				300	550		
Quiescent Current IN1	I_{OUT1} = 0 mA			I_{Q1}		10	20	μA
Quiescent Current IN2	I_{OUT2} = 0 mA			I_{Q2}		80	130	
Disable Current	V_{IN1} Pin	$V_{EN1} \le 0.4$ V		$I_{IN1(DIS)}$		0.05	1	μA
	V_{IN2} Pin			$I_{IN2(DIS)}$		0.1	1	
EN Pin Threshold Voltage	EN Input Voltage “H”			$V_{EN(H)}$	0.9			V
	EN Input Voltage “L”			$V_{EN(L)}$			0.4	
EN Pull Down Current	V_{EN} = 5.5 V			I_{EN}		0.3	2	μA
Turn−On Delay	OUT1	From assertion of V_{EN} to raising V_{OUT}		t_{DELAY}		200		μs
	OUT2					130		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
6. For output 1 voltages below 0.9 V, V_{IN2} to V_{OUT1} dropout voltage does not apply due to a minimum V_{IN2} operating voltage of 2.4 V.
7. Refer to Table 6 for output slew rate configuration.

Table 4. ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; $V_{IN1} = V_{OUT1(NOM)} +0.3$ V, $V_{IN2} = 2.7$ V or ($V_{OUT1} + 1.6$ V) or $V_{OUT2(NOM)} + 0.3$ V whichever is greater, $I_{OUT1} = I_{OUT2} = 1$ mA, $V_{EN} = 1$ V, unless otherwise noted. $C_{IN1} = C_{IN2} = 1$ μF, $C_{OUT1} = 2.2$ μF, $C_{OUT2} = 1$ μF. Typical values are at $T_J = +25°C$. Min/Max values are for $-40°C \le T_J \le 125°C$ unless otherwise noted.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
V_{OUT} Slew Rate (Note 7)	Normal		V_{OUT1}		100		mV/μs
			V_{OUT2}		200		
	Slow		V_{OUT1}		15		
			V_{OUT2}		30		
Power Supply Rejection Ratio	V_{IN1} to V_{OUT1}, f = 1 kHz, I_{OUT1} = 150 mA, $V_{IN1} \ge V_{OUT}$ +0.5 V		PSRR(V_{IN1})		70		dB
	V_{IN2} to V_{OUT2}, f = 1 kHz, I_{OUT2} = 10 mA, $V_{IN2} \ge V_{OUT}$ +0.5 V		PSRR(V_{IN2})		92		
	V_{IN2} to V_{OUT1}, f = 1 kHz, I_{OUT1} = 150 mA, $V_{IN1} \ge V_{OUT1}$ +0.5 V		PSRR(IN2 to OUT1)		80		
Output Noise Voltage	OUT1	$V_{IN} = V_{OUT}$ +0.5 V, f = 10 Hz to 100 kHz	V_N		40		μVRMS
	OUT2				8.5		
Thermal Shutdown Threshold	Temperature increasing		T_{SDL}		160		°C
	Temperature decreasing		T_{SDH}		140		
Output Discharge Pull−Down	$V_{EN} \le 0.4$ V (only if Active Discharge feature enabled)		R_{DISCH}		150		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
6. For output 1 voltages below 0.9 V, V_{IN2} to V_{OUT1} dropout voltage does not apply due to a minimum V_{IN2} operating voltage of 2.4 V.
7. Refer to Table 6 for output slew rate configuration.

TYPICAL CHARACTERISTICS

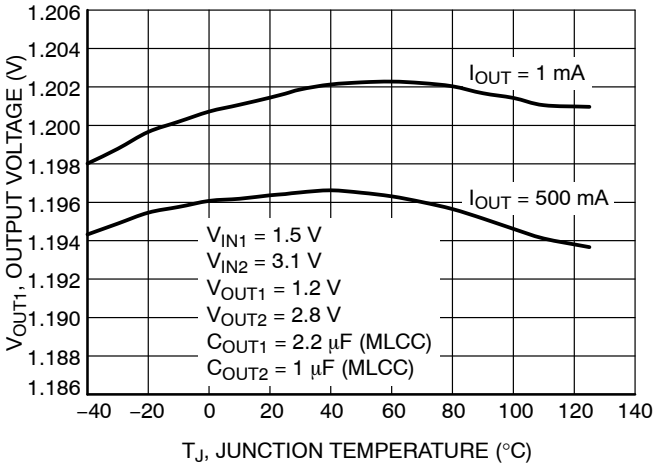


Figure 3. Output Voltage vs. Temperature – V_{OUT1} = 1.2 V

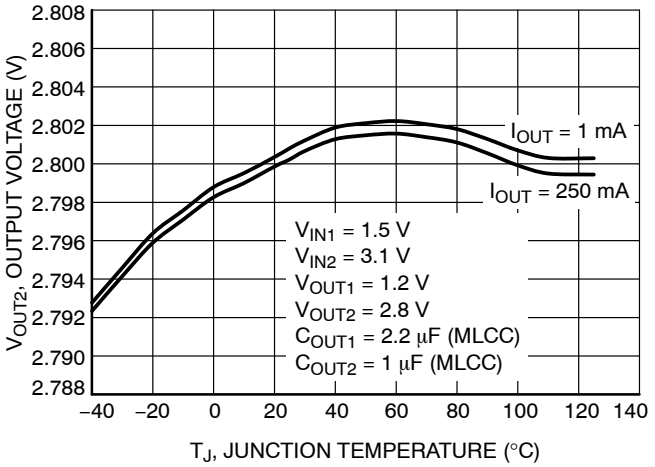


Figure 4. Output Voltage vs. Temperature – V_{OUT2} = 2.8 V

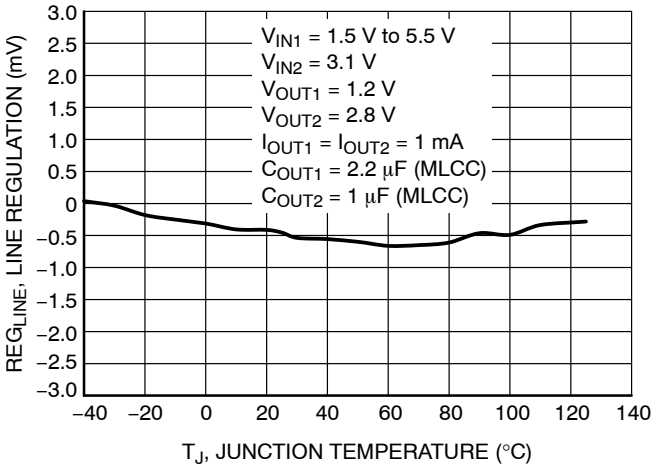


Figure 5. Line Regulation vs. Temperature – V_{OUT1} = 1.2 V

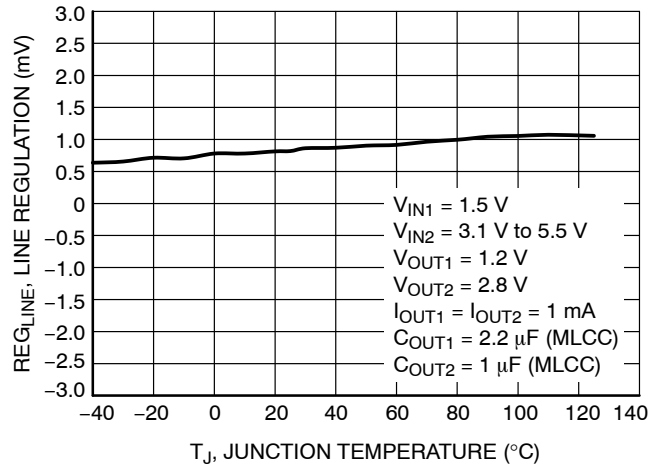


Figure 6. Line Regulation vs. Temperature – V_{OUT} = 2.8 V

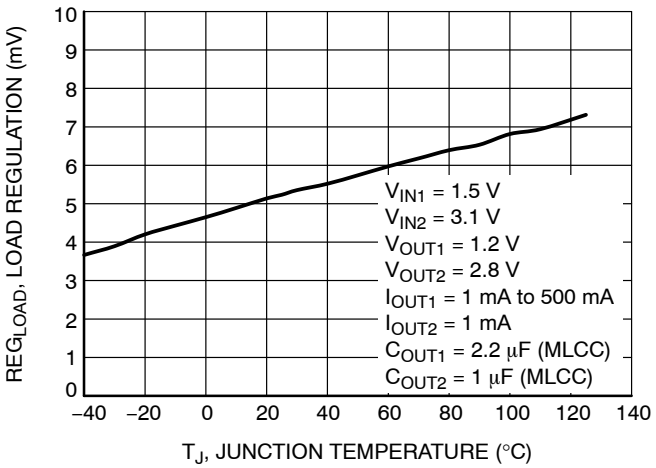


Figure 7. Load Regulation vs. Temperature – V_{OUT1} = 1.2 V

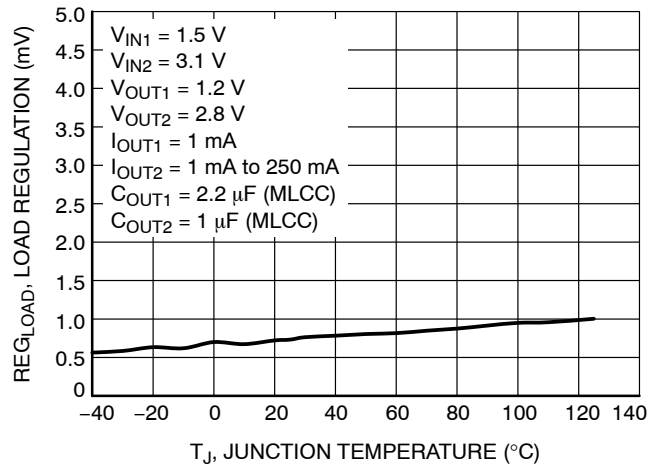


Figure 8. Load Regulation vs. Temperature – V_{OUT} = 2.8 V

APPLICATIONS INFORMATION

General

The NCP156 is a 500 mA/250 mA dual output high performance Low Dropout Linear Regulator. It offers unique combination of N−MOS and P−MOS regulators to provide the best performance and power efficiency. The device is optimized for camera sensor applications to supply digital and analog power rails. Digital supply rail requires high current, low input voltage and as low as possible dropout to achieve the best efficiency and analog pixel array requires less current but very stable and clean supply line with very fast transient response. The NCP156 is offered in WLCSP6 package which helps with high integration as close as possible to sensor for best parameters.

Input Capacitor Selection (C_{IN})

It is recommended to connect at least a 1 μF Ceramic X5R or X7R capacitor as close as possible to the IN pin of the device. Larger input capacitor may be necessary if fast and large load transients are encountered in the application. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. or max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling (C_{OUT})

The NCP156 requires an output capacitor for each output connected as close as possible to the output pin of the regulator. The recommended capacitor value for OUT1 is 2.2 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. Recommended output capacitor for OUT2 is 1 μF same type as OUT1. The NCP156 is designed to remain stable with minimum effective capacitance of 1 μF for OUT1 and 0.7 μF for OUT2 to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 1.9 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum or electrolytic capacitors on the output due to their large ESR. They can be used in connection with appropriate ceramic capacitor as secondary energy reservoir.

Input Voltage Requirements

The NCP156 is combination N−MOS and P−MOS regulators in one package. It brings specific needs to proper design of power supply voltage rails. Input voltage 1 can be as low as $V_{OUT1\_NOM}+V_{DO1}$ with minimal impact on performance. Typical parameters are characterized for V_{OUT1_NOM} + 0.3 V. The input voltage 2 is used as bias voltage of N−MOS output together with supply OUT2 and must be chosen more carefully. The basic condition to V_{IN2} selections is the same as for first input $V_{IN2} \geq V_{OUT2\_NOM} + V_{DO2}$. Due to the fact that V_{IN2} is also bias voltage for N−MOS regulator difference between V_{OUT1} and V_{IN2} must be at least 1.5 V.

The internal voltage references for both channels have cascade topology. It means reference V_{REF2} for OUT2 is derived from IN2 and reference for OUT1 is derived also from reference V_{REF2} not from V_{IN1}. All negative effects on V_{REF2} is visible also on V_{REF1} and then on V_{OUT1}. The reference voltage V_{REF2} has same value as V_{OUT2} due to there is necessary to have enough voltage headroom between V_{IN2} and V_{OUT2}. If V_{OUT2} is in dropout region then OUT1 is affected too. Consequently the OUT1 output voltage is lower than nominal due to lower V_{REF1} reference which is affected by drop V_{REF2}. For more information please refer design note DN05110/D.

Enable Operation

The NCP156 uses the single EN pin for both output channels. If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistors are turned−off so that there is virtually no current flow between the INs and OUTs. According to selected option the active discharge transistors are active so that the output voltages are pulled to GND through a 150 Ω resistor. In the disable state the device consumes as low as typ. 150 nA from the power supply. Active discharge feature is available for each output and can be select during manufacturing. It is necessary to choose correct option by exact device part number. Possible OPN configurations are in Table 5 below.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCP156 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 300 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

Slew Rate Control

The NCP156 is optimized for camera sensor application and meets all requirements for using in modern camera applications such as a smartphones, cameras and image capture devices. Power supply specification of sensors often requires output voltage slew rate limitation to protect sensor during regulator start−up. The NCP156 incorporates soft−start feature which can assure safe start−up output voltage ramp without excess current spikes and voltage undershoots. The device provides two options of slew rate speed, normal means typical slew rate about 100/200 mV/μs (OUT1/OUT2) and slow option means <15/30 mV/μs. Option is set during manufacturing process and cannot be

modified later. The possible slew rate configuration is explained in below in Table 6.

Output Current Limit

The NCP156 provides output overcurrent protection on each output which limits maximum output current. Typical values are 850 mA for OUT1 and 550 mA for OUT2. The NCP156 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current typically to 880 mA on OUT1 and 590 mA on OUT2. The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration. This protection works separately for each channel. Short circuit on the one channel do not influence second channel which will work according to specification.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the affected channel is turn−off. Second channel still working. The channel which is overheated will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the device temperature falls below the 140°C the appropriate channel is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking. The long duration of the short circuit condition to some output channel could cause turn−off other output when heat sinking is not enough and temperature of the other output reach T_{SD} temperature.

Power Dissipation

As power dissipated in the NCP156 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP156 can handle is given by:

$$P_{D(MAX)} = \frac{125^{\circ}C - T_A}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP156 for given application conditions can be calculated from the following equations:

$$P_D \approx \left(V_{IN1} \times I_{GND1}\right) + \left(V_{IN2} \times I_{GND2}\right) + \\ + I_{OUT1}\left(V_{IN1} - V_{OUT1}\right) + I_{OUT2}\left(V_{IN2} - V_{OUT2}\right) \quad \text{(eq. 2)}$$

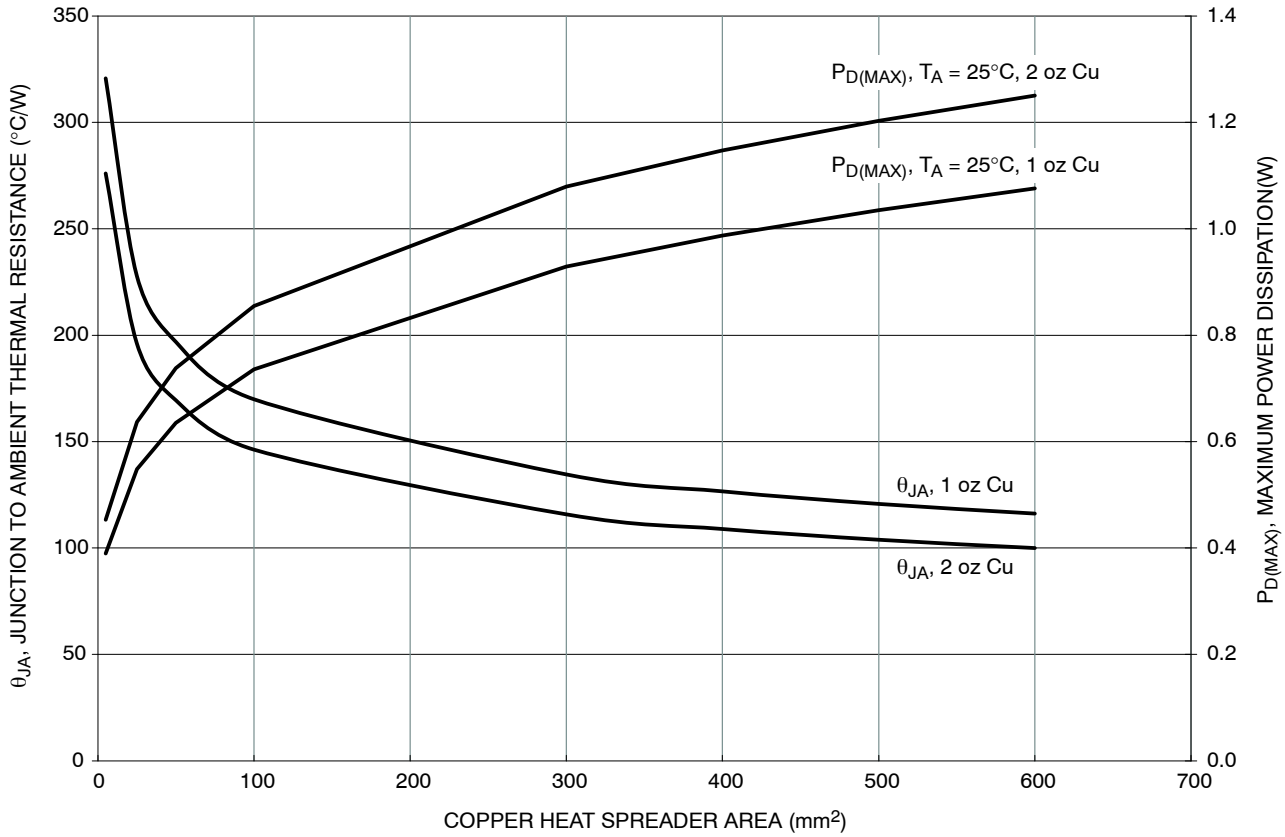


Figure 9. θ_{JA} vs. Copper Area (WLCSP−6)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCP156 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place input and output capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad should be tied the shortest path to the GND pin.

OPN Selection Guide

The NCP156 device offers various combinations of active discharge feature and V_{OUT} slew rate speed for each output channel. The OPN contains two letters behind product name which are dedicated for Active discharge and Slew rate speed. Possible combinations with corresponding letters are explained below.

Table 5. ACTIVE DISCHARGE OPTION

Act. Discharge (x = ON)	OUT1	OUT2
A	x	x
B		
C	x	
D		x

Table 6. V_{OUT} SLEW RATE SPEED

Slew rate (x = Slower)	OUT1	OUT2
A	x	x
B		
C	x	
D		x

ORDERING INFORMATION

Device	Marking	Voltage Option OUT1 / OUT2	Active Discharge OUT1 / OUT2	V_{OUT} Slew Rate OUT1 / OUT2	Package	Shipping†
NCP156AAFCT100280T2G*	DL	1.0 V / 2.8 V	Yes / Yes	Slow / Slow	WLCSP6 (Pb−Free)	5000 / Tape & Reel
NCP156AAFCT105280T2G	DM	1.05 V / 2.8 V	Yes / Yes	Slow / Slow		
NCP156AAFCT110280T2G*	DN	1.1 V / 2.8 V	Yes / Yes	Slow / Slow		
NCP156AAFCT120180T2G*	DA	1.2 V / 1.8 V	Yes / Yes	Slow / Slow		
NCP156AAFCT120270T2G*	DP	1.2 V / 2.7 V	Yes / Yes	Slow / Slow		
NCP156AAFCT120280T2G	DR	1.2 V / 2.8 V	Yes / Yes	Slow / Slow		
NCP156ABFCT100280T2G	DD	1.0 V / 2.8 V	Yes / Yes	Normal / Normal		
NCP156ABFCT105280T2G*	DK	1.05 V / 2.8 V	Yes / Yes	Normal / Normal		
NCP156ABFCT110280T2G	DE	1.1 V / 2.8 V	Yes / Yes	Normal / Normal		
NCP156ABFCT120270T2G*	DG	1.2 V / 2.7 V	Yes / Yes	Normal / Normal		
NCP156ABFCT120280T2G	DF	1.2 V / 2.8 V	Yes / Yes	Normal / Normal		
NCP156ABFCT180250T2G*	DJ	1.8 V / 2.5 V	Yes / Yes	Normal / Normal		
NCP156ABFCT180270T2G*	DH	1.8 V / 2.7 V	Yes / Yes	Normal / Normal		
NCP156BBFCT120180T2G*	DC	1.2 V / 1.8 V	No / No	Normal / Normal		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Please contact local sales representative for availability.

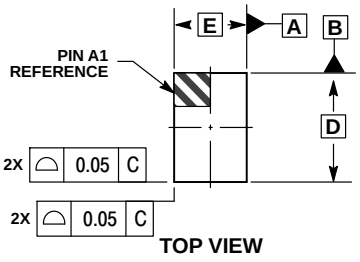
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

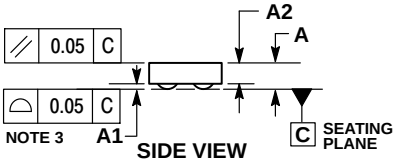
WLCSP6, 1.20x0.80
CASE 567MV
ISSUE B

SCALE 4:1

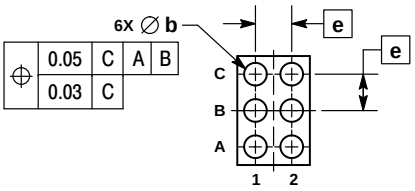
DATE 05 JUN 2018



TOP VIEW



SIDE VIEW

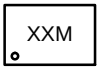


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	–––	0.33
A1	0.04	0.08
A2	0.23 REF	
b	0.24	0.30
D	1.20 BSC	
E	0.80 BSC	
e	0.40 BSC	

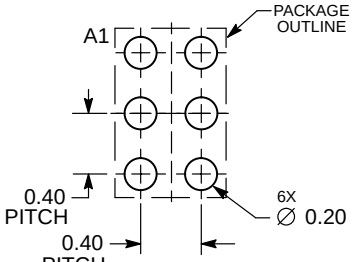
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP6, 1.20x0.80**		**PAGE 1 OF 1**

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