Voltage Regulator
Adjustable Output, Low Dropout

800 mA

MC33269, NCV33269

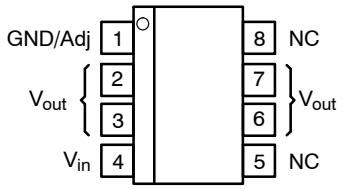
The MC33269/NCV33269 series are low dropout, medium current, fixed and adjustable, positive voltage regulators specifically designed for use in low input voltage applications. These devices offer the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum.

The regulator consists of a 1.0 V dropout composite PNP−NPN pass transistor, current limiting, and thermal shutdown.

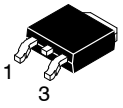
Features

- 3.3 V, 3.5 V, 5.0 V, 12 V and Adjustable Versions
  2.85 V version available as MC34268
- Space Saving DPAK, SO−8 and SOT−223 Power Packages
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.0% Tolerance
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

SO−8
D SUFFIX
CASE 751

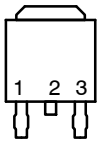


(Top View)



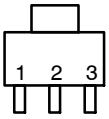
DPAK
DT SUFFIX
CASE 369C

1. GND/Adj
2. V_{out}
3. V_{in}



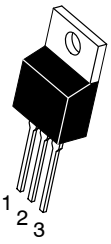
(Top View)

SOT−223
ST SUFFIX
CASE 318E



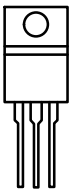
(Top View)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.



TO−220AB
T SUFFIX
CASE 221AB

1. GND/Adj
2. V_{out}
3. V_{in}



(Top View)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC33269D	Adj	MC33269T−3.5	3.5 V
NCV33269D*	Adj	MC33269D−5.0	5.0 V
MC33269DT	Adj	MC33269DT−5.0	5.0 V
NCV33269DTRK*	Adj	NCV33269DT−5.0*	5.0 V
MC33269T	Adj	NCV33269DTRK−5.0*	5.0 V
MC33269D−3.3	3.3 V	MC33269T−5.0	5.0 V
MC33269DT−3.3	3.3 V	MC33269D−012	12 V
NCV33269DTRK−3.3*	3.3 V	MC33269DT−012	12 V
MC33269T−3.3	3.3 V	NCV33269DTRK−012*	12 V
MC33269ST−3.3	3.3 V	MC33269T−012	12 V

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

MAXIMUM RATINGS

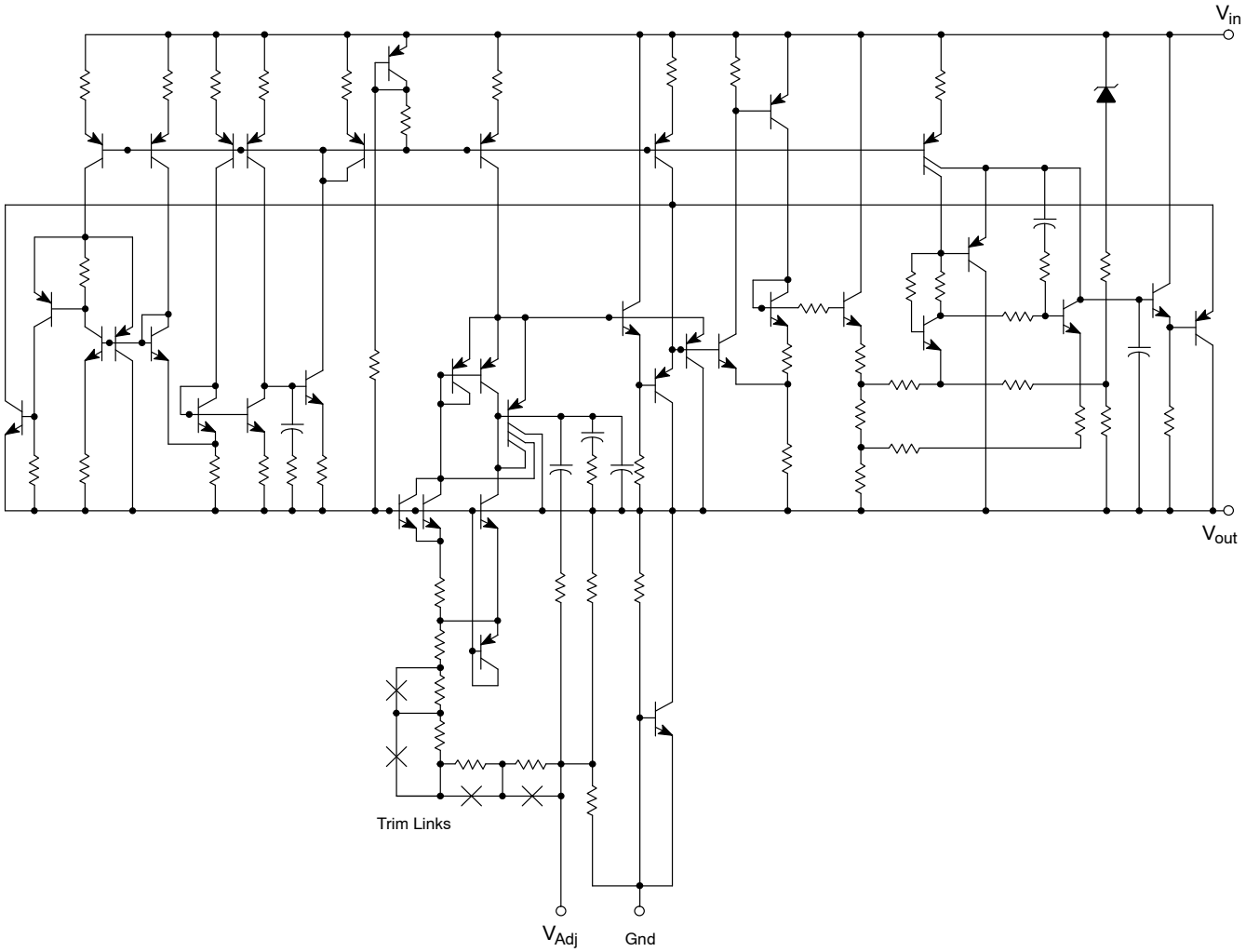
Rating		Symbol	Value	Unit
Power Supply Input Voltage		V_{in}	20	V
Power Dissipation				
Case 369C (DPAK)	T_A = 25°C	P_D	Internally Limited	W
	Thermal Resistance, Junction−to−Ambient	θ_{JA}	92	°C/W
	Thermal Resistance, Junction−to−Case	θ_{JC}	6.0	°C/W
Case 751 (SO−8)	T_A = 25°C	P_D	Internally Limited	W
	Thermal Resistance, Junction−to−Ambient	θ_{JA}	160	°C/W
	Thermal Resistance, Junction−to−Case	θ_{JC}	25	°C/W
Case 221A (TO−220)	T_A = 25°C	P_D	Internally Limited	W
	Thermal Resistance, Junction−to−Ambient	θ_{JA}	65	°C/W
	Thermal Resistance, Junction−to−Case	θ_{JC}	5.0	°C/W
Case 318E (SOT−223)	T_A = 25°C	P_D	Internally Limited	W
	Thermal Resistance, Junction−to−Ambient	θ_{JA}	156	°C/W
	Thermal Resistance, Junction−to−Case	θ_{JC}	15	°C/W
Operating Die Junction Temperature Range		T_J	−40 to +150	°C
Operating Ambient Temperature Range	MC33269	T_A	−40 to +125	°C
	NCV33269		−40 to +125	
Storage Temperature		T_{stg}	−55 to +150	°C
Electrostatic Discharge Sensitivity (ESD)	Human Body Model (HBM)	ESD	4000	V
	Machine Model (MM)		400	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (C_O = 10 μF, T_A = 25°C, for min/max values T_A = −40°C to +125°C, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Voltage (I_{out} = 10 mA, T_A = 25°C)		V_O				V
	3.3 Suffix (V_{CC} = 5.3 V)		3.27	3.3	3.33	
	3.5 Suffix (V_{CC} = 5.5 V)		3.465	3.5	3.535	
	5.0 Suffix (V_{CC} = 7.0 V)		4.95	5.0	5.05	
	12 Suffix (V_{CC} = 14 V)		11.88	12	12.12	
Output Voltage (Line, Load and Temperature) (Note 1) (1.25 V ≤ V_{in} − V_{out} ≤ 15 V, I_{out} = 500 mA) (1.35 V ≤ V_{in} − V_{out} ≤ 10 V, I_{out} = 800 mA)		V_O				V
	3.3 Suffix		3.23	3.3	3.37	
	3.5 Suffix		3.43	3.5	3.57	
	5.0 Suffix		4.90	5.0	5.10	
	12 Suffix		11.76	12	12.24	
Reference Voltage for Adjustable Voltage (I_{out} = 10 mA, V_{in} − V_{out} = 2.0 V, T_A = 25°C)		V_{ref}	1.235	1.25	1.265	V
Reference Voltage (Line, Load and Temperature) (Note 1) for Adjustable Voltage (1.25 V ≤ V_{in} − V_{out} ≤ 15 V, I_{out} = 500 mA) (1.35 V ≤ V_{in} − V_{out} ≤ 10 V, I_{out} = 800 mA)		V_{ref}	1.225	1.25	1.275	V
Line Regulation	(I_{out} = 10 mA, V_{in} = [V_{out} + 1.5 V] to V_{in} = 20 V, T_A = 25°C)	Reg_{line}	–	–	0.3	%
Load Regulation	(V_{in} = V_{out} + 3.0 V, I_{out} = 10 mA to 800 mA, T_A = 25°C)	Reg_{load}	–	–	0.5	%
Dropout Voltage	(I_{out} = 500 mA)	V_{in} − V_{out}	–	1.0	1.25	V
	(I_{out} = 800 mA)		–	1.1	1.35	
Ripple Rejection	(10 V_{pp}, 120 Hz Sinewave; I_{out} = 500 mA)	RR	55	–	–	dB
Current Limit	(V_{in} − V_{out} = 10 V)	I_{Limit}	800	–	–	mA
Quiescent Current (Fixed Output)	(1.5 V ≤ V_{out} ≤ 3.5 V)	I_Q	–	5.5	8.0	mA
	(5 V ≤ V_{out} ≤ 12 V)		–	–	20	
Minimum Required Load Current	Fixed Output Voltage	I_{Load}	–	–	0	mA
	Adjustable Voltage		8.0	–	–	
Adjustment Pin Current		I_{Adj}	–	–	120	μA

1. The MC33269−12, V_{in} − V_{out} is limited to 8.0 V maximum, because of the 20 V maximum rating applied to V_{in}.



This device contains 38 active transistors.

Figure 1. Internal Schematic

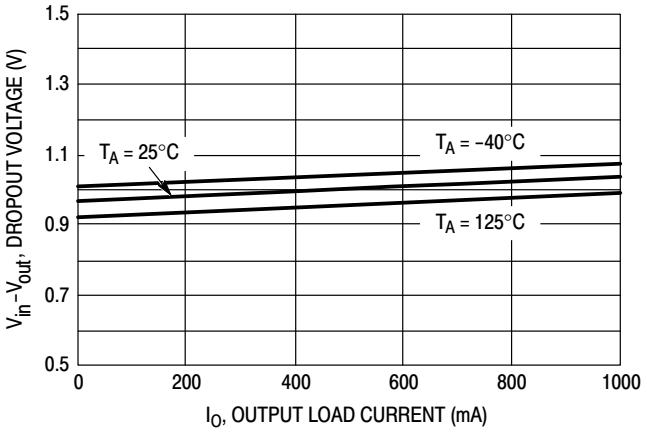


Figure 2. Dropout Voltage versus Output Load Current

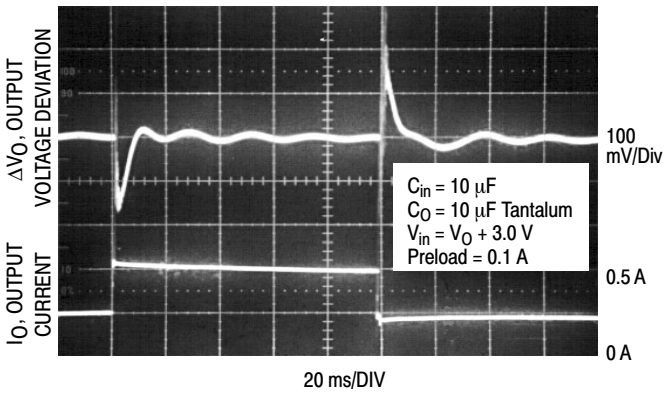


Figure 3. Transient Load Regulation

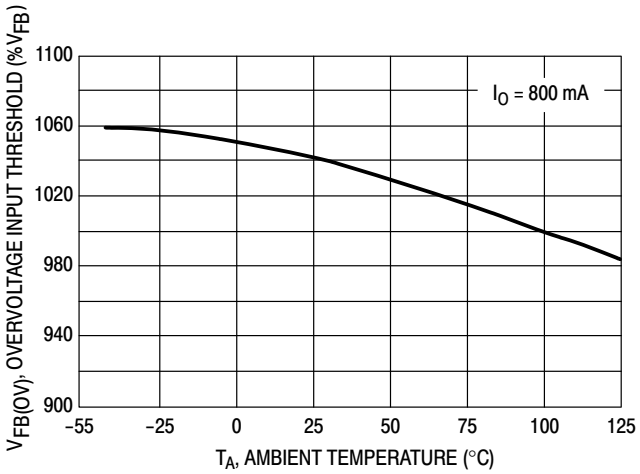


Figure 4. Dropout Voltage versus Temperature

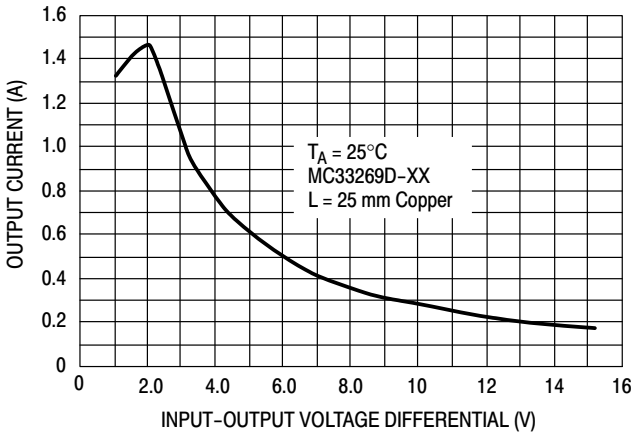


Figure 5. MC33269−XX Output DC Current versus Input−Output Differential Voltage

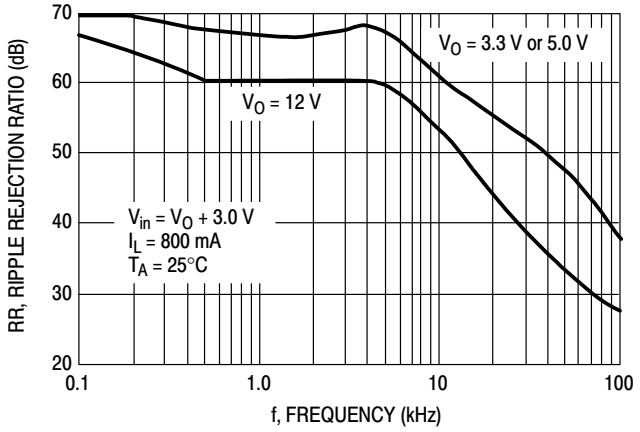


Figure 6. MC33269 Ripple Rejection versus Frequency

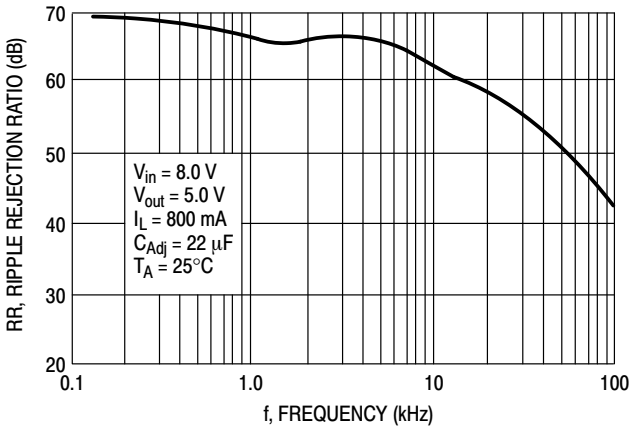


Figure 7. MC33269−ADJ Ripple Rejection versus Frequency

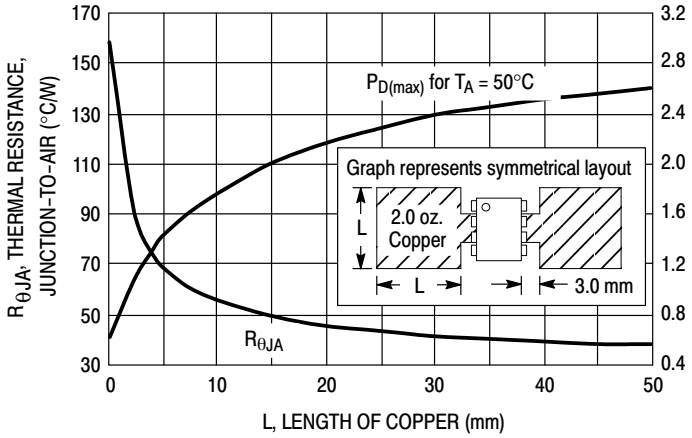


Figure 8. SOP−8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

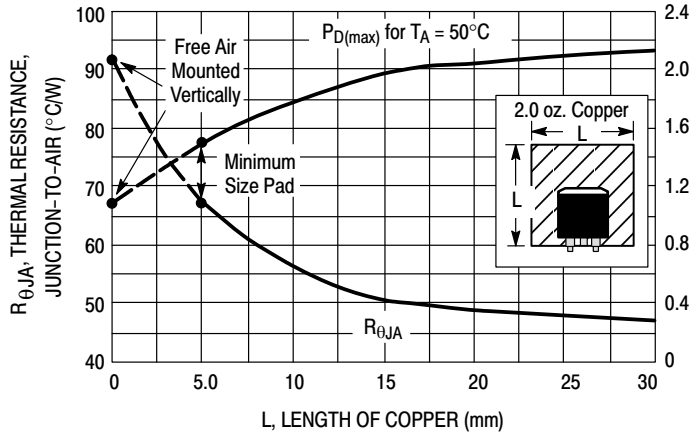


Figure 9. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

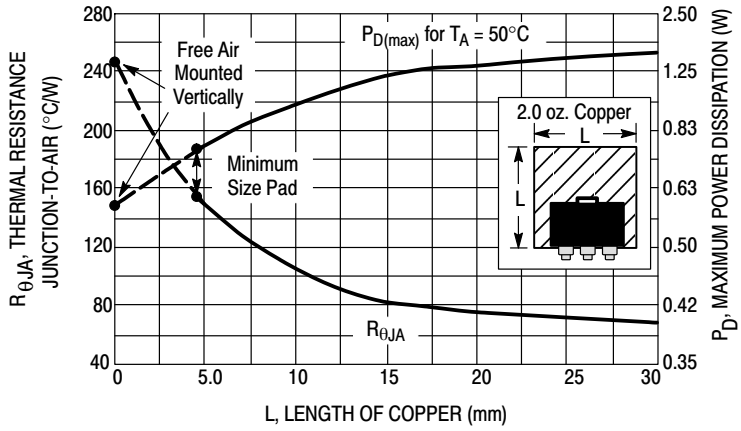


Figure 10. SOT−223 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

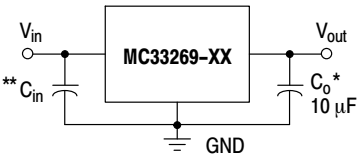
APPLICATIONS INFORMATION

Figures 11 through 15 are typical application circuits. The output current capability of the regulator is in excess of 800 mA, with a typical dropout voltage of less than 1.0 V. Internal protective features include current and thermal limiting.

* The MC33269 requires an external output capacitor for stability. The capacitor should be at least 10 μF with an equivalent series resistance (ESR) of less than 10 Ω but greater than 0.2 Ω over the anticipated operating temperature range. With economical electrolytic capacitors, cold temperature operation can pose a problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Also capacitance and ESR of a solid tantalum capacitor is more stable over temperature. The use of a low ESR ceramic capacitor placed within close proximity to the output of the device could cause instability.

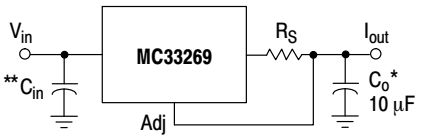
** An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the supply input filter with long wire lengths. This will reduce the circuit's sensitivity to the input line impedance at high frequencies. A 0.33 μF or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. **Applications should be tested over all operating conditions to insure stability.**

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the output is disabled. There is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heat−sinking.**



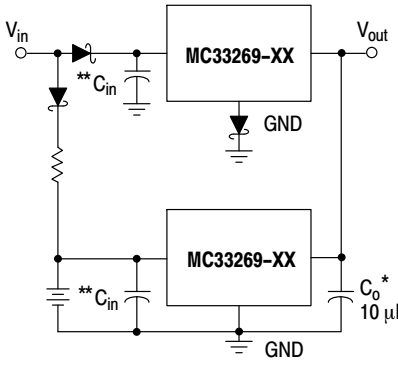
An input capacitor is not necessary for stability, however it will improve the overall performance.

Figure 11. Typical Fixed Output Application



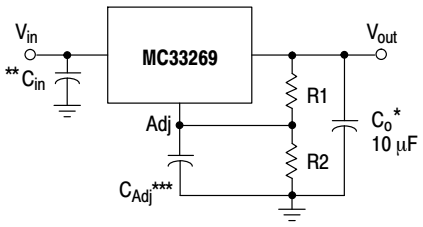
$$I_{out} = \frac{1.25}{R_S}$$

Figure 13. Current Regulator



The Schottky diode in series with the ground leg of the upper regulator shifts its output voltage higher by the forward voltage drop of the diode. This will cause the lower device to remain off until the input voltage is removed.

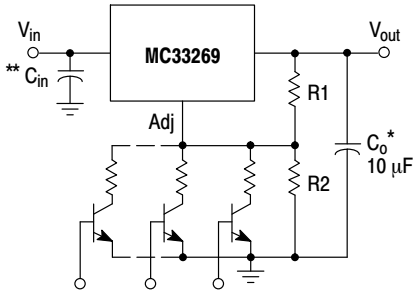
Figure 14. Battery Backed−Up Power Supply



$$V_{out} = 1.25 \left(1 + \frac{R2}{R1}\right) + I_{Adj} R2$$

***C_{Adj} is optional, however it will improve the ripple rejection. The MC34269 develops a 1.25 V reference voltage between the output and the adjust terminal. Resistor R1, operates with constant current to flow through it and resistor R2. This current should be set such that the Adjust Pin current causes negligible drop across resistor R2. The total current with minimum load should be greater than 8.0 mA.

Figure 12. Typical Adjustable Output Application



R_2 sets the maximum output voltage. Each transistor reduces the output voltage when turned on.

Figure 15. Digitally Controlled Voltage Regulator

ORDERING INFORMATION

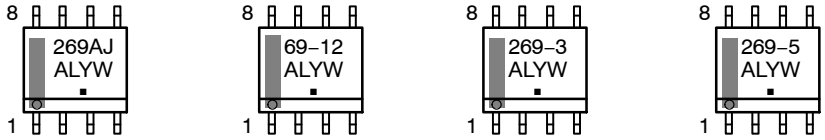
Device	Package	Shipping Information†
MC33269DR2G	SO−8 (Pb−Free)	2500 Units / Tape & Reel
MC33269DTRKG	DPAK (Pb−Free)	2500 Units / Tape & Reel
MC33269D−3.3G	SO−8 (Pb−Free)	98 Units / Rail
MC33269DR2−3.3G	SO−8 (Pb−Free)	2500 Units / Tape & Reel
MC33269DT−3.3G	DPAK (Pb−Free)	75 Units / Rail
MC33269DTRK−3.3G	DPAK (Pb−Free)	2500 Units / Tape & Reel
MC33269ST−3.3T3G	SOT−223 (Pb−Free)	4000 Units / Tape & Reel
MC33269T−3.3G	TO−220 (Pb−Free)	50 Units / Rail
MC33269DR2−5.0G	SO−8 (Pb−Free)	2500 Units / Tape & Reel
NCV33269DT−5.0G*	DPAK (Pb−Free)	75 Units / Rail
MC33269DTRK−5.0G	DPAK (Pb−Free)	2500 Units / Tape & Reel
NCV33269DR2G*	SO−8 (Pb−Free)	2500 Units / Tape & Reel
NCV33269DTRKG*	DPAK (Pb−Free)	2500 Units / Tape & Reel
NCV33269DTRK3.3G*	DPAK (Pb−Free)	2500 Units / Tape & Reel
NCV33269DTRK5.0G*	DPAK (Pb−Free)	2500 Units / Tape & Reel
NCV33269DTRK−12G*	DPAK (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

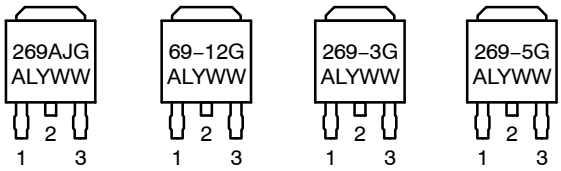
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MARKING DIAGRAMS

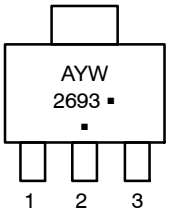
SO−8
D SUFFIX
CASE 751



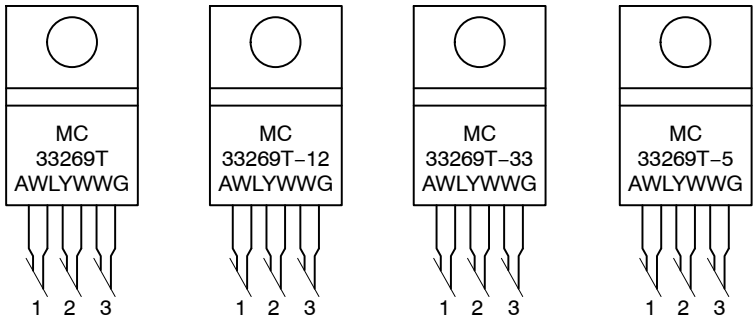
DPAK
DT SUFFIX
CASE 369C



SOT−223
ST SUFFIX
CASE 318E



TO−220AB
T SUFFIX
CASE 221A

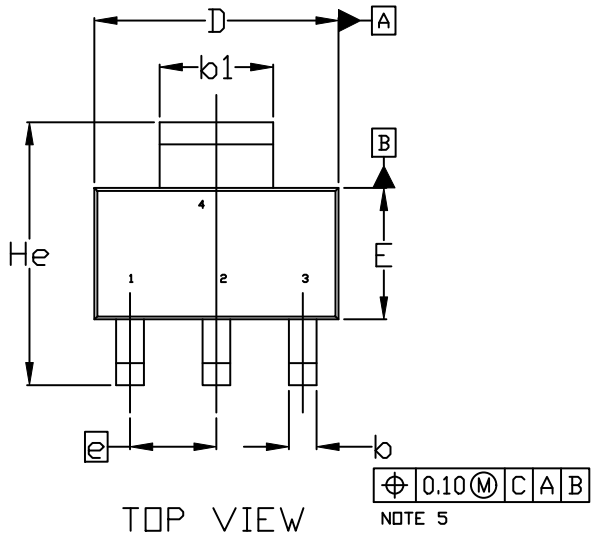


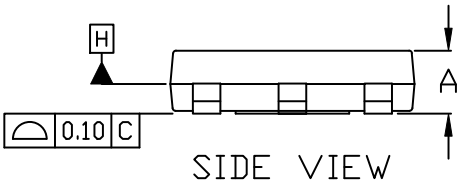
A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
G = Pb−Free Package
▪ = Pb−Free Package
(Note: Microdot may be in either location)

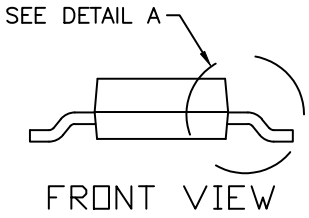
SCALE 1:1

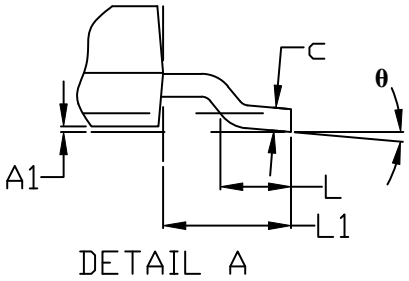
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



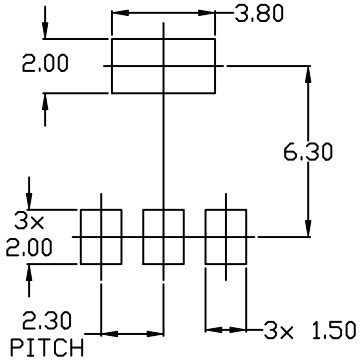






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

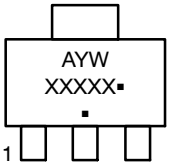
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*

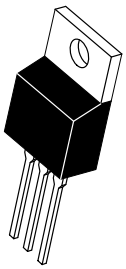


A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

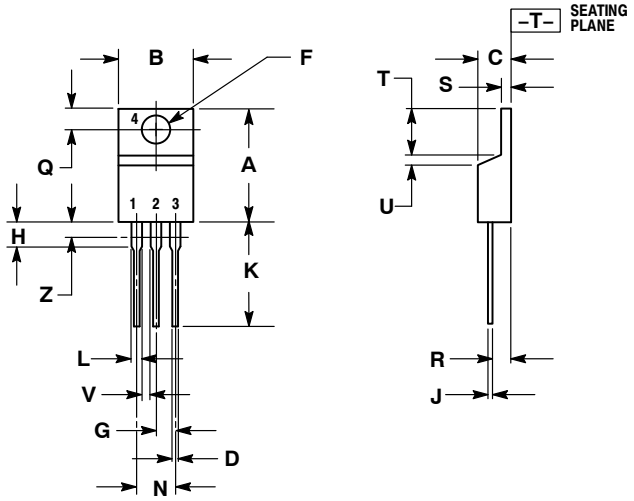
DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOT−223 (TO−261)	PAGE 2 OF 2



SCALE 1:1

TO−220, SINGLE GAUGE
CASE 221AB−01
ISSUE A

DATE 16 NOV 2010



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. PRODUCT SHIPPED PRIOR TO 2008 HAD DIMENSIONS S = 0.045 − 0.055 INCHES (1.143 − 1.397 MM)

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.024	0.508	0.61
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

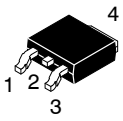
STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

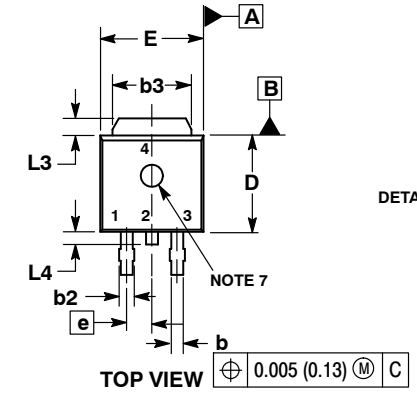
ON Semiconductor®

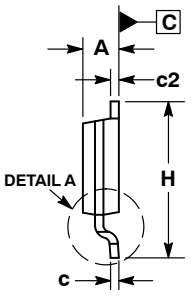


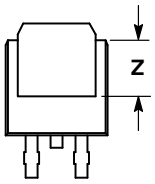
SCALE 1:1

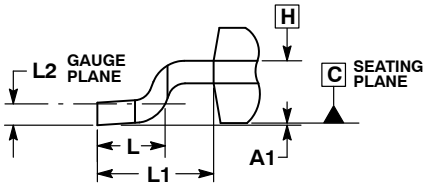
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

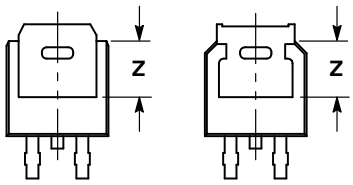
DATE 21 JUL 2015











NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

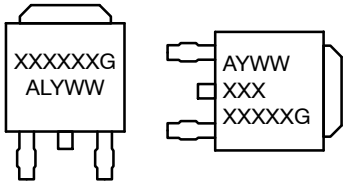
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

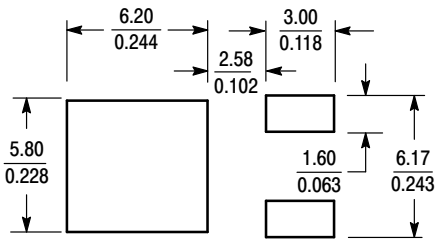


IC Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

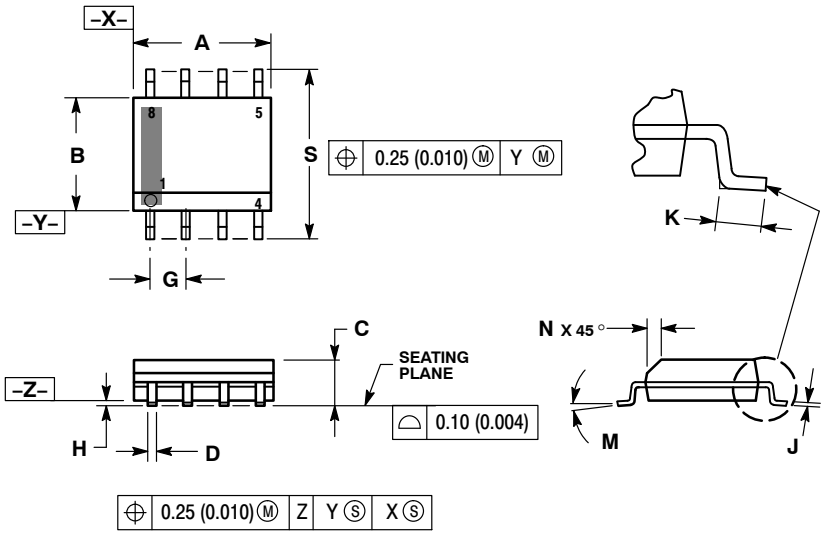
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

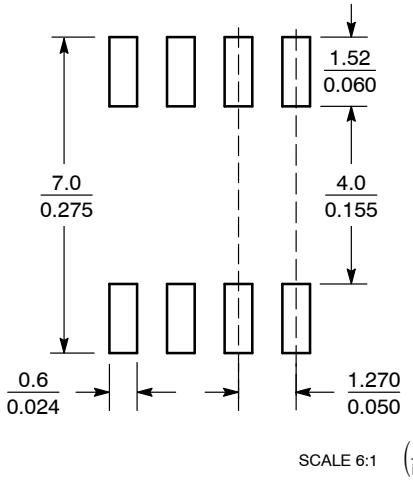
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

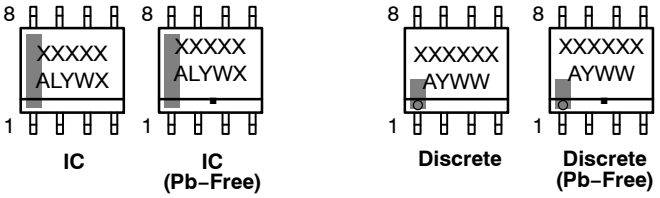
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

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