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FDMC010N08C

N-Channel Shielded Gate PowerTrench $^{\! (\! R \!)}$ MOSFET 80 V, 51 A, 10 $m\Omega$

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 10 m Ω at V_{GS} = 10 V, I_D = 16 A
- Max $r_{DS(on)}$ = 25 m Ω at V_{GS} = 6 V, I_D = 8 A
- 50% lower Qrr than other MOSFET suppliers
- Lowers switching noise/EMI
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

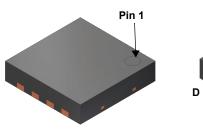


General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

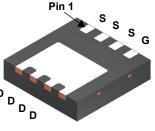
Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar



Top





Bottom

S 1 D S 3 D G 4 D D

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parame	ter		Ratings	Units	
V_{DS}	Drain to Source Voltage			80	V	
V_{GS}	Gate to Source Voltage			±20	V	
	Drain Current -Continuous	T _C = 25 °C	(Note 5)	51		
	-Continuous	T _C = 100 °C	(Note 5)	32	^	
ID	-Continuous	T _A = 25 °C	(Note 1a)	11	Α	
	-Pulsed		(Note 4)	206		
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	96	mJ	
P _D	Power Dissipation	T _C = 25 °C		52	W	
	Power Dissipation	T _A = 25 °C	(Note 1a)	2.4	VV	
T _J , T _{STG}	Operating and Storage Junction Temperat	ture Range		-55 to +150	°C	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC010N08C	FDMC010N08C	Power 33	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25 °C		75		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 64 V, V _{GS} = 0 V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 90 \mu A$	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 90 μA, referenced to 25 °C		-8		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 16 A		8.0	10	
		V _{GS} = 6 V, I _D = 8 A		12.3	25	mΩ
, ,		$V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}, T_J = 125 ^{\circ}\text{C}$		14	18	
9 _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 16 A		35		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz		1070	1500	pF
C _{oss}	Output Capacitance			381	530	pF
C _{rss}	Reverse Transfer Capacitance			20	30	pF
R _g	Gate Resistance		0.1	0.4	0.7	Ω

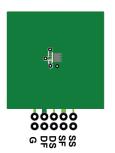
Switching Characteristics

t _{d(on)}	Turn-On Delay Time		9	19	ns
t _r	Rise Time	V _{DD} = 40 V, I _D = 16 A,	3	10	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_{GEN} = 6 Ω	17	31	ns
t _f	Fall Time		5	10	ns
Qg	Total Gate Charge	V _{GS} = 0 V to 10 V	15	22	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to 6 V}$ $V_{DD} = 40 \text{ V},$	10	14	nC
Q_{gs}	Gate to Source Charge	I _D = 16 A	5		nC
Q _{gd}	Gate to Drain "Miller" Charge		3		nC
Q _{oss}	Output Charge	V _{DD} = 40 V, V _{GS} = 0 V	22.1		nC
Q _{svnc}	Total Gate Charge Sync	V _{DS} = 0 V, I _D = 16 A	13.3		nC

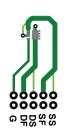
Drain-Source Diode Characteristics

V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2 \text{ A}$ (Note 2)	0.7	1.2	V
	Source to Drain Diode Torward Voltage	V _{GS} = 0 V, I _S = 16 A (Note 2)	0.8	1.3	V
t _{rr}	Reverse Recovery Time	I _F = 8 A, di/dt = 300 A/μs	17	30	ns
Q _{rr}	Reverse Recovery Charge	- 1 _F - 8 A, αι/αι - 300 A/μs	20	33	nC
t _{rr}	Reverse Recovery Time	I _E = 8 A, di/dt = 1000 A/μs	13	23	ns
Q _{rr}	Reverse Recovery Charge	-1 _F - 8 A, αι/αι - 1000 A/μs	45	73	nC

1. R_{0,1A} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,0A} is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

^{2.} Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
3. E_{AS} of 96 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 8 A, V_{DD} = 72 V, V_{GS} = 10 V, 100% test at L = 0.1 mH, I_{AS} = 25 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted.

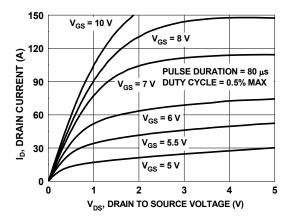


Figure 1. On Region Characteristics

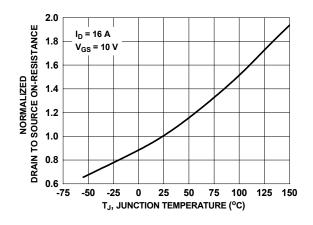


Figure 3. Normalized On Resistance vs. Junction Temperature

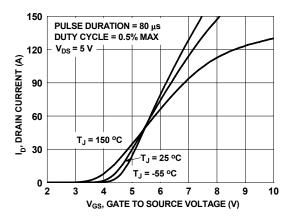


Figure 5. Transfer Characteristics

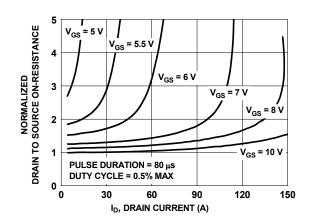


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

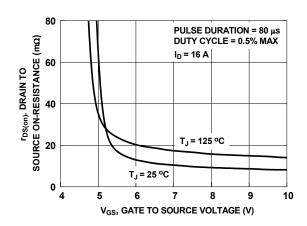


Figure 4. On-Resistance vs. Gate to Source Voltage

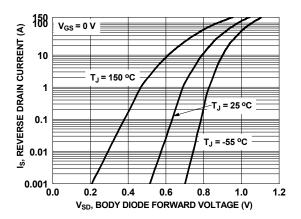


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted.

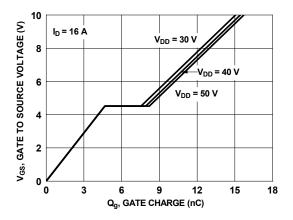


Figure 7. Gate Charge Characteristics

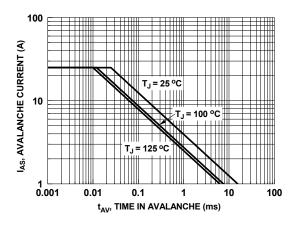


Figure 9. Unclamped Inductive Switching Capability

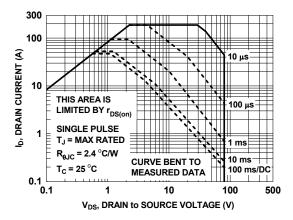


Figure 11. Forward Bias Safe Operating Area

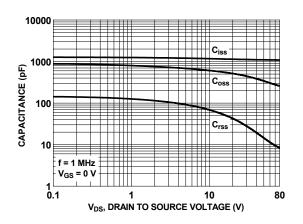


Figure 8. Capacitance vs. Drain to Source Voltage

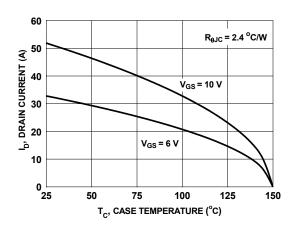


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

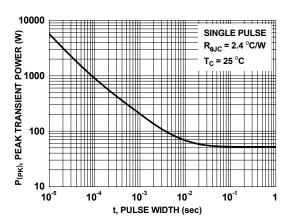


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted.

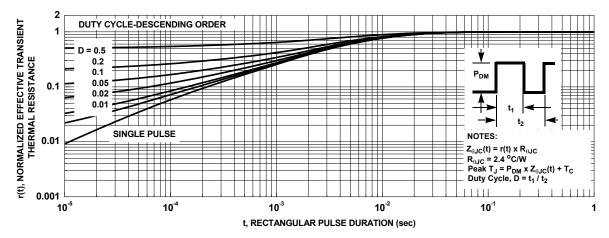
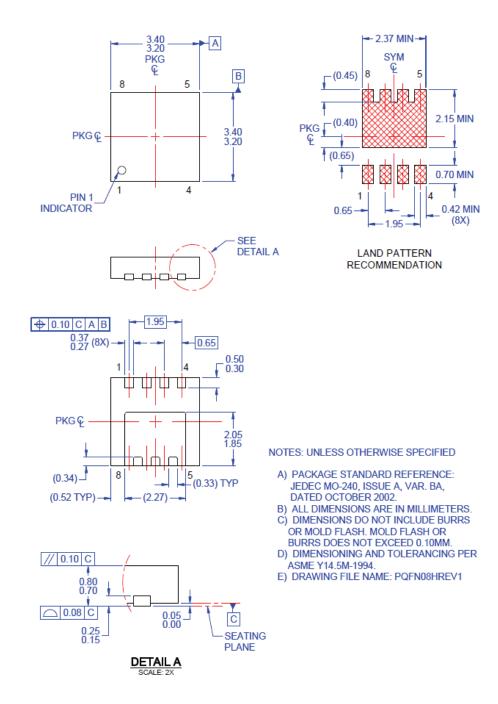


Figure 13. Junction-to-Case Transient Thermal Response Curve

Dimensional Outline and Pad Layout



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