

74LVT162245B

3.3 V 16-bit transceiver with 30 Ω termination resistors;
3-state

Rev. 4 — 6 August 2021

Product data sheet

1. General description

The 74LVT162245B is a 16-bit transceiver with 30 Ω termination resistors and 3-state outputs. The device can be used as two 8-bit transceivers or one 16-bit transceiver. The device features two output enables (1OE and 2OE) each controlling eight outputs, and two send/receive (1DIR and 2DIR) inputs for direction control. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

2. Features and benefits

- 16-bit bidirectional bus interface
- 3-state buffers
- Output capability: +12 mA/-12 mA
- Wide supply voltage range from 2.7 to 3.6 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30 Ω making external termination resistors unnecessary
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM: JESD22-A114F exceeds 2000 V
 - MM: JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | |
| 74LVT162245BDGG | -40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |

4. Functional diagram

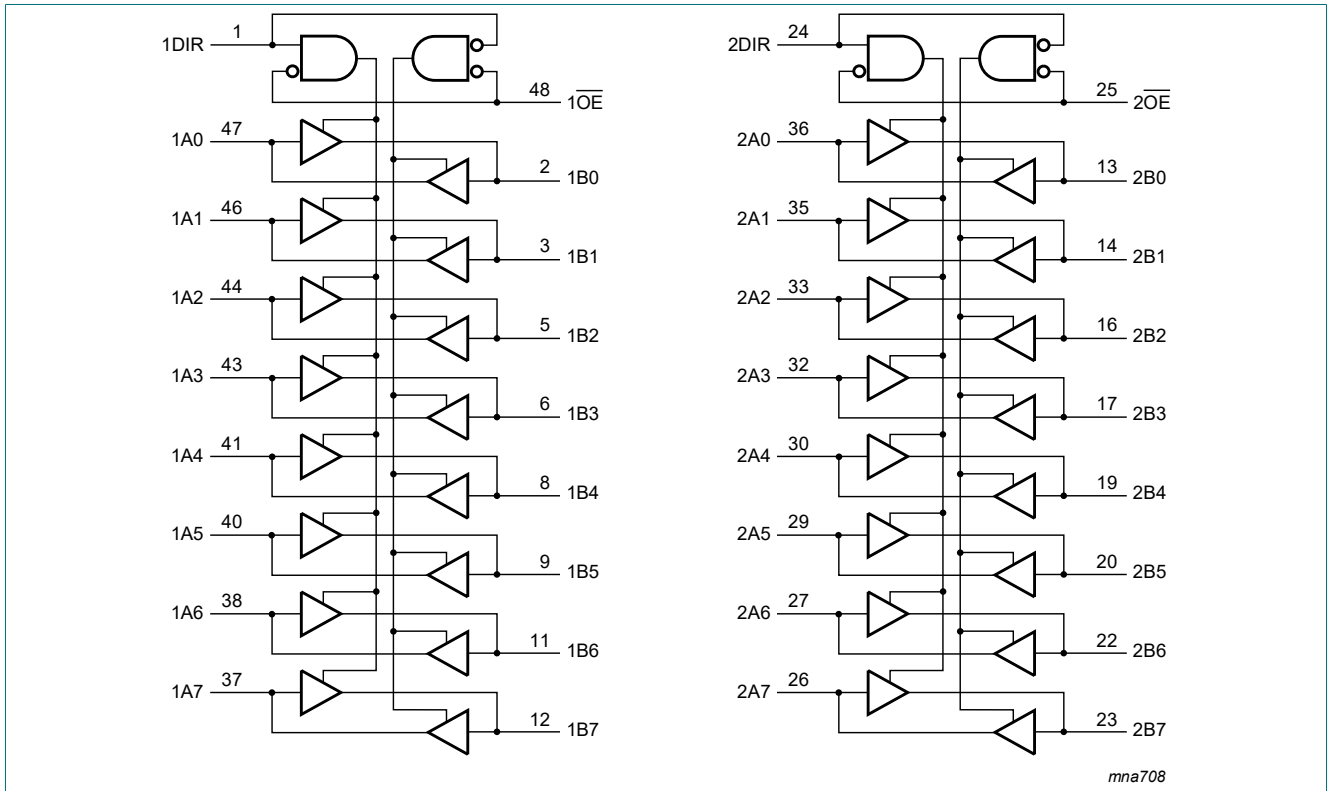


Fig. 1. Logic symbol

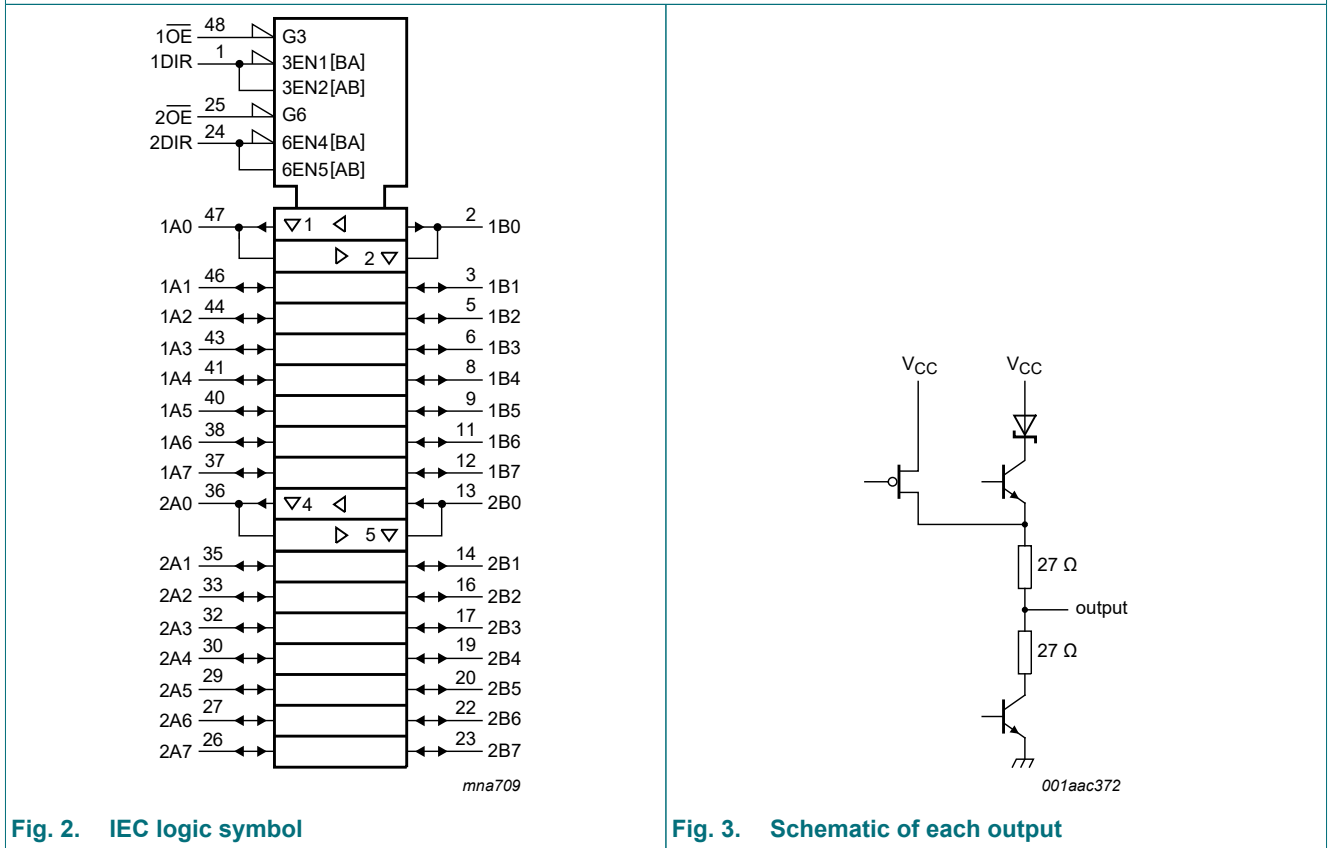


Fig. 2. IEC logic symbol

Fig. 3. Schematic of each output

5. Pinning information

5.1. Pinning

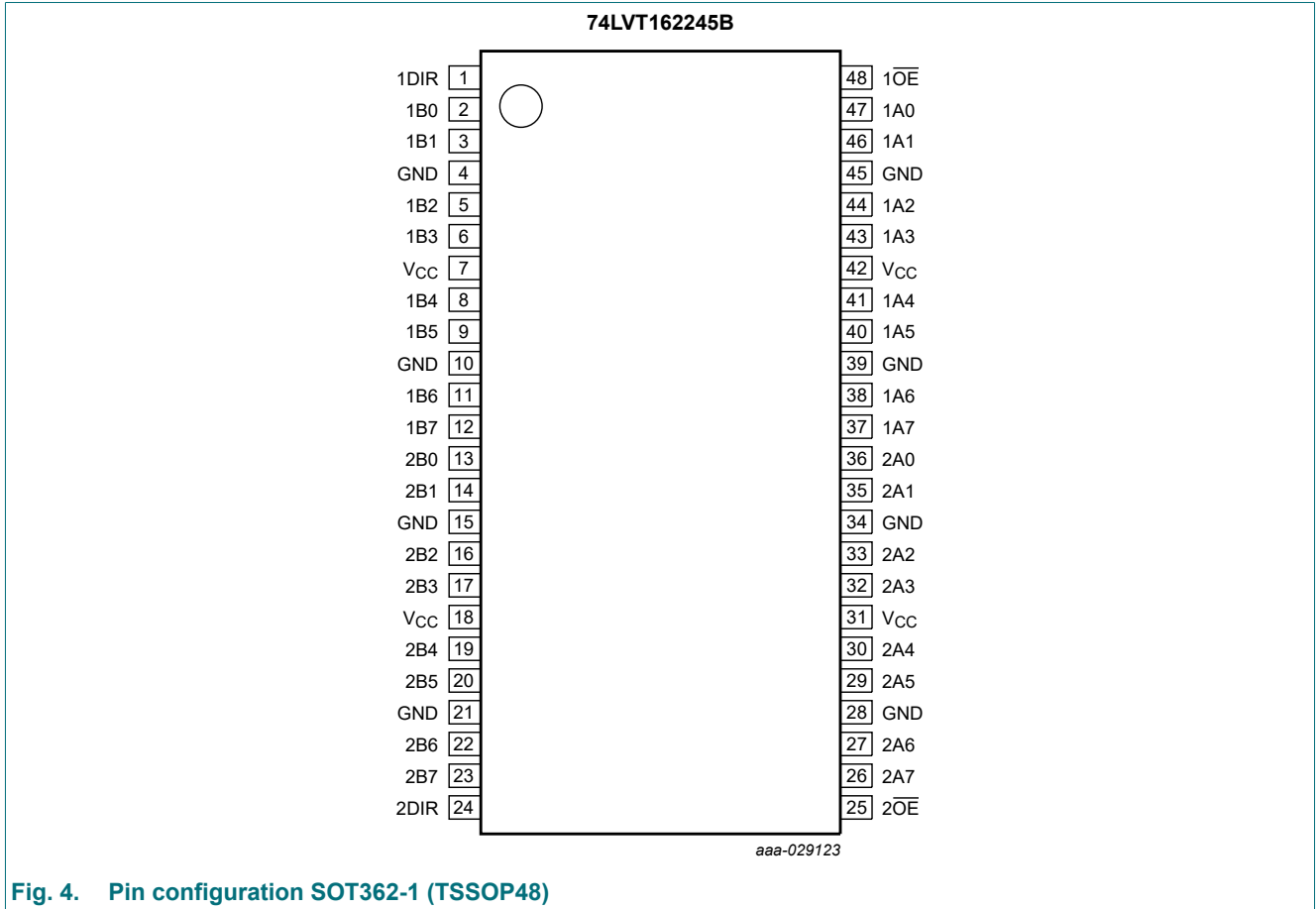


Fig. 4. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--|--------------------------------|-------------------------|
| 1DIR, 2DIR | 1, 24 | direction control input |
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | 47, 46, 44, 43, 41, 40, 38, 37 | data input/output |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | 36, 35, 33, 32, 30, 29, 27, 26 | data input/output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | 2, 3, 5, 6, 8, 9, 11, 12 | data input/output |
| 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | 13, 14, 16, 17, 19, 20, 22, 23 | data input/output |
| 1OE, 2OE | 48, 25 | output enable input |
| VCC | 7, 18, 31, 42 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

| Control | | Input/output | |
|---------|------|------------------|------------------|
| nOE | nDIR | nAn | nBn |
| L | L | output nAn = nBn | input |
| L | H | input | output nBn = nAn |
| H | X | Z | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-----------------------------------|----------|------|--------------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| V_I | input voltage | | [1] -0.5 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state | [1] -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | -50 | - | mA |
| I_O | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | -64 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | $^{\circ}$ C |
| T_j | junction temperature | | [2] - | 150 | $^{\circ}$ C |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-----------------|-----|-----|-----|--------------|
| V_{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | $^{\circ}$ C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | - | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|-----------------|------------------------------------|---|-----|--------|---------------|---------------|
| V_{IK} | input clamping voltage | $V_{CC} = 2.7\text{ V}$; $I_{IK} = -18\text{ mA}$ | - | 0.8 | -1.2 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_{CC} = 3.0\text{ V}$; $I_{OH} = -12\text{ mA}$ | 2.0 | 2.5 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 3.0\text{ V}$; $I_{OL} = 12\text{ mA}$ | - | 0.3 | 0.8 | V |
| I_{OH} | HIGH-level output current | | - | - | -12 | mA |
| I_{OL} | LOW-level output current | | - | - | 12 | mA |
| I_I | input leakage current | control pins | | | | |
| | | $V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$ | - | 0.1 | 10 | μA |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND | - | 0.1 | ± 1 | μA |
| | | I/O data pins; $V_{CC} = 3.6\text{ V}$ [2] | | | | |
| | | $V_I = V_{CC}$ | - | 0.5 | 10 | μA |
| | $V_I = 0\text{ V}$ | - | 0.1 | -5 | μA | |
| I_{OFF} | power-off leakage current | $V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V | - | 0.1 | ± 100 | μA |
| I_{BHL} | bus hold LOW current | $V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$ | 75 | 130 | - | μA |
| I_{BHH} | bus hold HIGH current | $V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$ | -75 | -130 | - | μA |
| I_{BHLO} | bus hold LOW overdrive current | $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$ to 3.6 V [3] | 500 | - | - | μA |
| I_{BHHO} | bus hold HIGH overdrive current | $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$ to 3.6 V [3] | - | - | -500 | μA |
| I_{CEX} | output high leakage current | output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5\text{ V}$; $V_{CC} = 3.0\text{ V}$ | - | 75 | 125 | μA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $n\overline{OE} = \text{don't care}$ [4] | - | 40 | ± 100 | μA |
| I_{OZ} | OFF-state output current | $V_{CC} = 3.6\text{ V}$; $V_I = V_{IL}$ or V_{IH} | | | | |
| | | output HIGH: $V_O = 3.0\text{ V}$ | - | 0.5 | 5 | μA |
| | | output LOW: $V_O = 0.5\text{ V}$ | - | 0.5 | -5 | μA |
| I_{CC} | supply current | $V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$ | | | | |
| | | outputs HIGH | - | 0.07 | 0.12 | mA |
| | | outputs LOW | - | 4.2 | 6 | mA |
| | | outputs disabled [5] | - | 0.07 | 0.12 | mA |
| ΔI_{CC} | additional supply current | per input pin; $V_{CC} = 3\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$ and other inputs at V_{CC} or GND [6] | - | 0.1 | 0.2 | mA |
| C_I | input capacitance | $n\text{DIR}$ and $n\overline{OE}$; $V_I = 0\text{ V}$ or 3.0 V | - | 3 | - | pF |
| $C_{I/O}$ | input/output capacitance | $V_{I/O} = 0\text{ V}$ or 3.0 V | - | 9 | - | pF |

[1] Typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.

From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of 100 μs is permitted. This parameter is valid for $T_{amb} = 25\text{ }^{\circ}\text{C}$ only.

[5] Measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

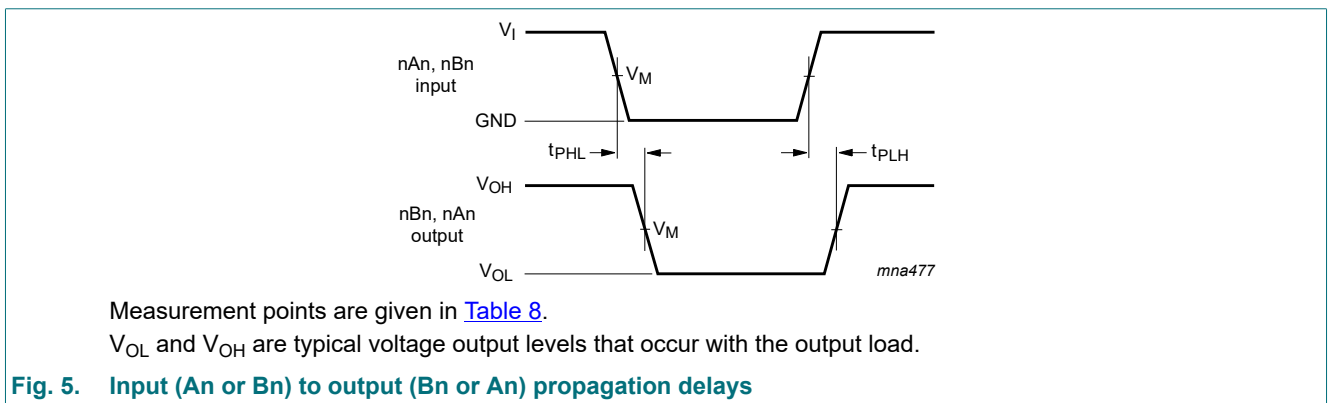
Table 7. Dynamic characteristics

At recommended operating conditions; $T_{amb} = -40\text{ °C}$ to 85 °C ; voltages are referenced to GND (ground = 0 V); for test circuit see [Fig. 7](#).

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|-----------|-------------------------------------|---|-----|--------|-----|------|
| t_{PLH} | LOW to HIGH propagation delay | nAn to nBn or nBn to nAn; see Fig. 5 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 3.9 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | 2.5 | 3.5 | ns |
| t_{PHL} | HIGH to LOW propagation delay | nAn to nBn or nBn to nAn; see Fig. 5 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 3.9 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | 2.2 | 3.5 | ns |
| t_{PZH} | OFF-state to HIGH propagation delay | n \overline{OE} to nAn or nBn; see Fig. 6 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 6.4 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.5 | 3.5 | 5.3 | ns |
| t_{PZL} | OFF-state to LOW propagation delay | n \overline{OE} to nAn or nBn; see Fig. 6 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.0 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.5 | 3.2 | 4.4 | ns |
| t_{PHZ} | HIGH to OFF-state propagation delay | n \overline{OE} to nAn or nBn; see Fig. 6 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.1 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.5 | 3.5 | 4.8 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | n \overline{OE} to nAn or nBn; see Fig. 6 | | | | |
| | | $V_{CC} = 2.7\text{ V}$ | - | - | 5.9 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.5 | 4.3 | 6.7 | ns |

[1] Typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ °C}$.

10.1. Waveforms and test circuit



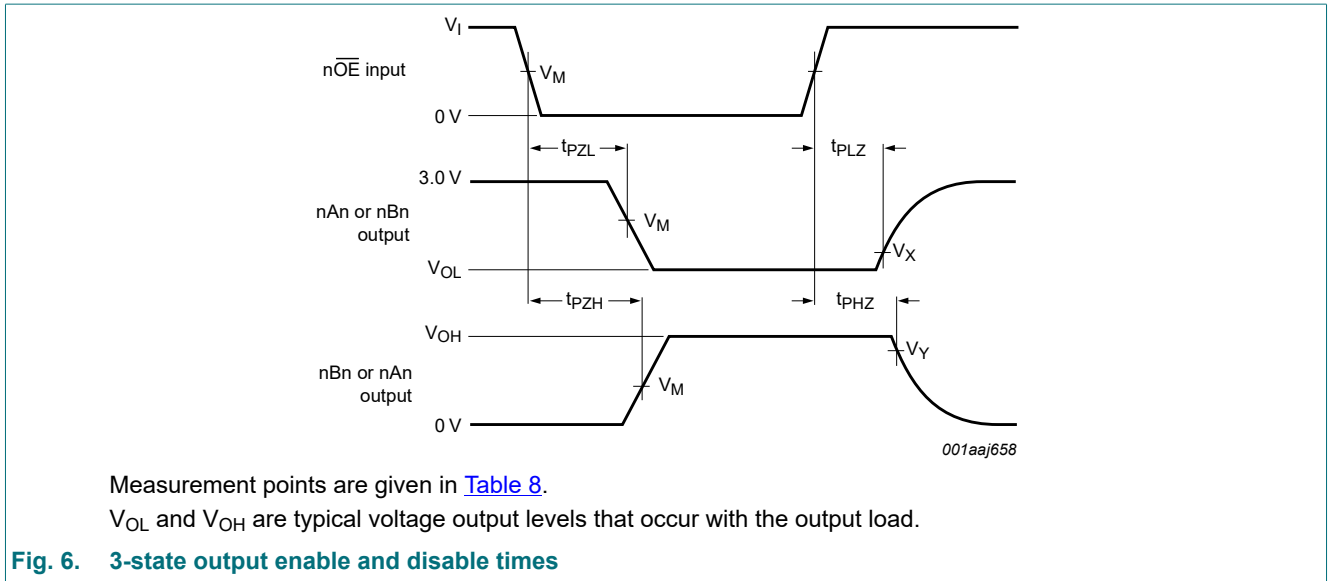


Table 8. Measurement points

| Input | | Output | | |
|-------|-------|--------|------------------|------------------|
| V_I | V_M | V_M | V_X | V_Y |
| 2.7 V | 1.5 V | 1.5 V | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |

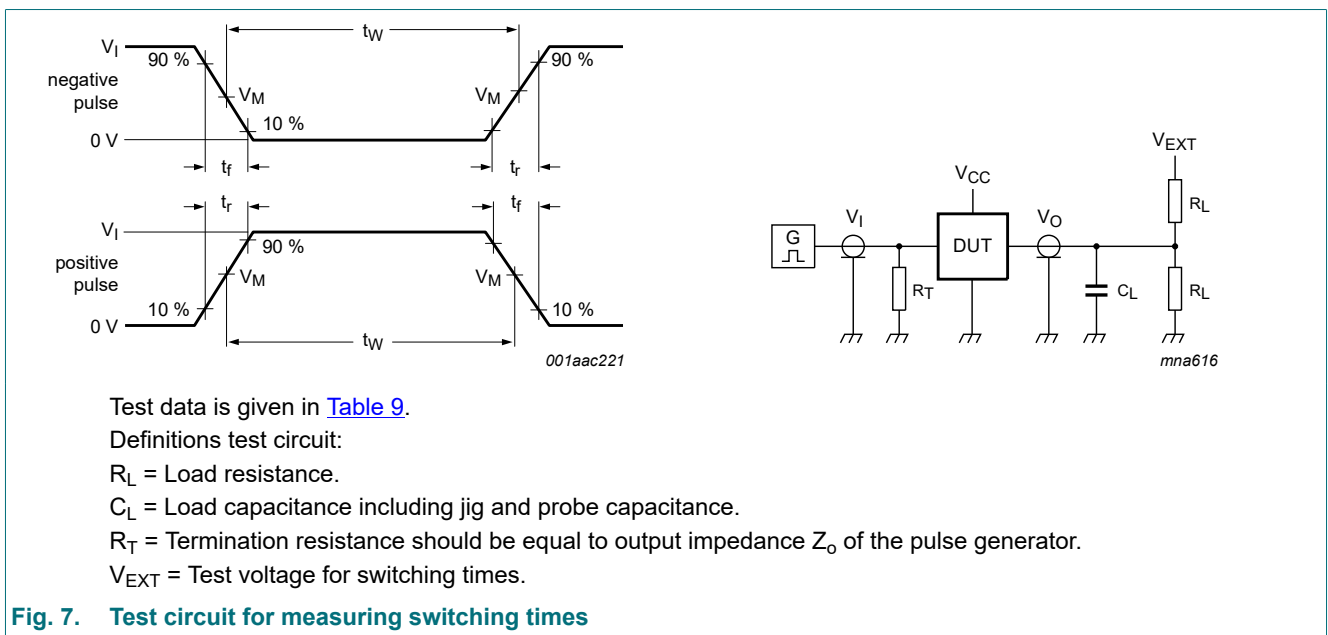


Table 9. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|-----------------------|--------|-----------------------|-------|-------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 2.7 V | $\leq 10 \text{ MHz}$ | 500 ns | $\leq 2.5 \text{ ns}$ | 50 pF | 500 Ω | GND | 6 V | open |

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

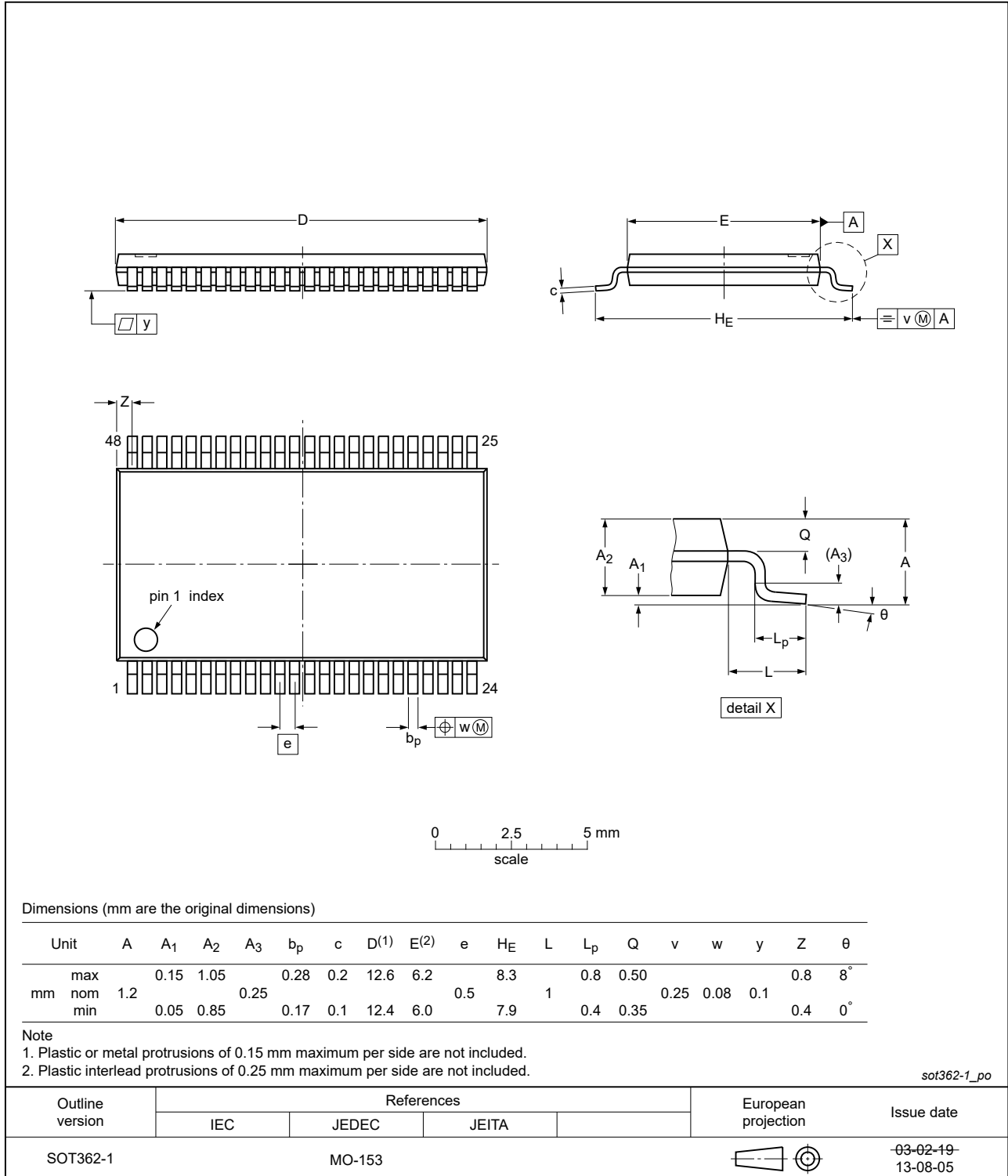


Fig. 8. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|---|-----------------------|---------------|------------------|
| 74LVT162245B v.4 | 20210806 | Product data sheet | - | 74LVT162245B v.3 |
| Modifications: | <ul style="list-style-type: none"> Type number 74LVT162245BDL (SOT370-1/SSOP48) removed. Section 1 and Section 2 updated. | | | |
| 74LVT162245B v.3 | 20181001 | Product data sheet | - | 74LVT162245B v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74LVT162245B v.2 | 19980219 | Product specification | - | 74LVT162245B v.1 |
| 74LVT162245B v.1 | 19950822 | Product specification | - | - |

14. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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