

# 74LVC162245A; 74LVCH162245A

16-bit transceiver with direction pin; 30  $\Omega$  series termination resistors; 5 V tolerant input/output; 3-state

Rev. 8 — 23 September 2021

Product data sheet

## 1. General description

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The 74LVC162245A; 74LVCH162245A is a 16-bit transceiver with 30  $\Omega$  termination resistors and 3-state outputs. The device can be used as two 8-bit transceivers or one 16-bit transceiver. The device features two output enables ( $1\overline{OE}$  and  $2\overline{OE}$ ) each controlling eight outputs, and two send/receive (1DIR and 2DIR) inputs for direction control. A HIGH on  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

The 74LVCH162245A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features and benefits

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- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Integrated 30  $\Omega$  termination resistors
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- All data inputs have bus hold (74LVCH162245A only)
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM ANSI/ESDA/Jedec JS-002 exceeds 1000 V
- Specified from -40  $^{\circ}\text{C}$  to +85  $^{\circ}\text{C}$  and from -40  $^{\circ}\text{C}$  to +125  $^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC162245ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH162245ADGG				
74LVC162245ADGV	-40 °C to +125 °C	TVSOP48	plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm	SOT480-1
74LVCH162245ADGV				

### 4. Functional diagram

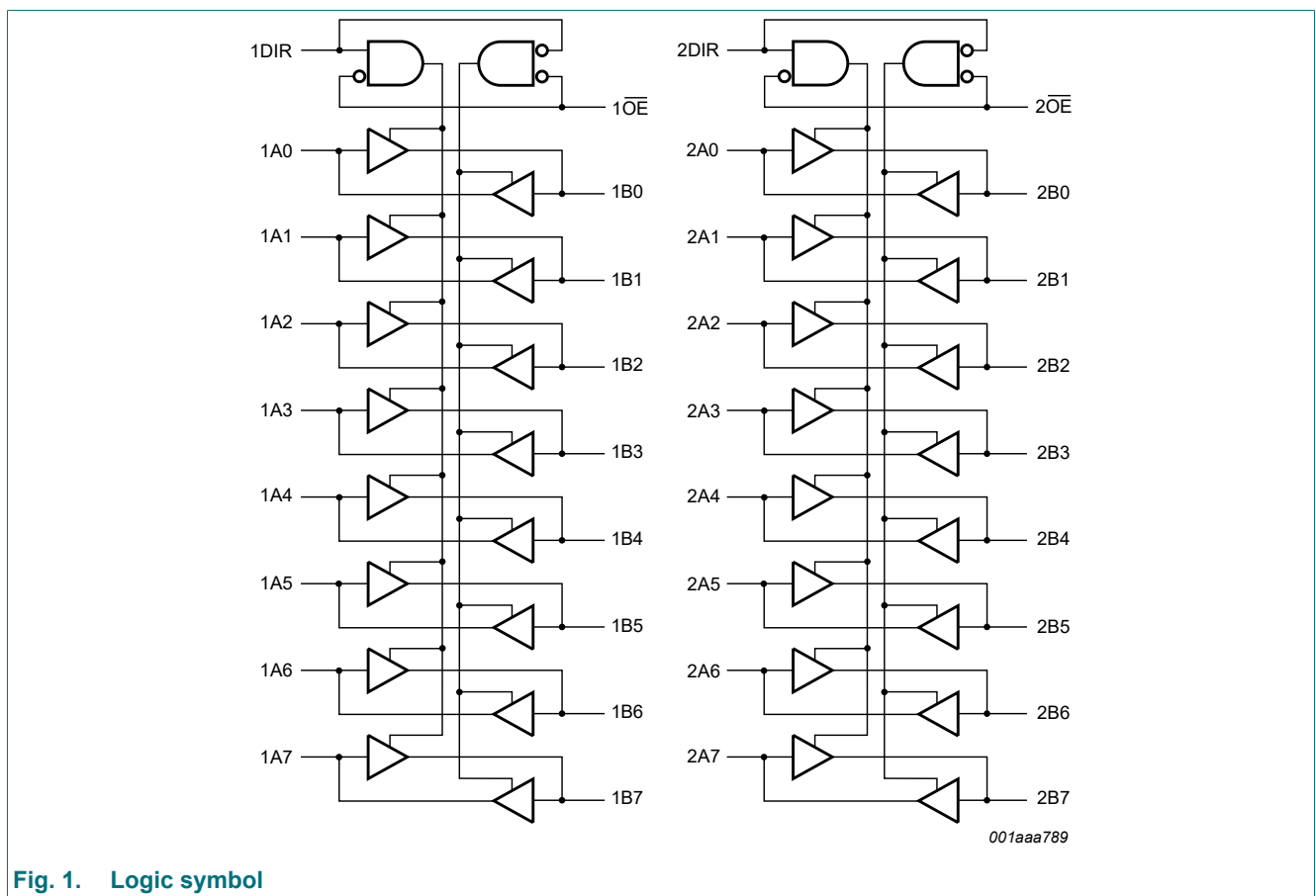


Fig. 1. Logic symbol

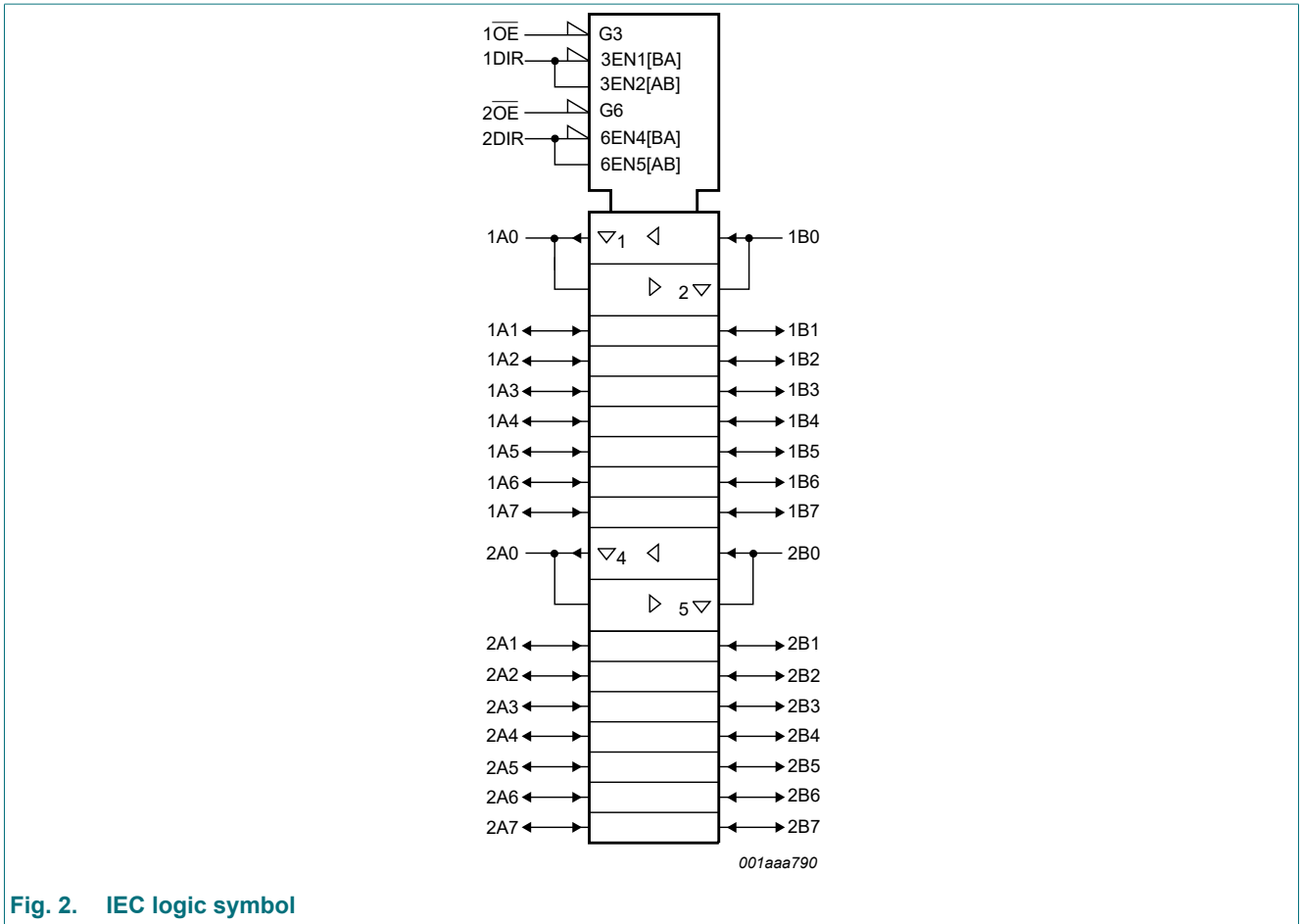


Fig. 2. IEC logic symbol

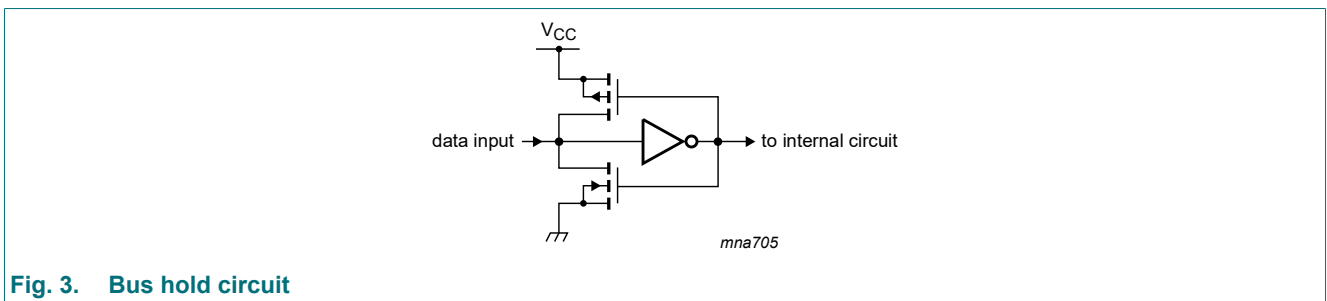


Fig. 3. Bus hold circuit

## 5. Pinning information

### 5.1. Pinning

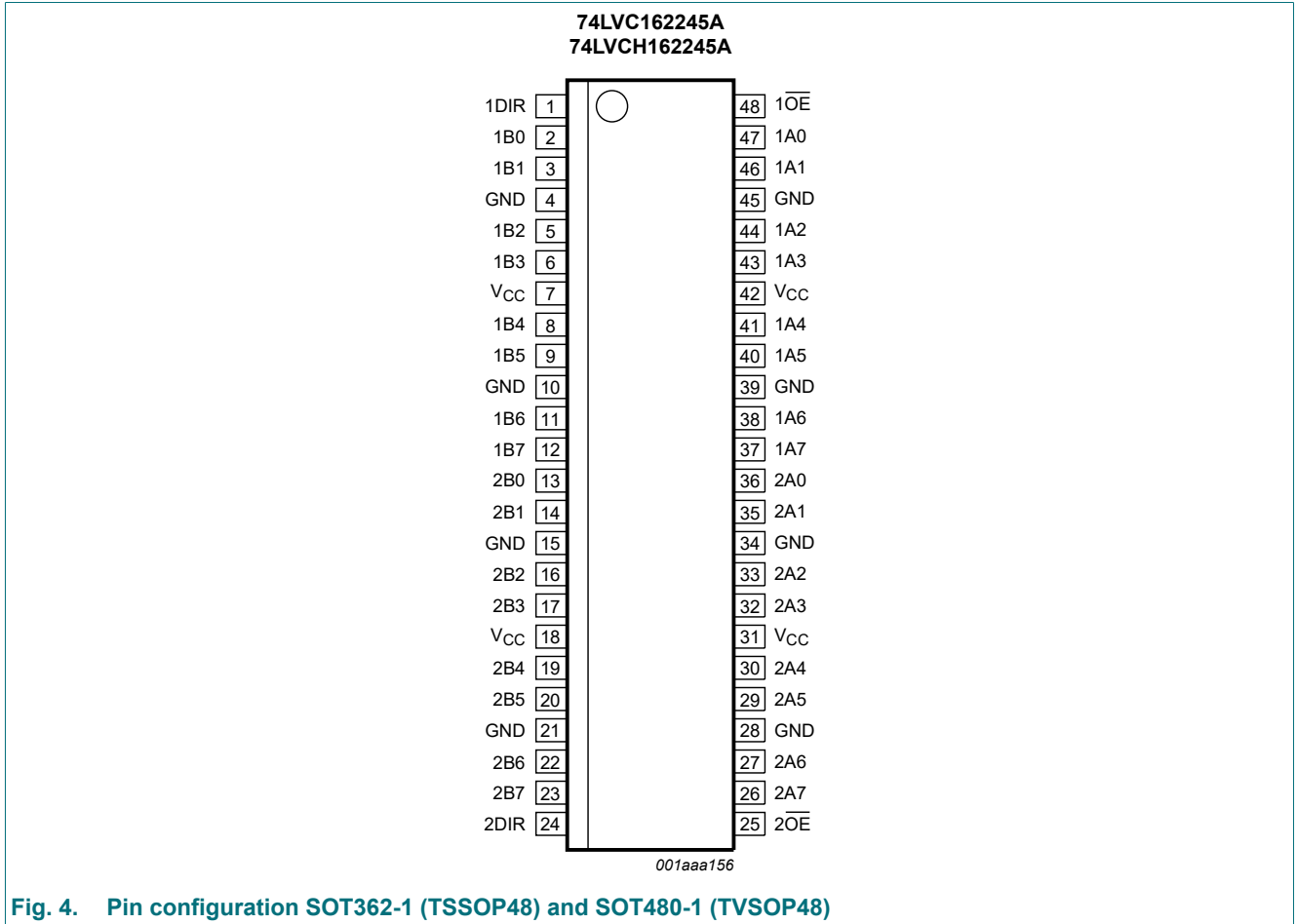


Fig. 4. Pin configuration SOT362-1 (TSSOP48) and SOT480-1 (TVSOP48)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1OE, 2OE	48, 25	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs		Outputs	
nOE	nDIR	nAn	nBn
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA	
V <sub>I</sub>	input voltage	[1]	-0.5	+6.5	V	
I <sub>OK</sub>	output clamping current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0 V	-	±50	mA	
V <sub>O</sub>	output voltage	output HIGH or LOW	[2]	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state	[2]	-0.5	+6.5	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA	
I <sub>CC</sub>	supply current		-	100	mA	
I <sub>GND</sub>	ground current		-100	-	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT362-1 (TSSOP48) packages: P<sub>tot</sub> derates linearly with 12.2 mW/K above 109 °C.  
For SOT480-1 (TVSOP48) packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.2 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -2 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 2 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V [2]	-	±0.1	±5	-	±20	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V [2][3]	-	±0.1	±5	-	±20	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 0.0 V	-	±0.1	±10	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.6 V	-	0.1	20	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.7 V to 3.6 V	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	10	-	-	-	pF
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 1.65; V <sub>I</sub> = 0.58 V [4][5]	10	-	-	10	-	μA
		V <sub>CC</sub> = 2.3; V <sub>I</sub> = 0.7 V	30	-	-	25	-	μA
		V <sub>CC</sub> = 3.0; V <sub>I</sub> = 0.8 V	75	-	-	60	-	μA

16-bit transceiver with direction pin; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 1.65; V <sub>I</sub> = 1.07 V [4][5]	-10	-	-	-10	-	μA
		V <sub>CC</sub> = 2.3; V <sub>I</sub> = 1.7 V	-30	-	-	-25	-	μA
		V <sub>CC</sub> = 3.0; V <sub>I</sub> = 2.0 V	-75	-	-	-60	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 1.95 V [4][6]	200	-	-	200	-	μA
		V <sub>CC</sub> = 2.7 V	300	-	-	300	-	μA
		V <sub>CC</sub> = 3.6 V	500	-	-	500	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 1.95 V [4][6]	-200	-	-	-200	-	μA
		V <sub>CC</sub> = 2.7 V	-300	-	-	-300	-	μA
		V <sub>CC</sub> = 3.6 V	-500	-	-	-500	-	μA

- [1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.
- [2] The bus hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.
- [3] For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.
- [4] Valid for data inputs of bus hold parts only (74LVCH162245A). Note that control inputs do not have a bus hold circuit.
- [5] The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
- [6] The specified overdrive current at the data input forces the data input to the opposite input state.

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn to nBn; nBn to nAn; see Fig. 5 [2]						
		V <sub>CC</sub> = 1.2 V	-	12	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	6.6	16.0	1.5	18.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.5	7.8	1.0	9.1	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.5	6.7	1.0	9.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.9	5.7	1.0	8.5	ns
t <sub>en</sub>	enable time	nOE to nAn, nBn; see Fig. 6 [2]						
		V <sub>CC</sub> = 1.2 V	-	18	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	7.7	17.2	2.0	19.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	4.3	9.4	1.5	10.9	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.6	8.5	1.5	9.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.5	7.5	1.0	7.5	ns
t <sub>dis</sub>	disable time	nOE to nAn, nBn; see Fig. 6 [2]						
		V <sub>CC</sub> = 1.2 V	-	10	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.8	4.6	11.0	2.8	12.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.6	6.3	1.0	7.3	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.4	7.5	1.5	11.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	3.2	6.5	1.5	8.5	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub> [3]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	10.4	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	14.0	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	17.2	-	-	-	pF

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in Volts  
 N = number of inputs switching  
 Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

### 10.1. Waveforms and test circuit

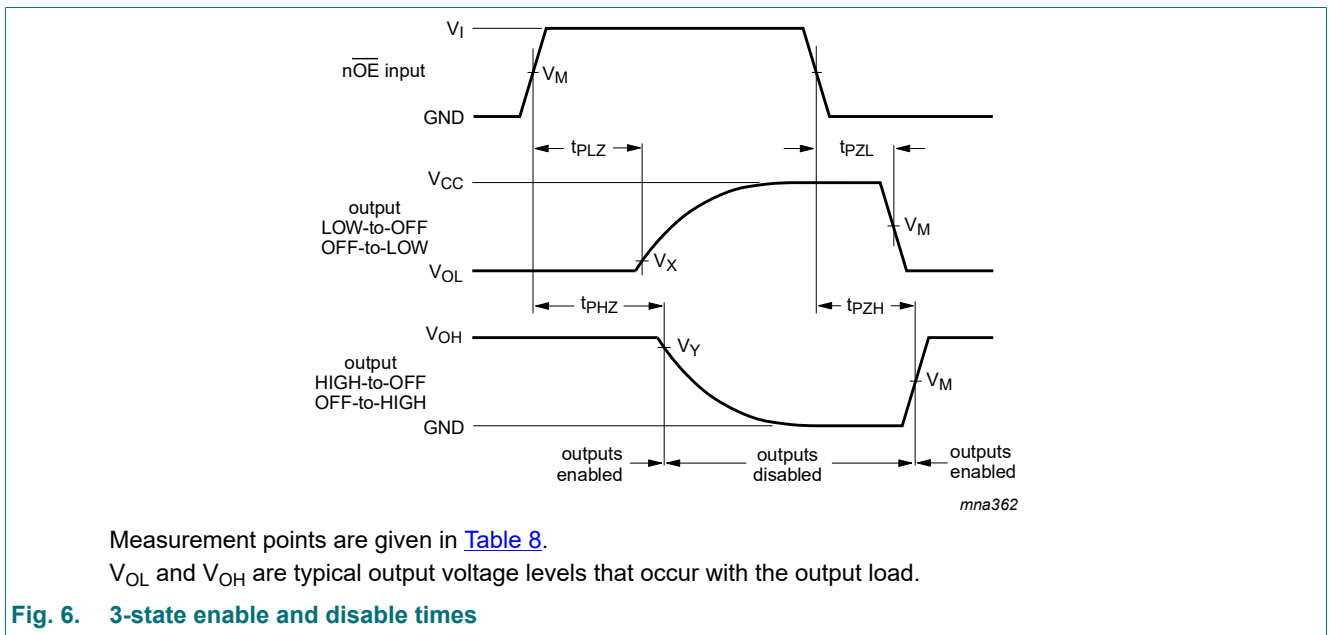
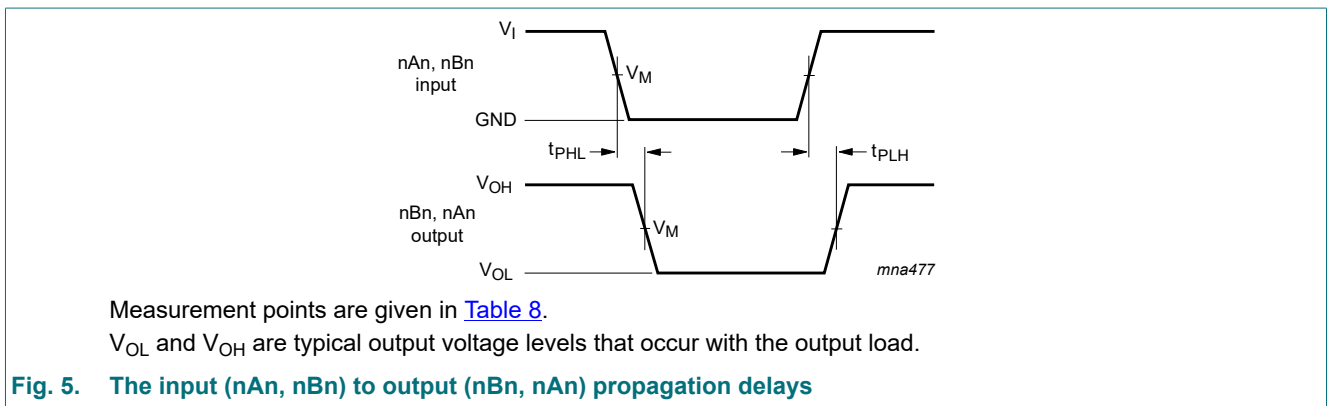
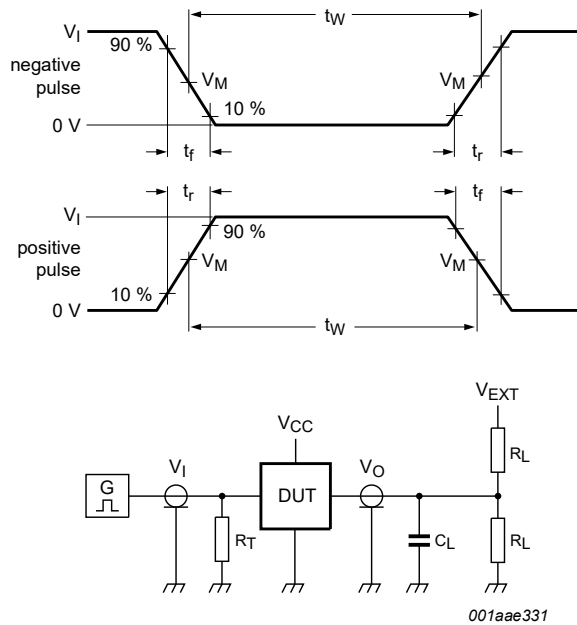




Table 8. Measurement points

Supply voltage	Input		Output		
V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
1.65 V to 1.95 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.7 V	1.5 V	2.7 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
1.2 V	V <sub>CC</sub>	≤ 2 ns	30 pF	1 kΩ	open	2 × V <sub>CC</sub>	GND
1.65 V to 1.95 V	V <sub>CC</sub>	≤ 2 ns	30 pF	1 kΩ	open	2 × V <sub>CC</sub>	GND
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2 ns	30 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND

### 11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

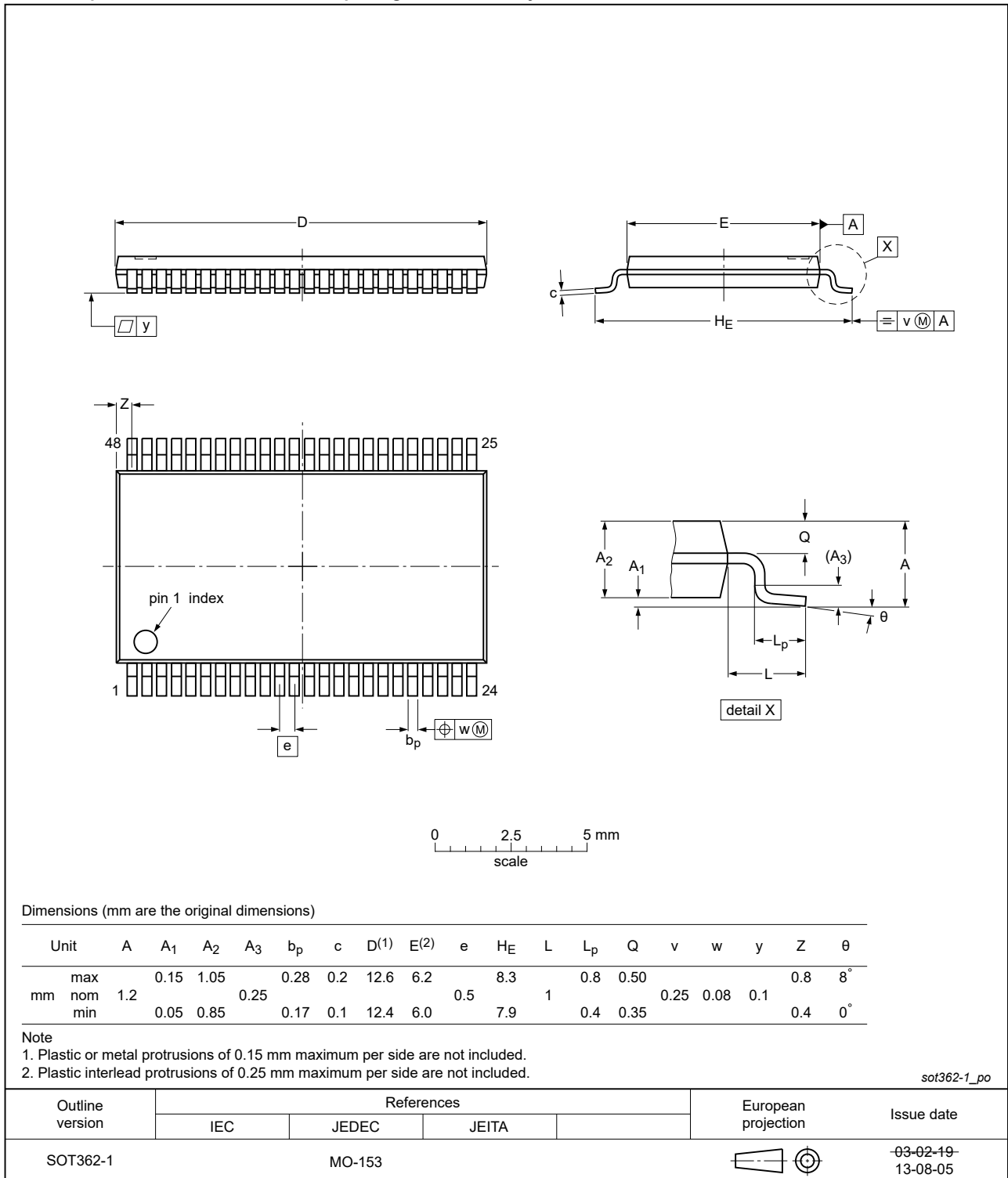


Fig. 8. Package outline SOT362-1 (TSSOP48)

TVSOP48: plastic thin shrink small outline package; 48 leads;  
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1

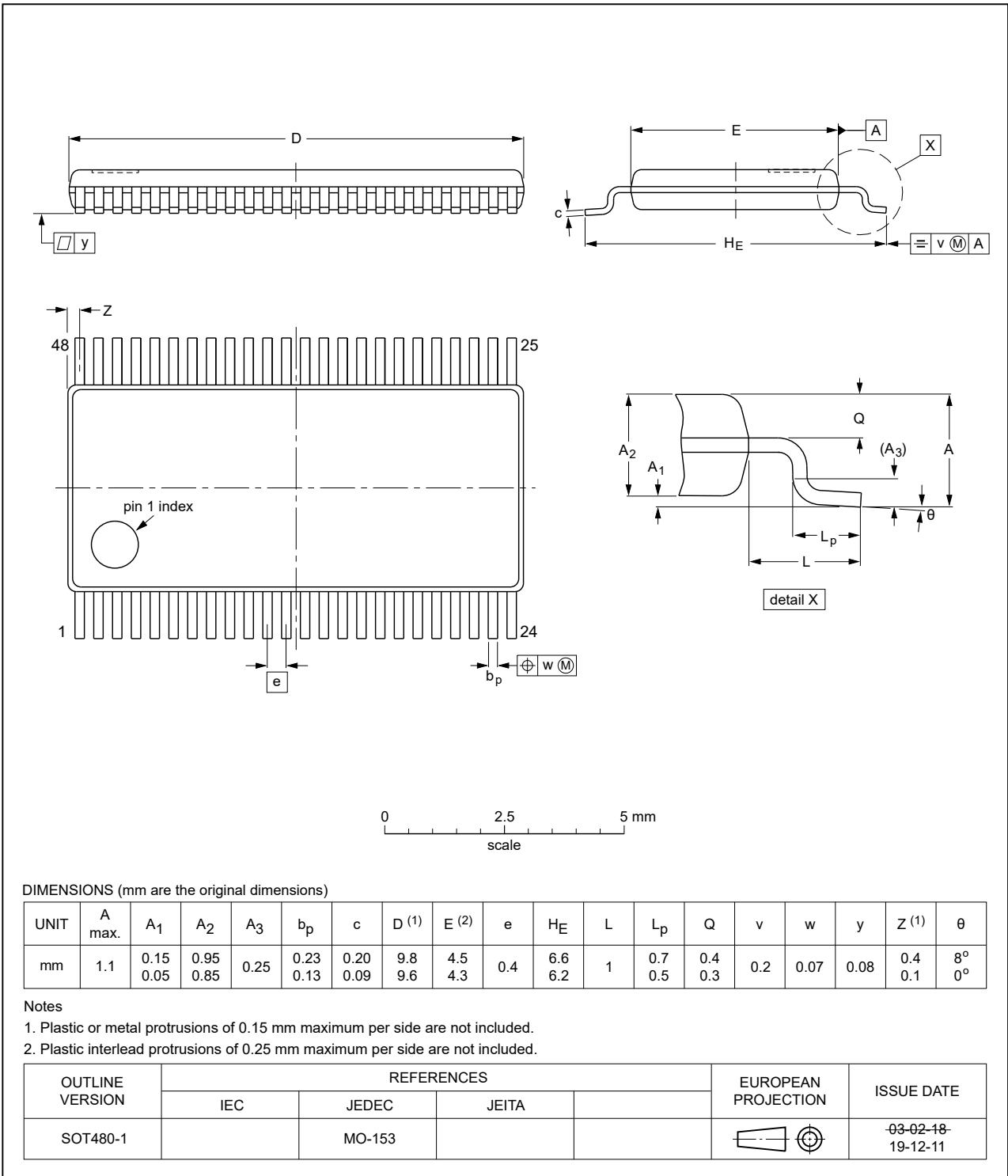


Fig. 9. Package outline SOT480-1 (TVSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH162245A v.8	20210923	Product data sheet	-	74LVC_LVCH162245A v.7
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74LVC162245ADL and 74LVCH162245ADL (SOT370-1/SSOP48) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for P<sub>tot</sub> total power dissipation updated.</li> </ul>			
74LVC_LVCH162245A v.7	20190211	Product data sheet	-	74LVC_LVCH162245A v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74LVC162245ADGV and 74LVCH162245ADGV (SOT480-1) added.</li> <li>Package outline drawing <a href="#">Fig. 8</a> (TVSOP48) updated.</li> </ul>			
74LVC_LVCH162245A v.6	20111123	Product data sheet	-	74LVC_LVCH162245A v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC_LVCH162245A v.5	20031208	Product specification	-	74LVC_H162245A v.4
74LVC_H162245A v.4	19980217	Product specification	-	74LVC162245A_74LVCH162245A v.3
74LVC162245A_74LVCH162245A v.3	19980217	Product specification	-	74LVC162245A v.2
74LVC162245A v.2	19970801	Product specification	-	74LVC162245A v.1
74LVC162245A v.1	19960108	-	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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