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Kind regards,

Team Nexperia

# PHB47NQ10T

## N-channel TrenchMOS standard level FET

Rev. 02 — 25 February 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- DC-to-DC convertors
- Switched-mode power supplies

### 1.4 Quick reference data

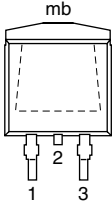
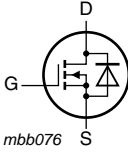
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> and <a href="#">2</a>	-	-	47	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 3</a>	-	-	166	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 40\text{ A};$ $V_{DS} = 80\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 13</a>	-	21	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 11</a> and <a href="#">12</a>	-	20	28	m $\Omega$



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT404 (D2PAK)</p>	
2	D	drain <a href="#">[1]</a>		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

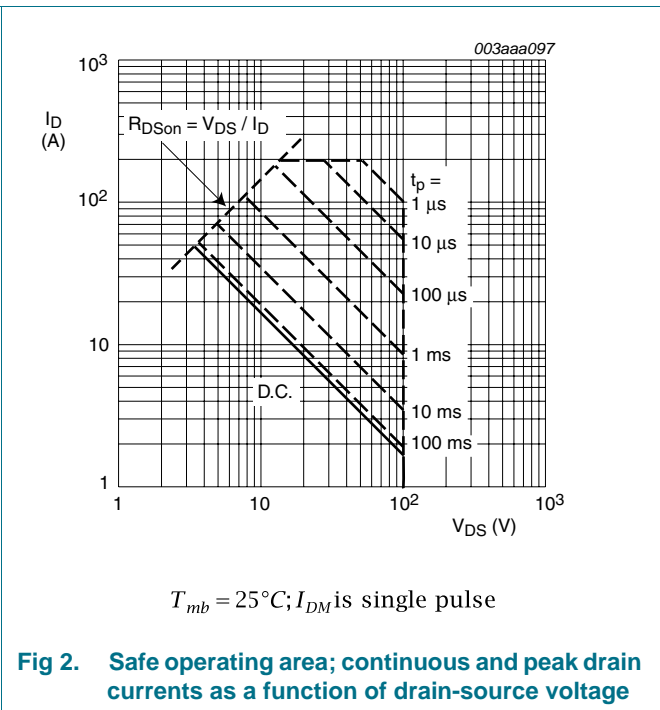
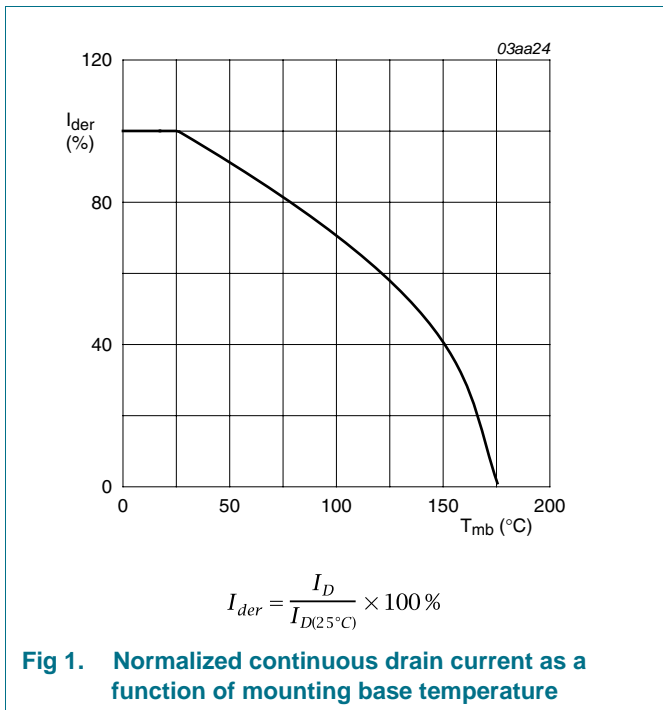
Type number	Package		Version
	Name	Description	
PHB47NQ10T	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

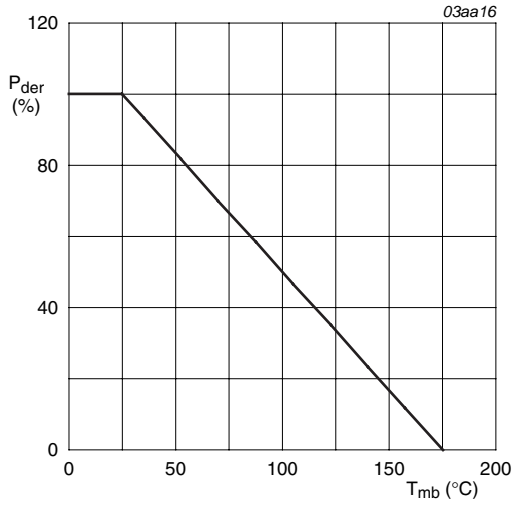
### 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

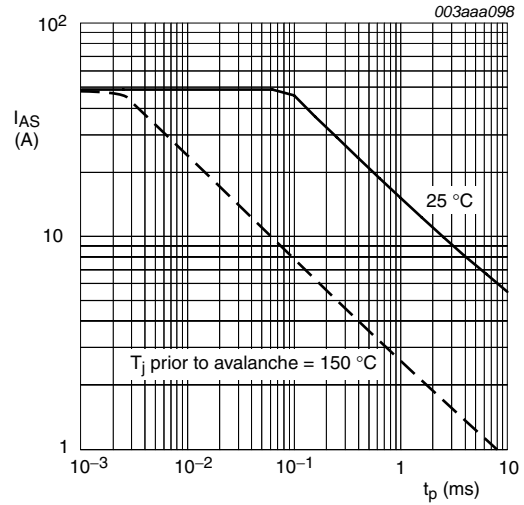
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	100	V
V <sub>DGR</sub>	drain-gate voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	100	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>	-	33	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a> and <a href="#">2</a>	-	47	A
I <sub>DM</sub>	peak drain current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	187	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 3</a>	-	166	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	47	A
I <sub>SM</sub>	peak source current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C	-	187	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 30 A; V <sub>sup</sub> ≤ 25 V; unclamped; t <sub>p</sub> = 0.1 ms; R <sub>GS</sub> = 50 Ω; see <a href="#">Figure 4</a>	-	45	mJ





$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 3. Normalized total power dissipation as a function of mounting base temperature



Unclamped inductive load;  $V_{DD} \leq 25V$ ;  
 $R_{GS} = 50\Omega$ ;  $V_{GS} = 5V$ ; starting at  $T_j = 25^{\circ}C$  and  $150^{\circ}C$ .

Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	-	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board; minimum footprint	-	50	-	K/W

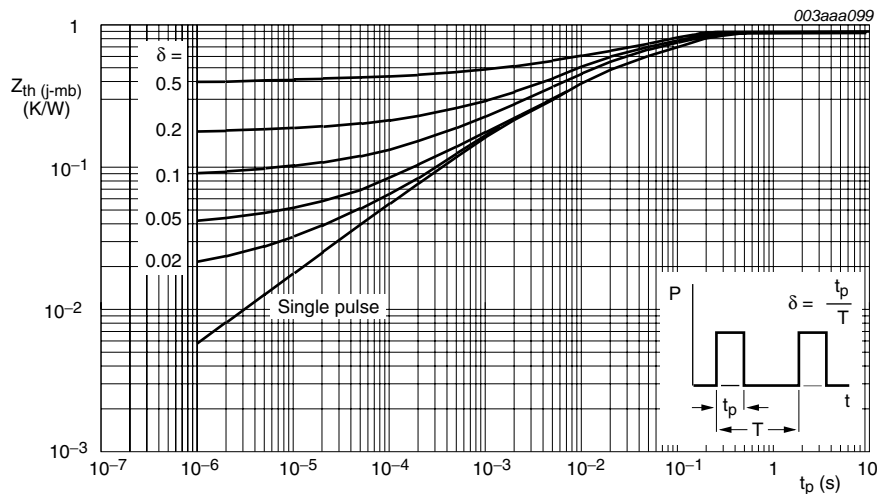
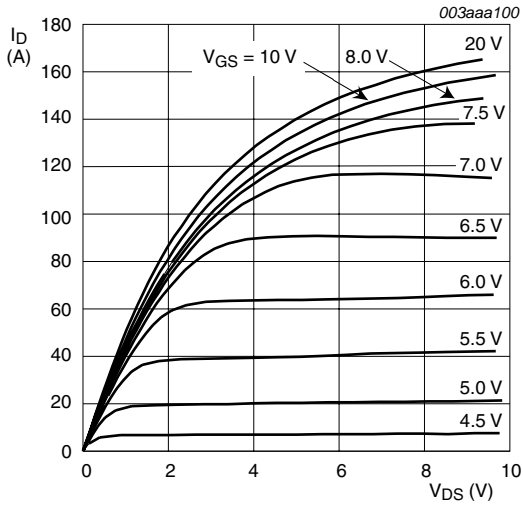


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

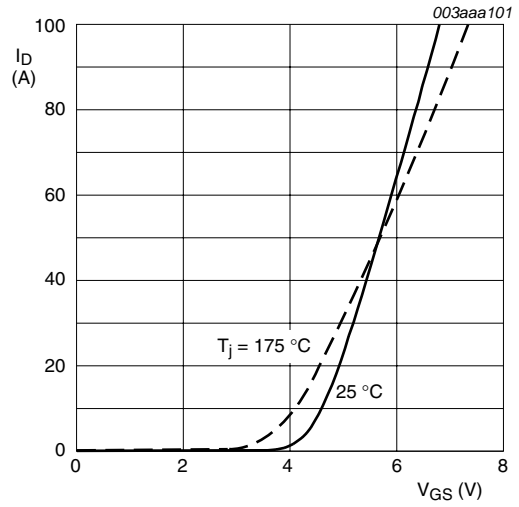
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 10</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	-	76	m $\Omega$
		$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	20	28	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 40 \text{ A}$ ; $V_{DS} = 80 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a>	-	66	-	nC
$Q_{GS}$	gate-source charge		-	12	-	nC
$Q_{GD}$	gate-drain charge		-	21	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 14</a>	-	2320	3100	pF
$C_{oss}$	output capacitance		-	315	378	pF
$C_{rSS}$	reverse transfer capacitance		-	187	256	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}$ ; $R_L = 1.2 \text{ } \Omega$ ; $V_{GS} = 10 \text{ V}$ ; $R_{G(ext)} = 10 \text{ } \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	15	23	ns
$t_r$	rise time		-	70	105	ns
$t_{d(off)}$	turn-off delay time		-	83	116	ns
$t_f$	fall time		-	45	63	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 47 \text{ A}$ ; $di_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = -10 \text{ V}$ ; $V_{DS} = 30 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	66	-	ns
$Q_r$	recovered charge		-	0.24	-	$\mu\text{C}$



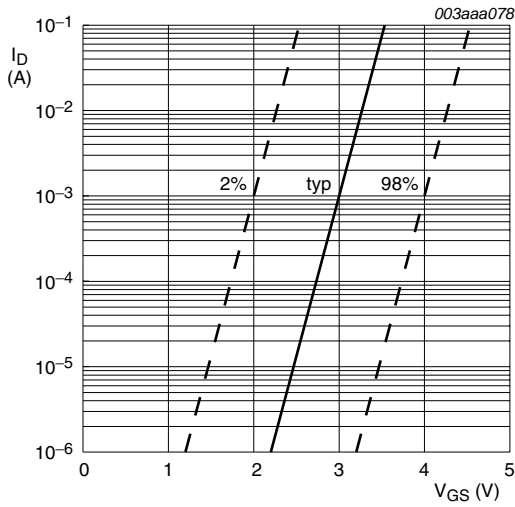
$T_j = 25^\circ\text{C}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



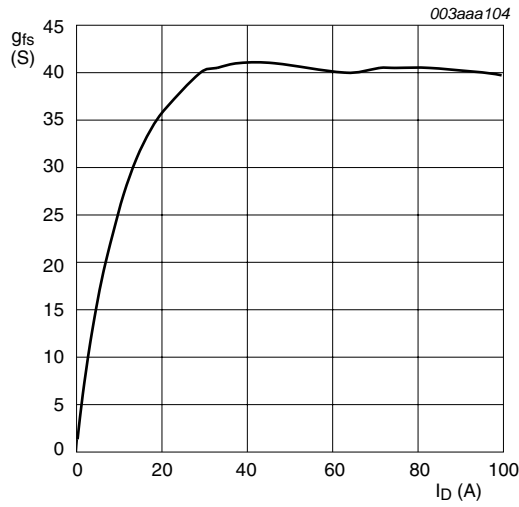
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



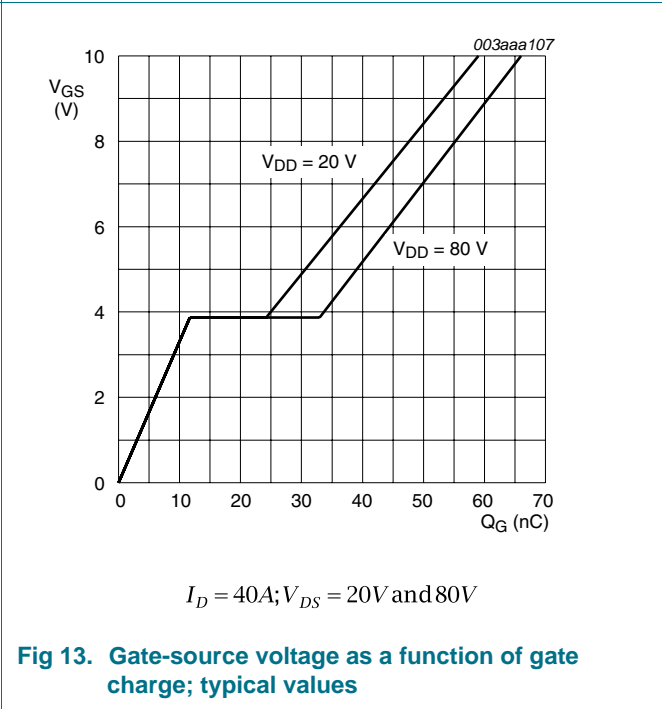
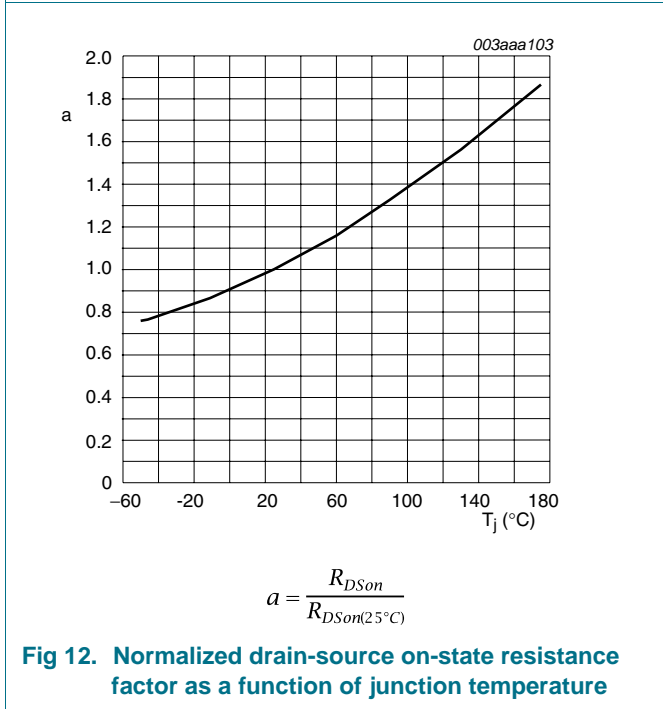
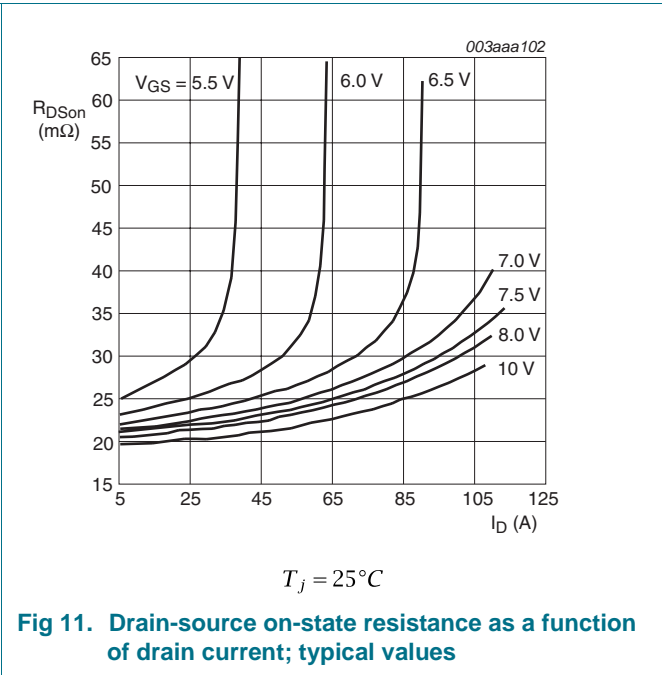
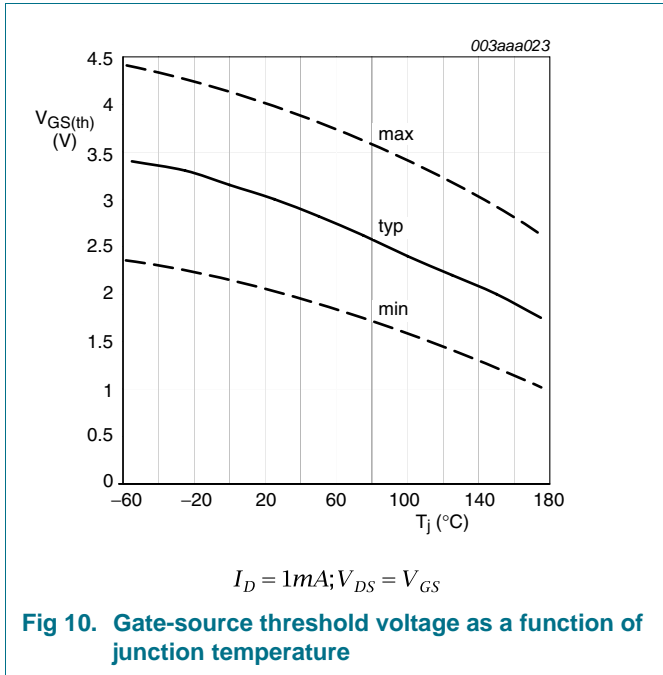
$T_j = 25^\circ\text{C}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage

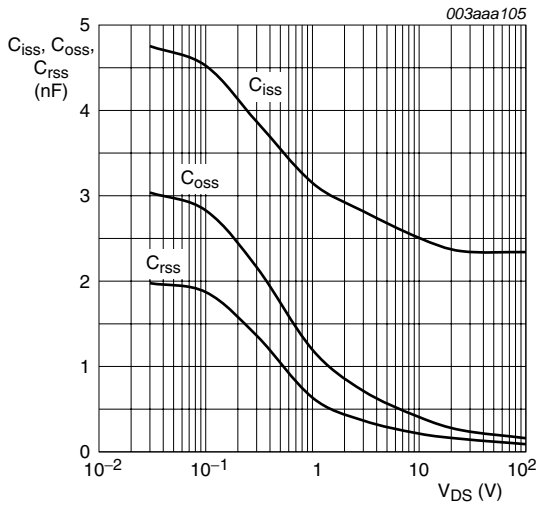


$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 9. Forward transconductance as a function of drain current; typical values

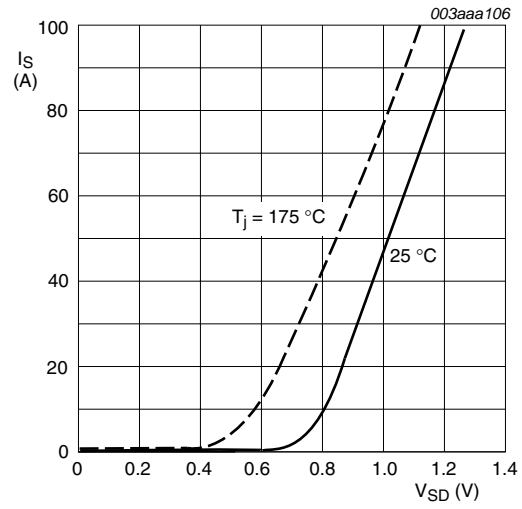






$V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ C$  and  $175^\circ C; V_{GS} = 0V$

Fig 15. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

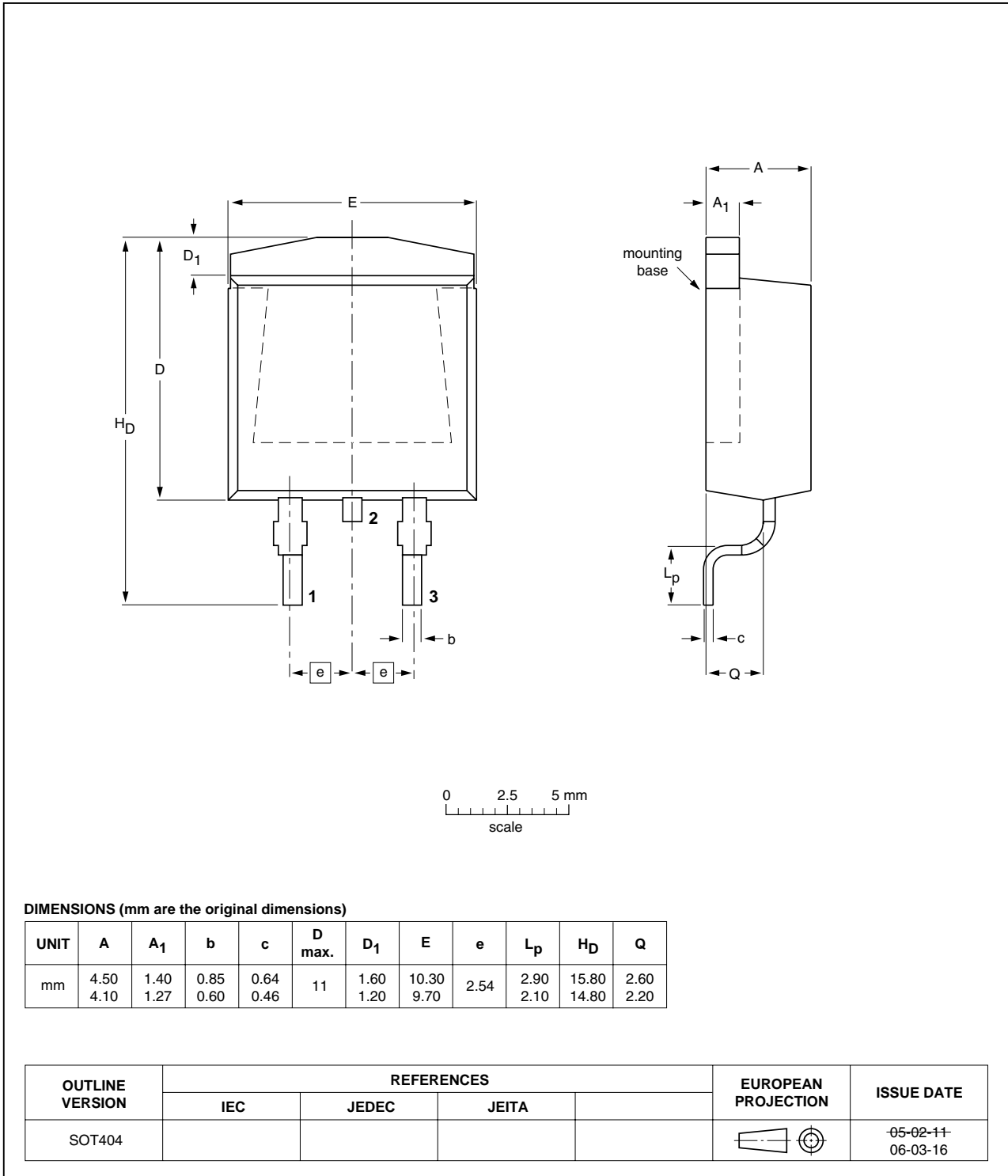


Fig 16. Package outline SOT404 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHB47NQ10T_2	20100225	Product data sheet	-	PHP_PHB_47NQ10T-01
Modifications:		<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>		
PHP_PHB_47NQ10T-01 (9397 750 08243)	20010516	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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