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# FQB19N20C

## N-Channel QFET® MOSFET

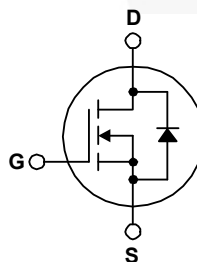
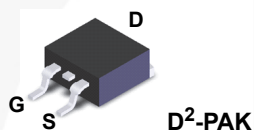
200 V, 19 A, 170 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 19.0 A, 200 V,  $R_{DS(on)} = 170 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 9.5 \text{ A}$
- Low Gate Charge (Typ. 40.5 nC)
- Low  $C_{rss}$  (Typ. 85 pF)
- 100% Avalanche Tested
- RoHS Compliant



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQB19N20CTM	Unit
$V_{DSS}$	Drain-Source Voltage	200	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	19.0	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	12.1	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	76.0	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	433	mJ
$I_{AR}$	Avalanche Current (Note 1)	19.0	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	13.9	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ )*	3.13	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	139	W
	- Derate above $25^\circ\text{C}$	1.11	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQB19N20CTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	40	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB19N20C	FQB19N20CTM	D <sup>2</sup> -PAK	330 mm	24 mm	800 units

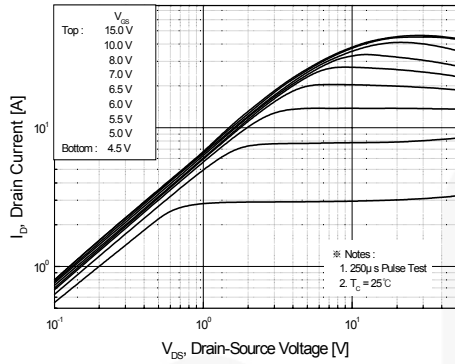
## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	200	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.24	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V	--	--	10	μA
		V <sub>DS</sub> = 160 V, T <sub>C</sub> = 125°C	--	--	100	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9.5 A	--	0.14	0.17	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 9.5 A	--	10.8	--	S
<b>Dynamic Characteristics</b>						
C <sub>iSS</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	830	1080	pF
C <sub>oss</sub>	Output Capacitance		--	195	255	pF
C <sub>rSS</sub>	Reverse Transfer Capacitance		--	85	110	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 19.0 A R <sub>G</sub> = 25 Ω	--	10	40	ns
t <sub>r</sub>	Turn-On Rise Time		--	150	310	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	135	280	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	--	115	240
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 160 V, I <sub>D</sub> = 19.0 A V <sub>GS</sub> = 10 V	--	40.5	53	nC
Q <sub>gs</sub>	Gate-Source Charge		--	6.0	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	22.5	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	19.0	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	76.0	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 19.0 A	--	--	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 19.0 A di <sub>F</sub> /dt = 100 A/μs	--	208	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	1.63	--	μC

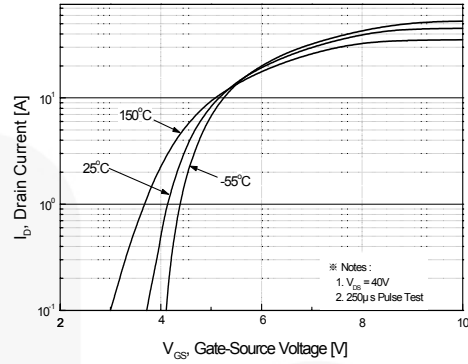
### Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 1.8 mH, I<sub>AS</sub> = 19.0 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 19.0 A, di/dt ≤ 300 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature.

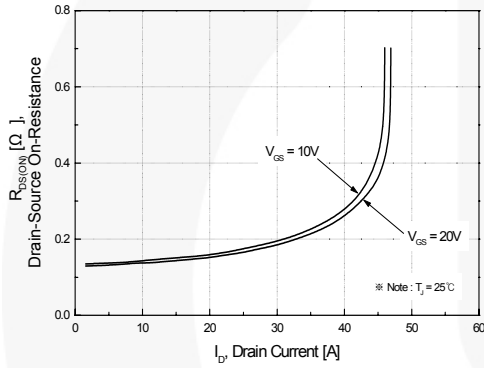
## Typical Characteristics



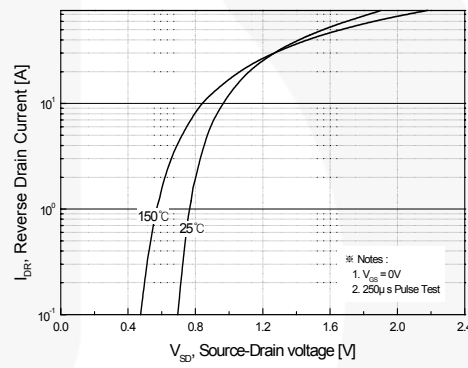
**Figure 1. On-Region Characteristics**



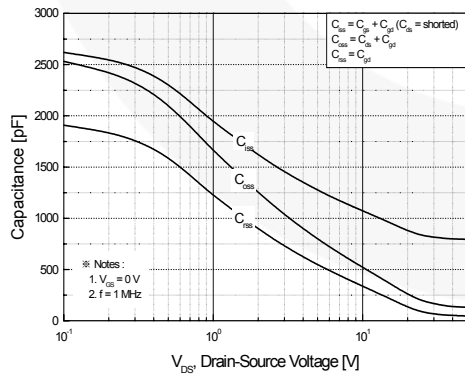
**Figure 2. Transfer Characteristics**



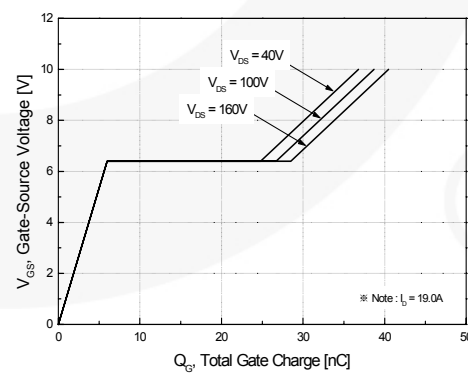
**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

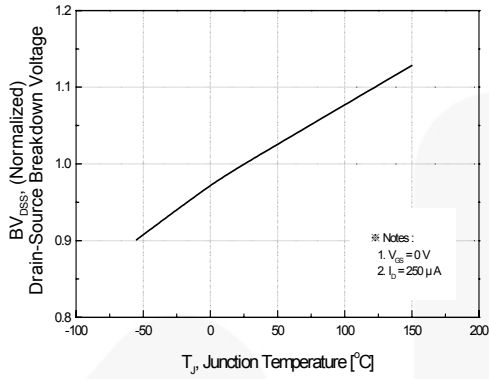


**Figure 5. Capacitance Characteristics**

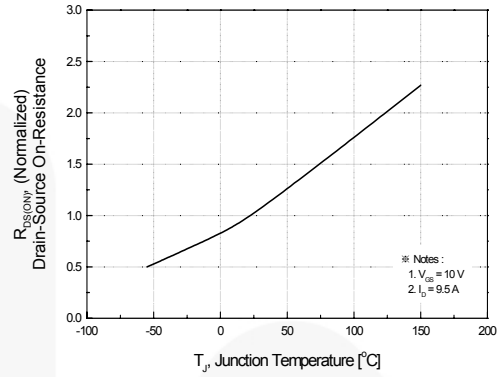


**Figure 6. Gate Charge Characteristics**

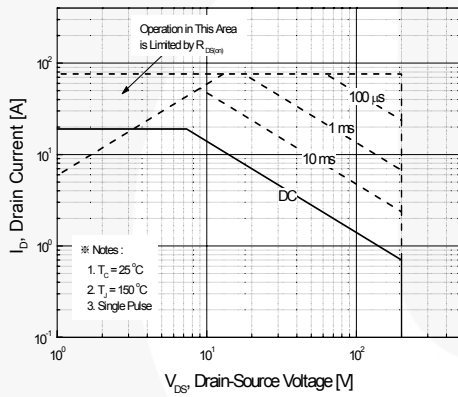
## Typical Characteristics (Continued)



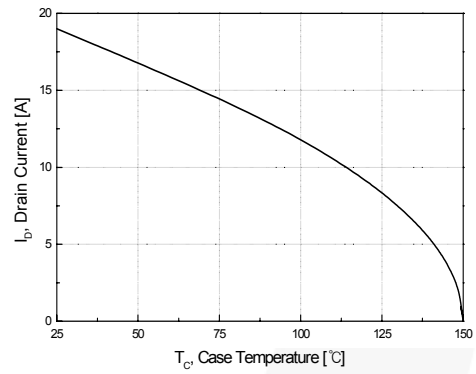
**Figure 7. Breakdown Voltage Variation vs Temperature**



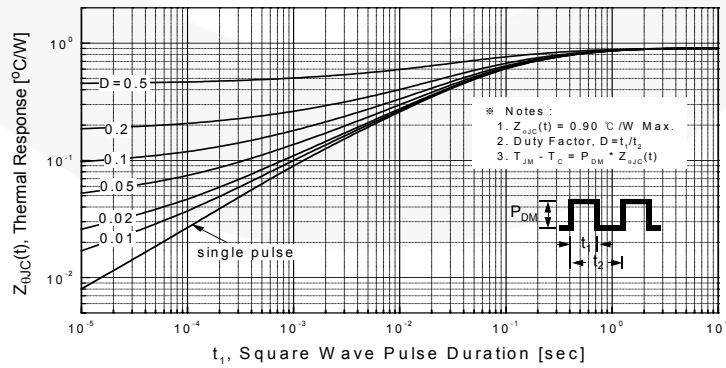
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs Case Temperature**



**Figure 11. Transient Thermal Response Curve**

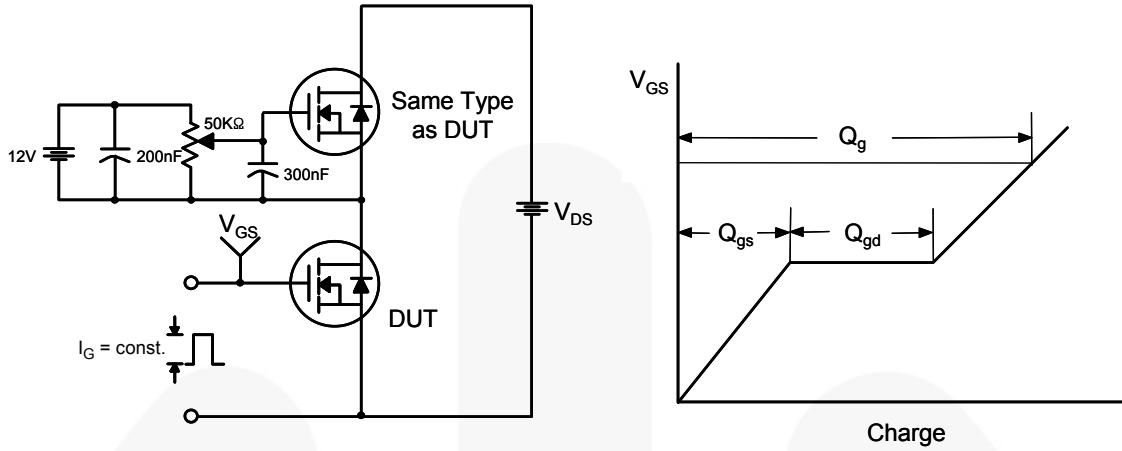


Figure 12. Gate Charge Test Circuit & Waveform

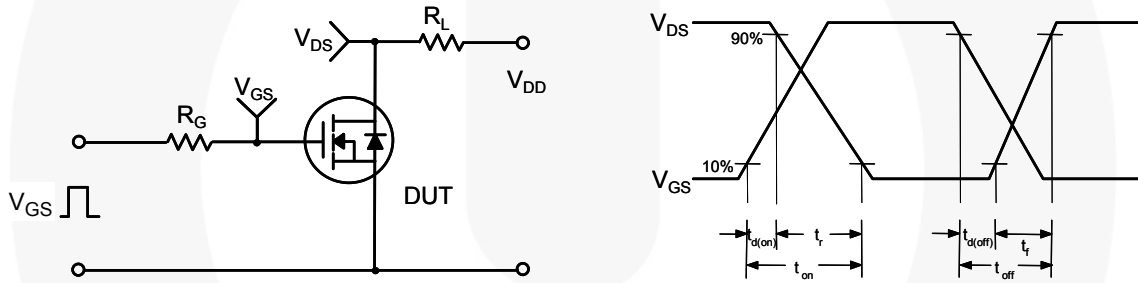


Figure 13. Resistive Switching Test Circuit & Waveforms

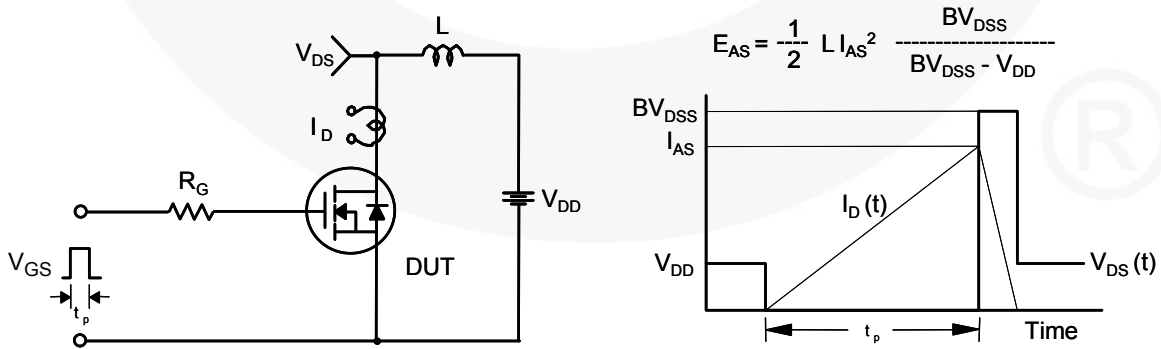
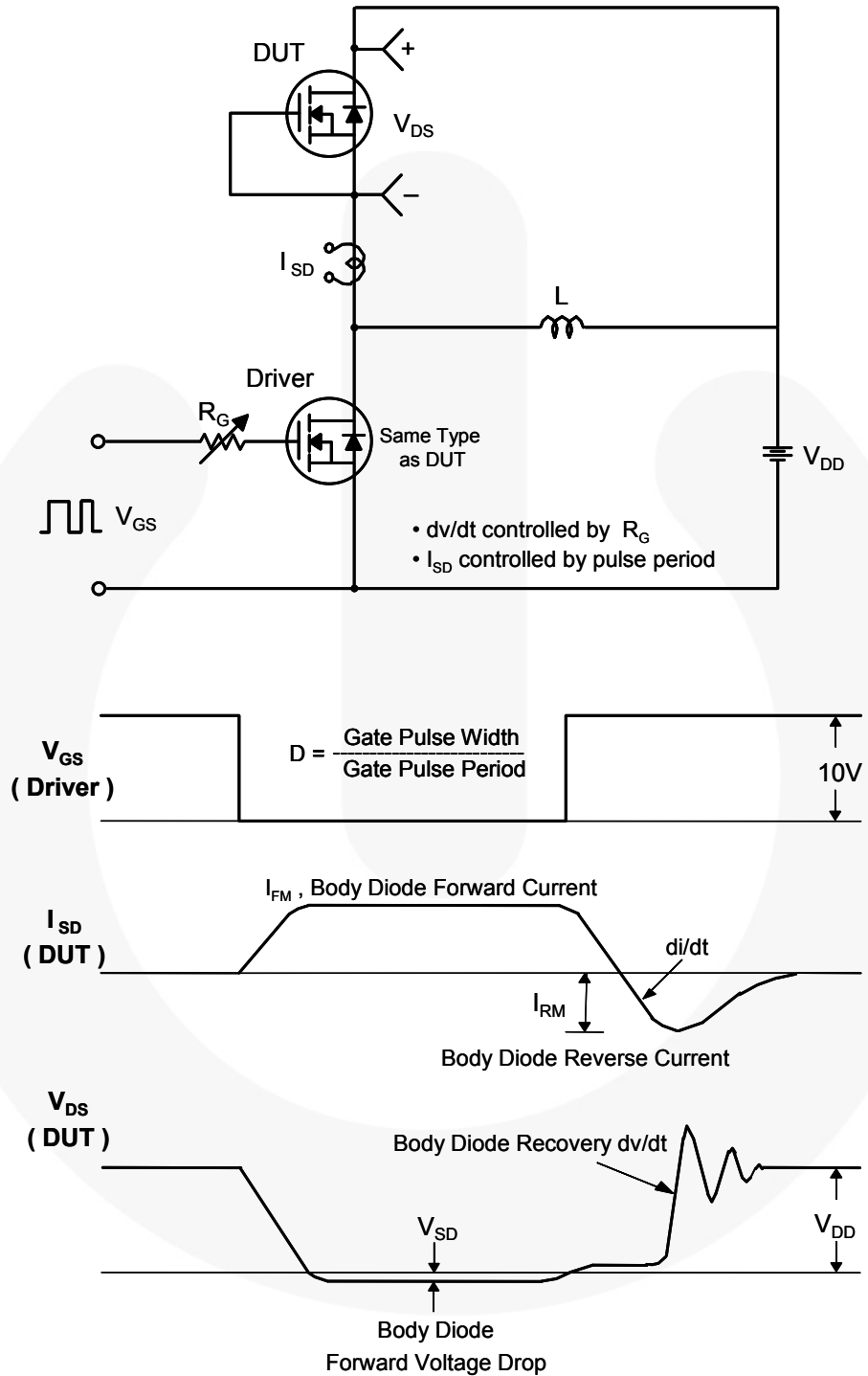
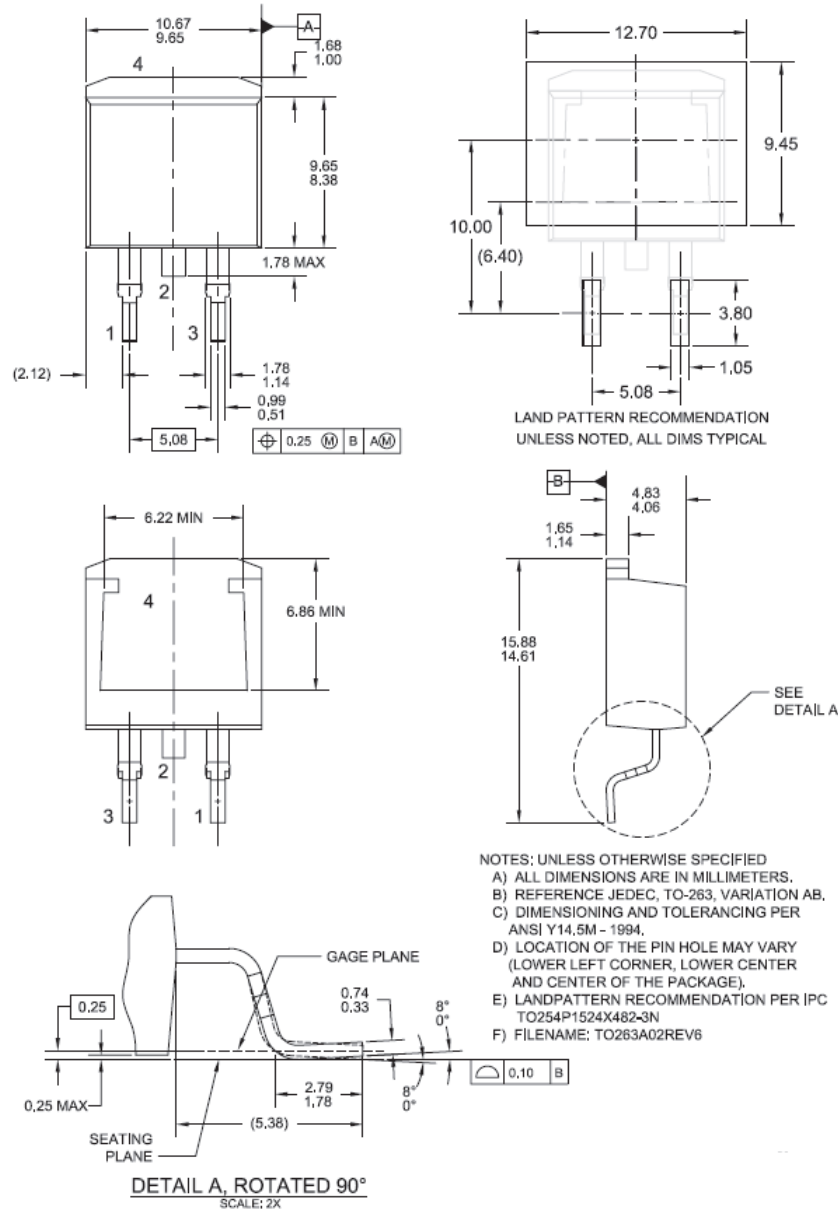


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



**Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms**

## Mechanical Dimensions



**Figure 16. TO263 (D<sup>2</sup>PAK), Molded, 2-Lead, Surface Mount**

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