

FDBL9401L-F085

N-Channel Logic Level PowerTrench[®] MOSFET

40 V, 300 A, 0.55 mΩ

Features

- Typical $R_{DS(on)}$ = 0.47 mΩ at $V_{GS} = 10$ V, $I_D = 80$ A
- Typical $Q_{g(tot)}$ = 269 nC at $V_{GS} = 10$ V, $I_D = 80$ A
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current – Continuous, ($V_{GS} = 10$ V) $T_C = 25^\circ\text{C}$ (Note 1)	300	A
	Pulsed Drain Current, $T_C = 25^\circ\text{C}$	(See Figure 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	913	mJ
P_D	Power Dissipation	429	W
	Derate Above 25°C	2.86	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

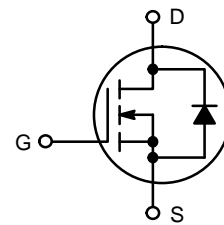
1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 530 \mu\text{H}$, $I_{AS} = 64$ A, $V_{DD} = 40$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.



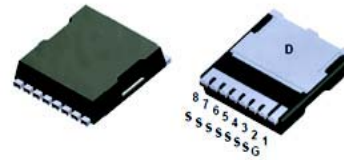
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V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
40 V	0.55 mΩ @ 10 V	300 A

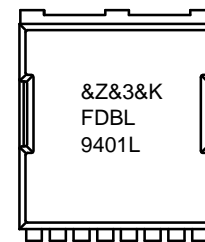


N-CHANNEL MOSFET



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 FDBL9401L = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

FDBL9401L–F085

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3)	43	

3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40	–	–	V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 40 V, V_{GS} = 0 V$ $T_J = 25^\circ C$ $T_J = 175^\circ C$ (Note 4)	–	–	1 2000	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 V$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.7	3	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 4.5 V, I_D = 80 A$	–	0.59	0.76	m Ω
		$V_{GS} = 10 V, I_D = 80 A$ $T_J = 25^\circ C$ $T_J = 175^\circ C$ (Note 4)	–	0.47 0.81	0.55 0.97	m Ω

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz$	–	19550	–	pF
C_{oss}	Output Capacitance		–	5630	–	pF
C_{rss}	Reverse Transfer Capacitance		–	509	–	pF
R_g	Gate Resistance	$V_{GS} = 0.5 V, f = 1 MHz$	–	2.8	–	Ω
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{GS} = 0 V$ to 10 V, $V_{DD} = 32 V, I_D = 80 A$	–	269	376	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 V$ to 1 V, $V_{DD} = 32 V, I_D = 80 A$	–	17	–	nC
Q_{gs}	Gate-to-Source Gate Charge	$V_{DD} = 32 V, I_D = 80 A$	–	56	–	nC
Q_{gd}	Gate-to-Drain "Miller" Charge	$V_{DD} = 32 V, I_D = 80 A$	–	33	–	nC

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 20 V, I_D = 80 A, V_{GS} = 10 V,$ $R_{GEN} = 6 \Omega$	–	–	150	ns
$t_{d(on)}$	Turn-On Delay Time		–	27	–	ns
t_r	Turn-On Rise Time		–	49	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	196	–	ns
t_f	Turn-Off Fall Time		–	79	–	ns
t_{off}	Turn-Off Time		–	–	412	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80 A, V_{GS} = 0 V$	–	0.78	1.25	V
		$I_{SD} = 40 A, V_{GS} = 0 V$	–	0.74	1	
t_{rr}	Reverse-Recovery Time	$I_F = 80 A, di_{SD}/dt = 100 A/\mu s$	–	130	195	ns
Q_{rr}	Reverse-Recovery Charge		–	270	405	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

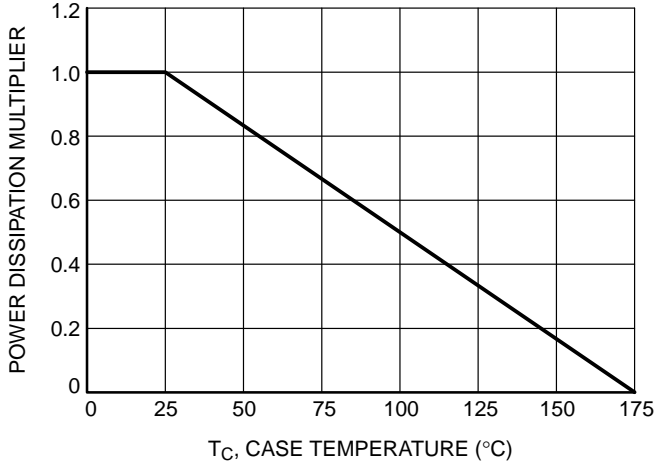


Figure 1. Normalized Power Dissipation vs. Case Temperature

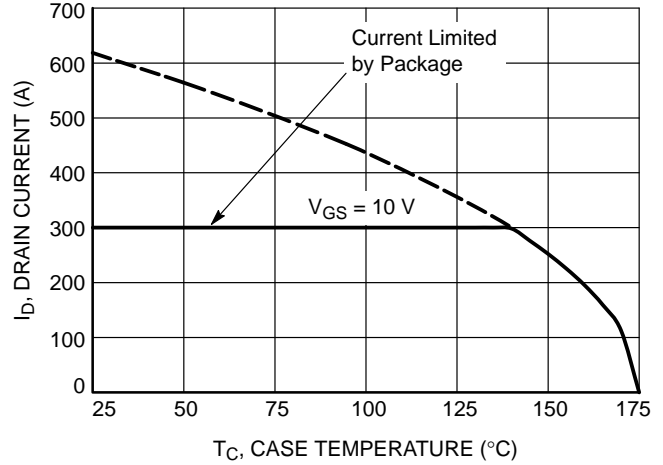


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

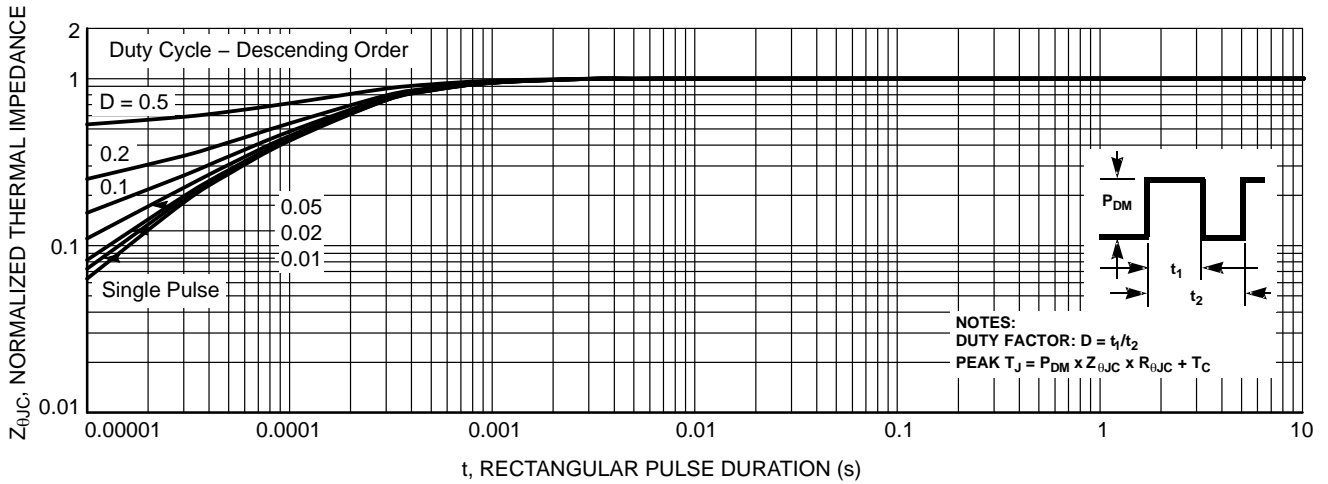


Figure 3. Normalized Maximum Transient Thermal Impedance

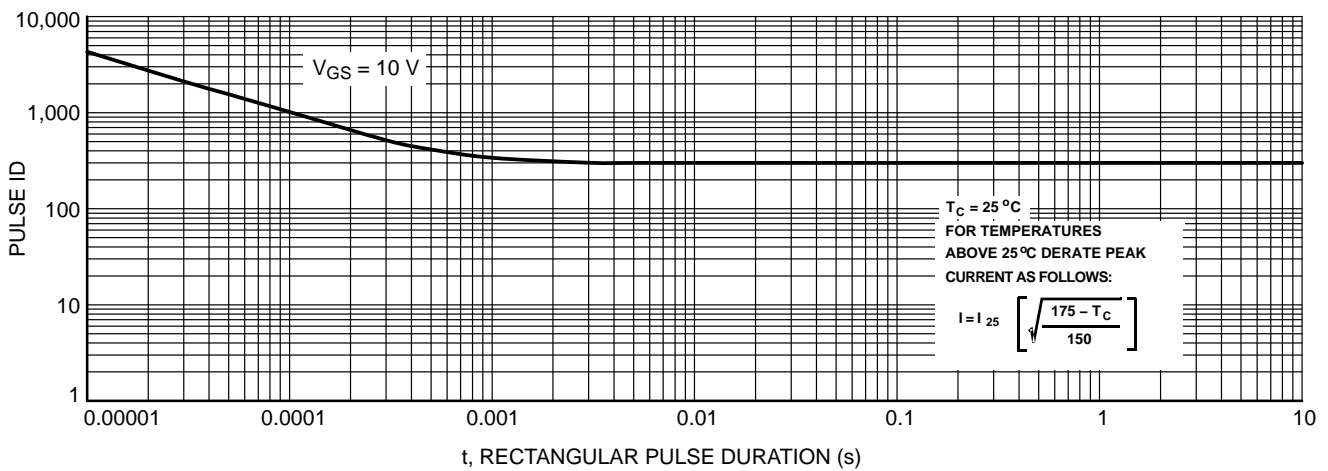


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

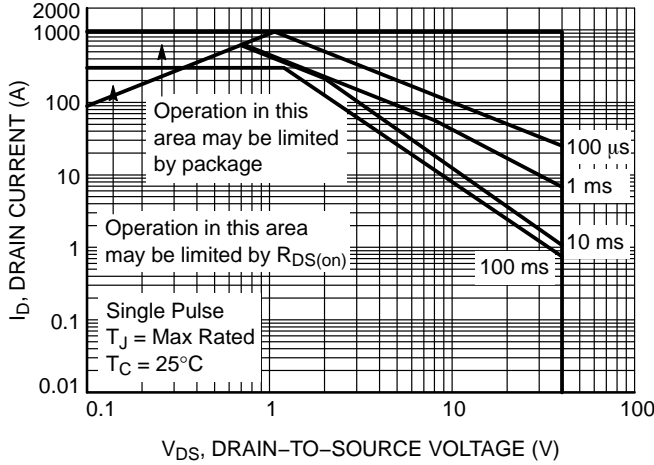


Figure 5. Forward Bias Safe Operating Area

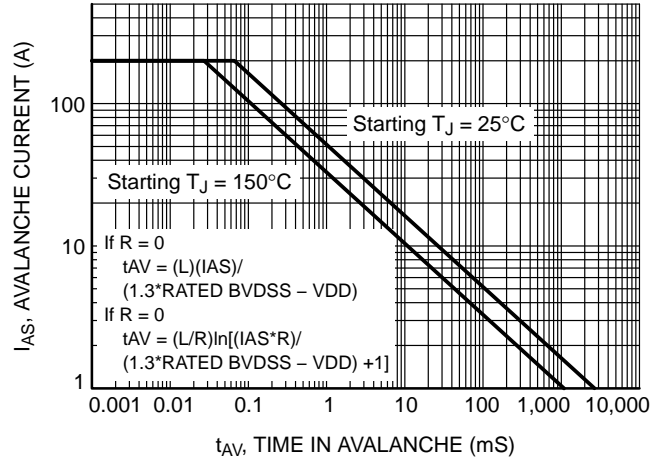


Figure 6. Unclamped Inductive Switching Capability

Note: Refer to ON Semiconductor Application Notes AN7514 and AN7515

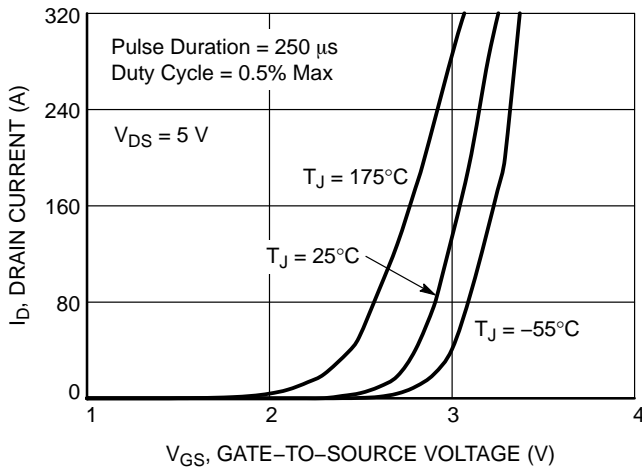


Figure 7. Transfer Characteristics

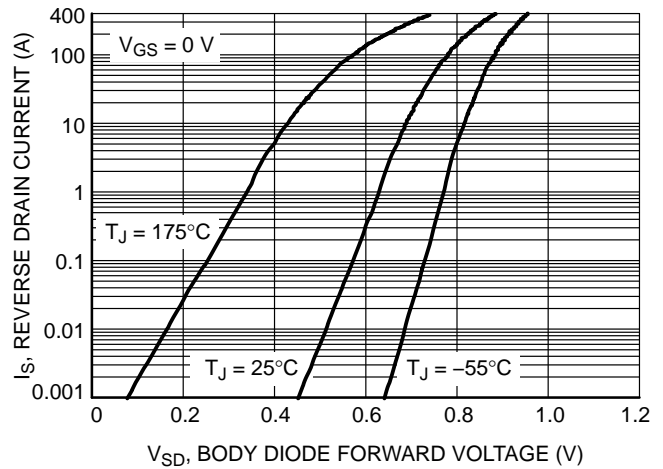


Figure 8. Forward Diode Characteristics

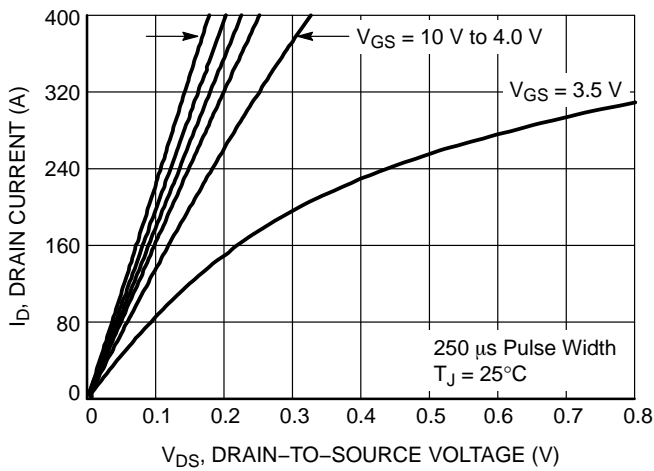


Figure 9. Saturation Characteristics

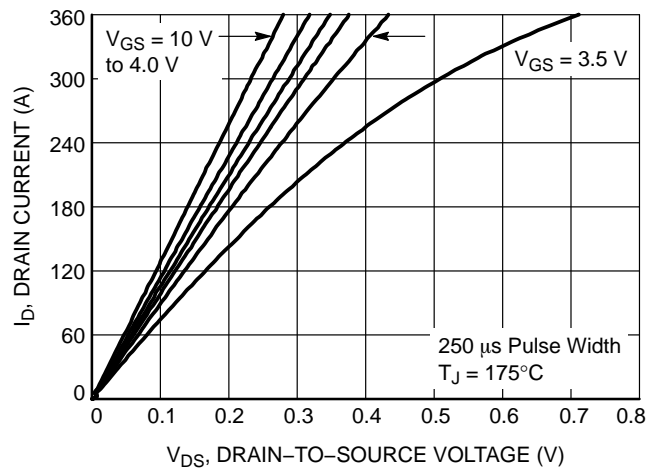


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

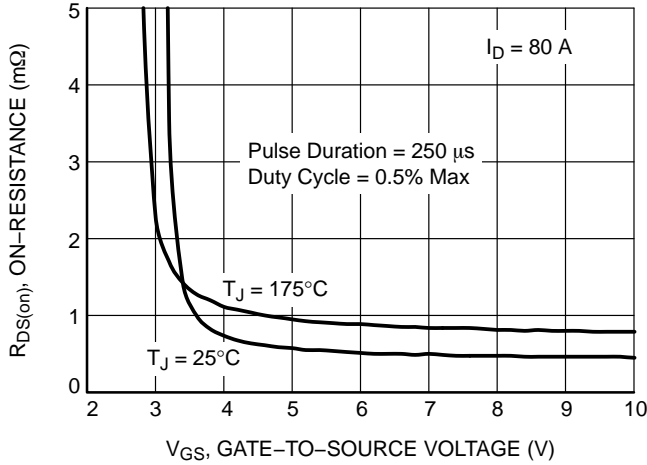


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

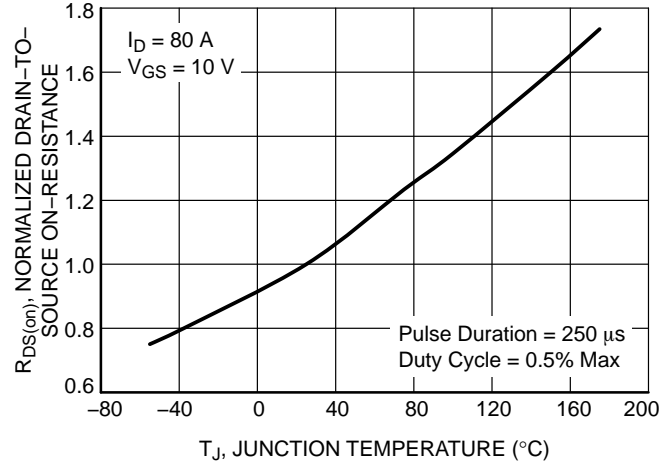


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

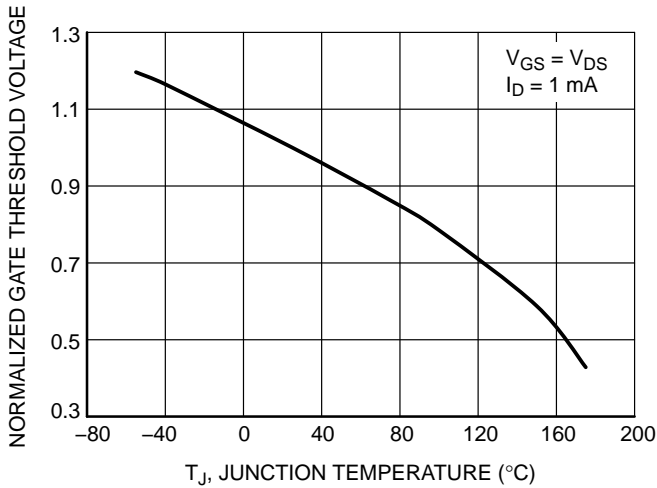


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

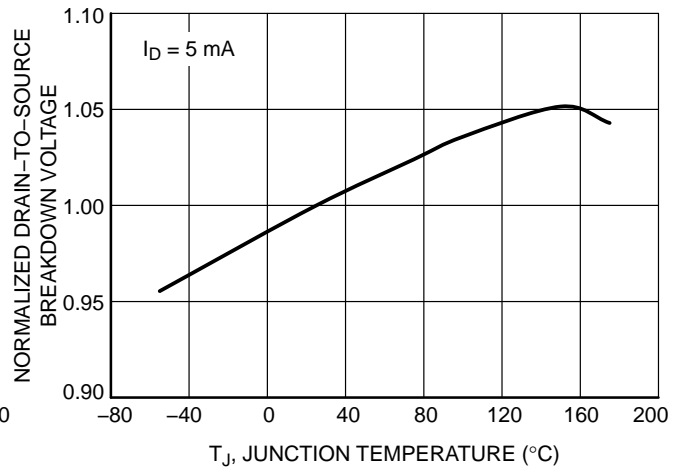


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

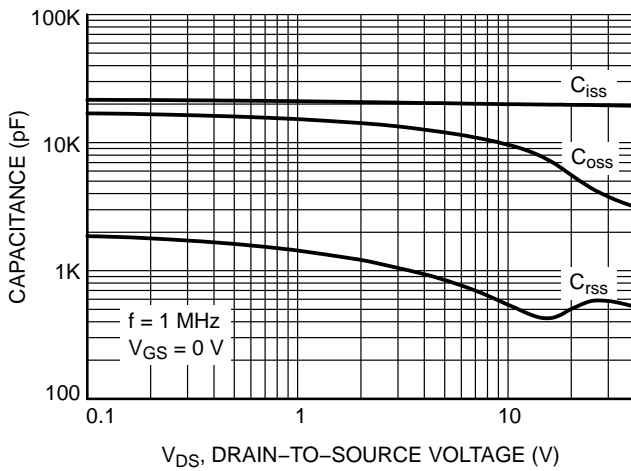


Figure 15. Capacitance vs. Drain-to-Source Voltage

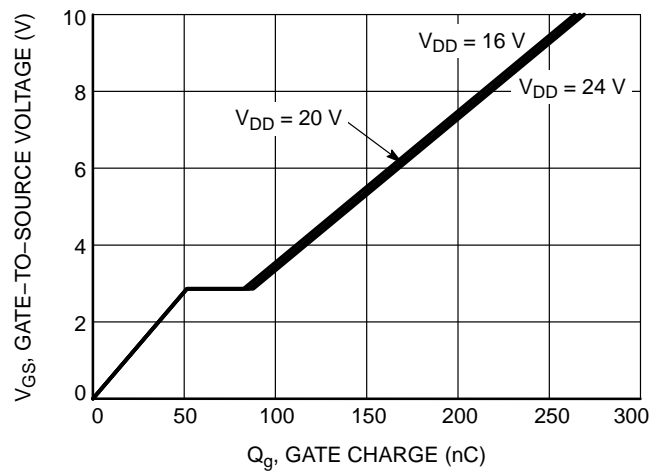


Figure 16. Gate Charge vs. Gate-to-Source Voltage

FDBL9401L-F085

PACKAGE MARKING AND ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Quantity
FDBL9401L-F085	FDBL9401L	H-PSOF8L (Pb-Free / Halogen Free)	13"	24 mm	2000 Units

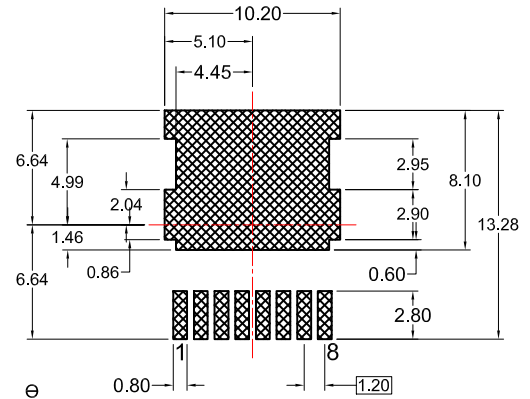
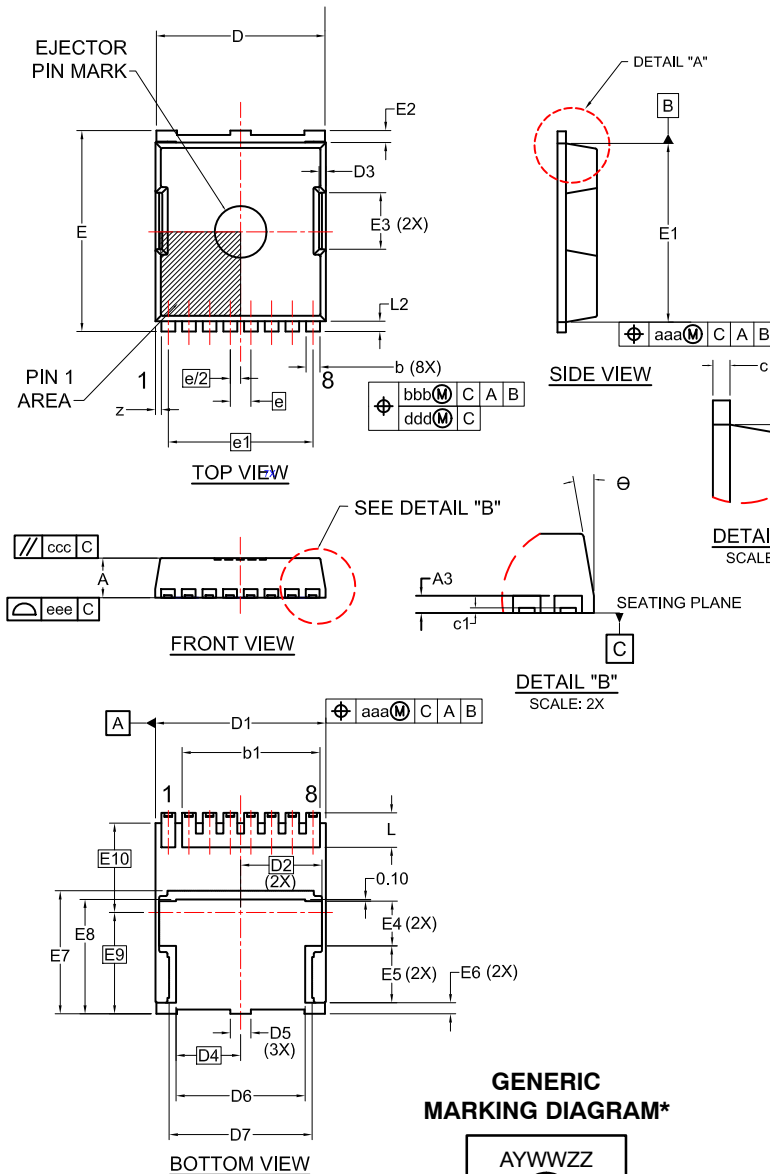
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



H-PSOF8L 11.68x9.80 CASE 100CU ISSUE A

DATE 06 JAN 2020



LAND PATTERN RECOMMENDATION
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

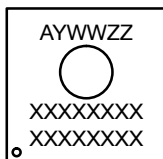
NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A3	0.40	0.50	0.60
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	--	--
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	--	1.20	--
D6	7.40	7.50	7.60
D7	(8.30)		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	--	2.60	--

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	1.50	1.57	1.70
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	--	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		
E5	--	3.30	--
E6	--	0.65	--
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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