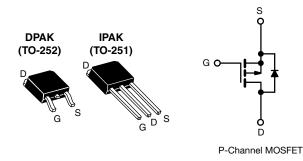


Vishay Siliconix

Power MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	-60				
R _{DS(on)} (Ω)	V _{GS} = -10 V 0.50				
Q _g max. (nC)	12				
Q _{gs} (nC)	3.8				
Q _{gd} (nC)	5.1				
Configuration	Single				

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Surface mount (IRFR9014, SiHFR9014)
- Straight lead (IRFU9014, SiHFU9014)
- Available in tape and reel
- P-channel
- Fast switching
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface-mount applications.

ORDERING INFORMATION							
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)			
Lood (Db) free and belagen free	SiHFR9014-GE3	SiHFR9014TRL-GE3 a	SiHFR9014TR-GE3 a	SiHFU9014-GE3			
Lead (Pb)-free and halogen-free	IRFR9014PbF-BE3	IRFR9014TRLPbF-BE3	IRFR9014TRPbF-BE3	-			
Lead (Pb)-free	IRFR9014PbF	IRFR9014TRLPbF ^a	IRFR9014TRPbF ^a	IRFU9014PbF			

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T C	= 25 °C, un	less otherwis	se noted)		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	-60	v		
Gate-source voltage	V _{GS}	± 20	v		
Continuous drain current	V _{GS} at 5 V	T _C = 25 °C	1-	-5.1	
Continuous drain current	V _{GS} at 5 V	T _C = 100 °C	۱ _D	-3.2	А
Pulsed drain current ^a	I _{DM}	-20			
Linear derating factor		0.20	W/°C		
Linear derating factor (PCB mount) ^e		0.020			
Single pulse avalanche energy ^b			E _{AS}	140	mJ
Repetitive avalanche current ^a			I _{AR}	-5.1	A
Repetitive avalanche energy ^a			E _{AR}	2.5	mJ
Maximum power dissipation	T _C =	25 °C	D	25	w
Maximum power dissipation (PCB mount) e T _A = 25 $^{\circ}$ C			P _D	2.5	vv
Peak diode recovery dV/dt ^c			dV/dt	-4.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C		
Soldering recommendations (peak temperature) ^d	For	10 s		260	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = - 25 V, starting T_J = 25 °C, L = 6.3 mH, R_g = 25 Ω , I_{AS} = - 5.1 A (see fig. 12)

c. $I_{SD} \leq$ - 6.7 A, dl/dt \leq 90 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C

d. 1.6 mm from case

e. When mounted on 1" square PCB (FR-4 or G-10 material)

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1



COMPLIANT

HALOGEN



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THERMAL RESISTANCE RATINGS								
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT			
Maximum junction-to-ambient	R _{thJA}	-	-	110				
Maximum junction-to-ambient (PCB mount) ^a	R _{thJA}	-	-	50	°C/W			
Maximum junction-to-case (drain)	R _{thJC}	-	-	5.0				

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

PARAMETER	SYMBOL	TEST	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 V, I_D = -$	- 250 μA	-60	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25	5 °C, I _D = -1 mA	-	-0.059	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D =$	-250 μA	-2.0	-	-4.0	V
Gate-source leakage	I _{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	$V_{DS} = -60 V, V_{G}$ $V_{DS} = -48 V, V_{G}$	_S = 0 V _S = 0 V, T _J = 125 °C	-	-	-100 -500	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = -3.1 A ^b	-	-	0.50	Ω
Forward transconductance		$V_{DS} = -25 V, I_{D} = -25 V$	= -3.1 A ^b	1.4	-	-	S
Dynamic		•					
Input capacitance	C _{iss}	$V_{GS} = 0 V,$		-	270	-	
Output capacitance	Coss	$V_{DS} = -25 V$,		-	170	-	pF
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, see	e fig. 5	-	31	-	
Total gate charge	Qg	$V_{GS} = -10 \text{ V} \qquad I_D = -6.7 \text{ A}, \text{ V}_{DS} = -48 \text{ V}, \\ \text{see fig. 6 and } 13^{\text{ b}} \qquad -$		-	-	12	nC
Gate-source charge	Q _{gs}			-	-	3.8	
Gate-drain charge	Q _{gd}			-	-	5.1	
Turn-on delay time	t _{d(on)}			-	11	-	
Rise time	tr	$V_{DD} = -30 \text{ V}, \text{ I}_{D} = -30 \text{ V}$		-	63	-	ns
Turn-off delay time	t _{d(off)}	$R_g = 24 \Omega, R_D =$	= 4.0 Ω, see fig. 10 ^b	-	9.6	-	
Fall time	t _f					-	1
Internal drain inductance	L _D	Between lead,	ر لر	-	4.5	-	
Internal source inductance	L _S	6 mm (0.25") fro package and ce die contact ^c		-	7.5	-	nH
Drain-Source Body Diode Characteristic	s	• •					
Continuous source-drain diode current	I _S	MOSFET symbo		-	-	-5.1	
Pulsed diode forward current ^a	I _{SM}		showing the integral reverse p - n junction diode		-	-20	А
Body diode voltage	V _{SD}	T _J = 25 °C, I _S =	-5.1 A, V_{GS} = 0 V ^b	-	-	-5.5	V
Body diode reverse recovery time	t _{rr}	T 05 %0 1		-	80	160	ns
Body diode reverse recovery charge	Q _{rr}	$I_{\rm J} = 25 {}^{-}\rm C, I_{\rm F} =$	-6.7 A, dl/dt = 100 A/µs ^b	-	0.096	0.19	μC
Forward turn-on time	t _{on}	Intrinsic turr	n-on time is negligible (turn	-on is dor	ninated b	v Ls and	L _D)

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width \leq 300 µs; duty cycle \leq 2 %

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

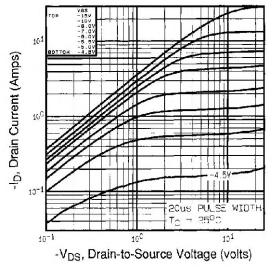


Fig. 1 - Typical Output Characteristics, $T_C = 25 \ ^{\circ}C$

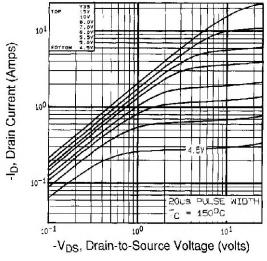


Fig. 2 - Typical Output Characteristics, $T_C = 150 \ ^\circ C$

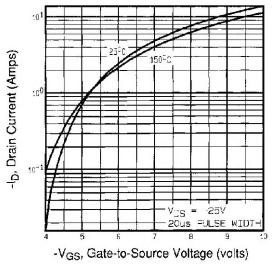


Fig. 3 - Typical Transfer Characteristics

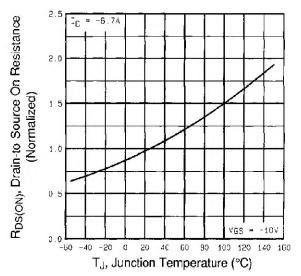


Fig. 4 - Normalized On-Resistance vs. Temperature



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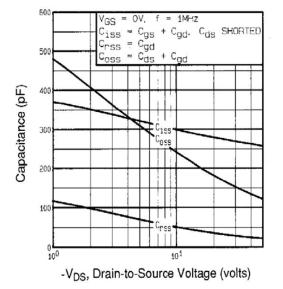


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

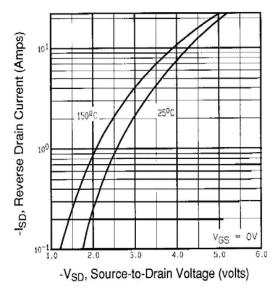


Fig. 7 - Typical Source-Drain Diode Forward Voltage

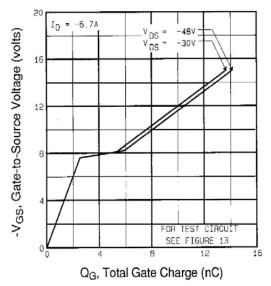
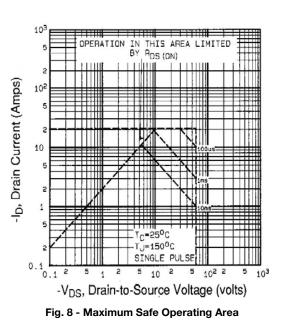


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage





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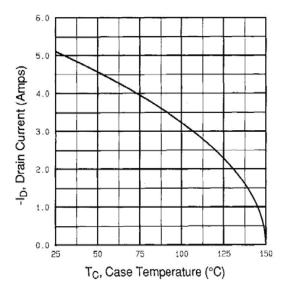


Fig. 9 - Maximum Drain Current vs. Case Temperature

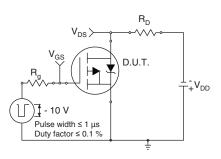


Fig. 10a - Switching Time Test Circuit

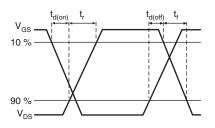


Fig. 10b - Switching Time Waveforms

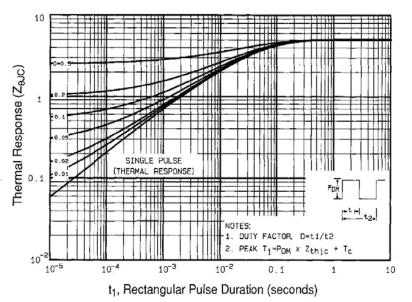


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



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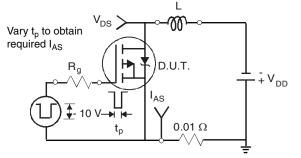


Fig. 12a - Unclamped Inductive Test Circuit

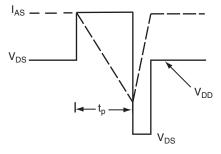


Fig. 12b - Unclamped Inductive Waveforms

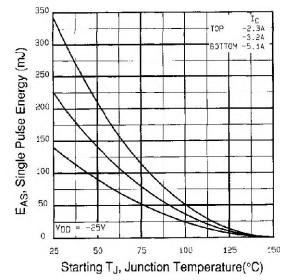


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

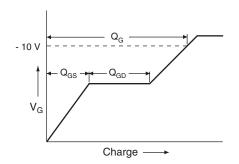


Fig. 13a - Basic Gate Charge Waveform

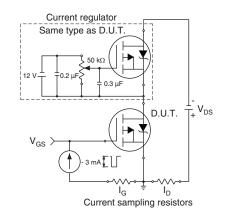


Fig. 13b - Gate Charge Test Circuit

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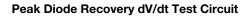
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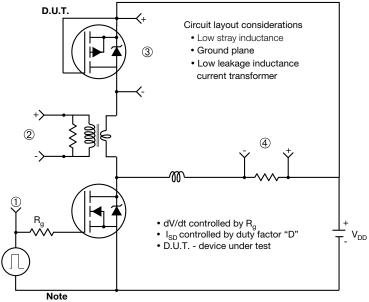
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• Compliment N-Channel of D.U.T. for driver

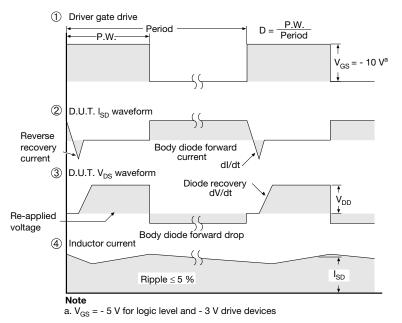


Fig. 14 - For P-Channel

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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y







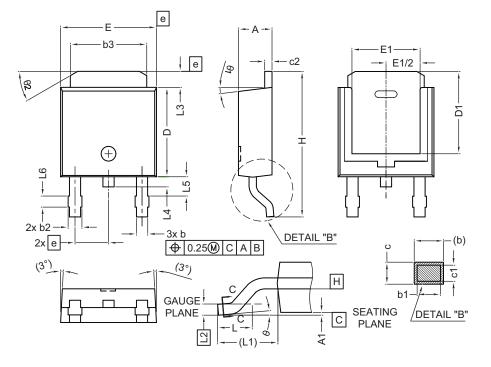
	MILLI	METERS
DIM.	MIN.	MAX.
А	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
С	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
Н	9.40	10.41
е	2.28	BSC
e1	4.56	BSC
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

• Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



	MILLIMETERS					
DIM.	MIN.	MAX.				
A	2.18	2.39				
A1	-	0.13				
b	0.65	0.89				
b1	0.64	0.79				
b2	0.76	1.13				
b3	4.95	5.46				
С	0.46	0.61				
c1	0.41	0.56				
c2	0.46	0.60				
D	5.97	6.22				
D1	5.21	-				
E	6.35	6.73				
E1	4.32	-				
е	2.29	BSC				
Н	9.94	10.34				

	MILLIMETERS					
DIM.	MIN.	MAX.				
L	1.50	1.78				
L1	2.74	l ref.				
L2	0.51	BSC				
L3	0.89	1.27				
L4	-	1.02				
L5	1.14	1.49				
L6	0.65	0.85				
θ	0°	10°				
θ1	0°	15°				
θ2	25°	35°				

Notes

• Dimensioning and tolerance confirm to ASME Y14.5M-1994

• All dimensions are in millimeters. Angles are in degrees

• Heat sink side flash is max. 0.8 mm

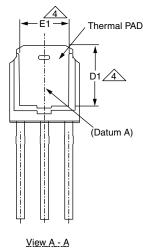
Radius on terminal is optional

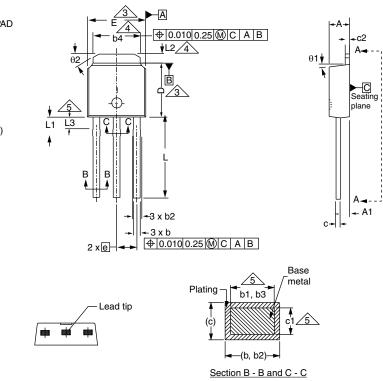
ECN: E19-0649-Rev. Q, 16-Dec-2019 DWG: 5347



Case Outline for TO-251AA (High Voltage)

OPTION 1:





	MILLIN	IETERS	INC	HES			MILLIN	IETERS	INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.	Γ	DIM.	MIN.	MAX.	MIN.	MA
А	2.18	2.39	0.086	0.094	Γ	D1	5.21	-	0.205	-
A1	0.89	1.14	0.035	0.045	Ī	Е	6.35	6.73	0.250	0.26
b	0.64	0.89	0.025	0.035	Γ	E1	4.32	-	0.170	-
b1	0.65	0.79	0.026	0.031	Γ	е	2.29	BSC	2.29	BSC
b2	0.76	1.14	0.030	0.045	Ī	L	8.89	9.65	0.350	0.38
b3	0.76	1.04	0.030	0.041	Ī	L1	1.91	2.29	0.075	0.09
b4	4.95	5.46	0.195	0.215	Γ	L2	0.89	1.27	0.035	0.05
С	0.46	0.61	0.018	0.024	Ī	L3	1.14	1.52	0.045	0.06
c1	0.41	0.56	0.016	0.022	Ī	θ1	0'	15'	0'	15
c2	0.46	0.86	0.018	0.034	Ī	θ2	25'	35'	25'	35
D	5.97	6.22	0.235	0.245	ľ		•	•	•	•

DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA

Revision: 27-Dec-2021

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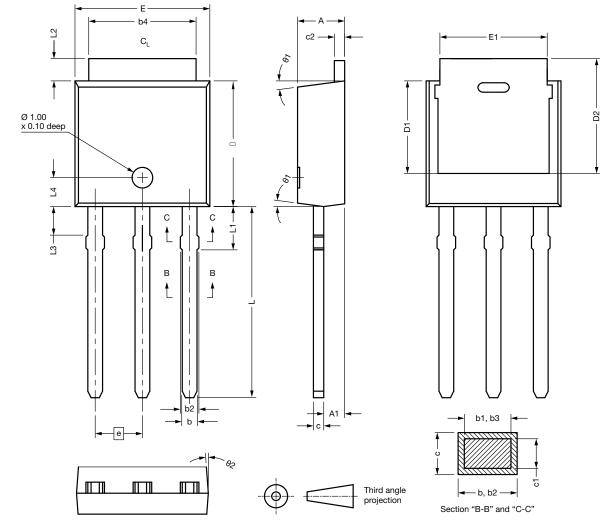
Document Number: 91362

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OPTION 2: FACILITY CODE = N



DIM.	MIN.	NOM.	MAX.	7 6	DIM.	MIN.	Ν
А	2.180	2.285	2.390	1 [D2	5.380	
A1	0.890	1.015	1.140		E	6.350	6
b	0.640	0.765	0.890		E1	4.32	
b1	0.640	0.715	0.790		е	2.29	BSC
b2	0.760	0.950	1.140		L	8.890	ę
b3	0.760	0.900	1.040		L1	1.910	2
b4	4.950	5.205	5.460		L2	0.890	1
С	0.460	-	0.610		L3	1.140	1
c1	0.410	-	0.560		L4	1.300	1
c2	0.460	-	0.610		θ1	0°	
D	5.970	6.095	6.220		θ2	4°	
D1	4.300	-	-				
ECN: E21-06 DWG: 5968	82-Rev. C, 27-Dec	-2021		· ·			

Notes

Dimensioning and tolerancing per ASME Y14.5M-1994

• All dimension are in millimeters, angles are in degrees

• Heat sink side flash is max. 0.8 mm

2

NOM.

-

6.540

-

9.270

2.100

1.080

1.330

1.400

7.5°

-

MAX.

-

6.730 -

9.650

2.290

1.270

1.520

1.500

15° -



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)

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