

NVMFS6D1N08H

Power MOSFET

80 V, 5.5 mΩ, 89 A, Single N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFSW6D1N08H – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters (USB PD) SR
- Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit |
|--|----------------|-------------|------------------|
| Drain-to-Source Voltage | V_{DSS} | 80 | V |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Note 1) | I_D | 89 | A |
| Power Dissipation $R_{\theta JC}$ (Note 1) | | | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2) | I_D | 17 | A |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | | | |
| Pulsed Drain Current | I_{DM} | 468 | A |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ |
| Source Current (Body Diode) | I_S | 87 | A |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{AV} = 5.9\text{ A}$) | E_{AS} | 465 | mJ |
| Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s) | T_L | 300 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State (Note 1) | $R_{\theta JC}$ | 1.44 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 1) | $R_{\theta JA}$ | 40 | |

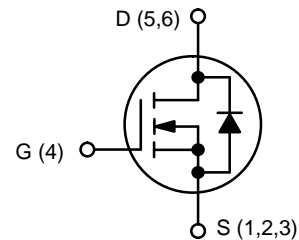
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in² pad size, 1 oz. Cu pad.



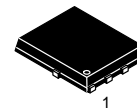
ON Semiconductor®

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| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ MAX}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| 80 V | 5.5 mΩ @ 10 V | 89 A |

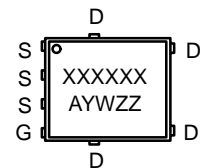


N-CHANNEL MOSFET



DFN5
(SO-8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



XXXXXX = 6D1N08
(NVMFS6D1N08H) or
W6D1N8
(NVMFSW6D1N08H)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NVMFS6D1N08H

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|--------------------------------------|--|------------------------|------|-----|-------|
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 80 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | I _D = 250 μA, ref to 25°C | | 43.8 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 80 V | T _J = 25°C | | 10 | μA |
| | | | T _J = 125°C | | 100 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = 20 V | | | 100 | nA |

ON CHARACTERISTICS (Note 3)

| | | | | | | |
|-----------------------------------|-------------------------------------|---|-----|-------|-----|-------|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 120 μA | 2.0 | | 4.0 | V |
| Threshold Temperature Coefficient | V _{GS(TH)} /T _J | I _D = 250 μA, ref to 25°C | | -7.08 | | mV/°C |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 20 A | | 4.5 | 5.5 | mΩ |
| Forward Transconductance | g _{FS} | V _{DS} = 15 V, I _D = 20 A | | 80 | | S |
| Gate-Resistance | R _G | T _A = 25°C | | 1.0 | | Ω |

CHARGES & CAPACITANCES

| | | | | | | |
|------------------------------|---------------------|---|--|------|--|----|
| Input Capacitance | C _{ISS} | V _{GS} = 0 V, f = 1 MHz, V _{DS} = 40 V | | 2085 | | pF |
| Output Capacitance | C _{OSS} | | | 300 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | 10 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 6 V, V _{DS} = 40 V, I _D = 30 A | | 10 | | nC |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 40 V, I _D = 30 A | | 32 | | nC |
| Gate-to-Source Charge | Q _{GS} | | | 10 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 6 | | |
| Plateau Voltage | V _{GP} | | | 5 | | |

SWITCHING CHARACTERISTICS (Note 3)

| | | | | | | |
|---------------------|---------------------|---|--|----|--|----|
| Turn-On Delay Time | t _{d(ON)} | V _{GS} = 10 V, V _{DS} = 64 V, I _D = 30 A, R _G = 2.5 Ω | | 18 | | ns |
| Rise Time | t _r | | | 50 | | |
| Turn-Off Delay Time | t _{d(OFF)} | | | 48 | | |
| Fall Time | t _f | | | 39 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

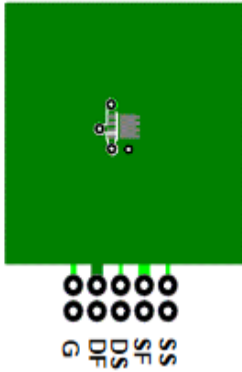
| | | | | | | | |
|-------------------------|-----------------|--|------------------------|----|-----|-----|---|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 20 A | T _J = 25°C | | 0.8 | 1.2 | V |
| | | | T _J = 125°C | | 0.7 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 20 A | | 49 | | ns | |
| Reverse Recovery Charge | Q _{RR} | | | 60 | | nC | |
| Charge Time | t _a | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 20 A | | 30 | | ns | |
| Discharge Time | t _b | | | 19 | | ns | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

4. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

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a) 53°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

5. Pulse Test: pulse width < 300 μ s, duty cycle < 2%.
6. E_{AS} of 465 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 5.9$ A, $V_{DD} = 80$ V, $V_{GS} = 10$ V. 100% test at $I_{AS} = 8.4$ A.
7. As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

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TYPICAL CHARACTERISTICS

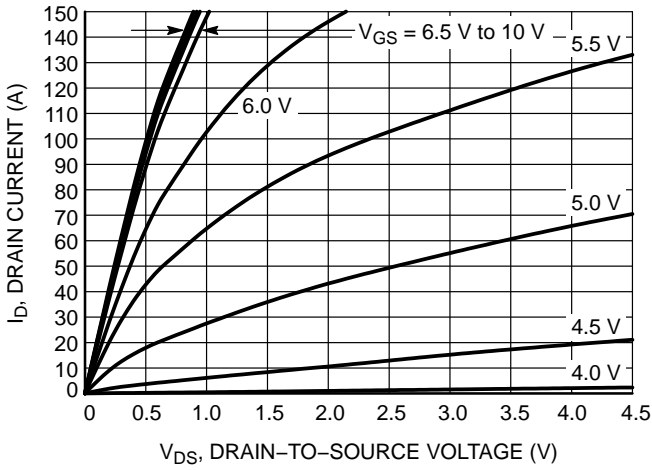


Figure 1. On-Region Characteristics

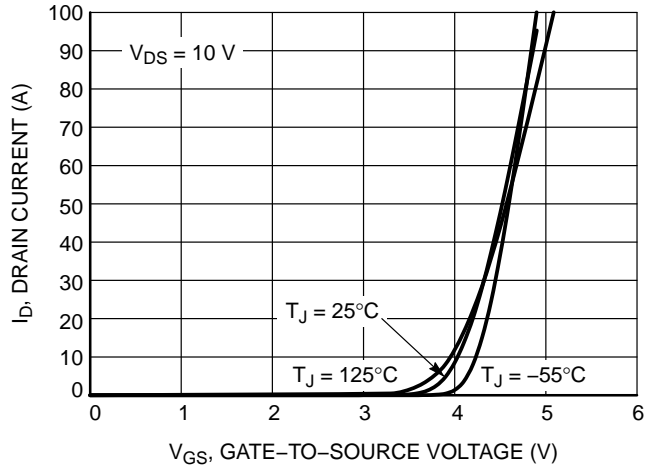


Figure 2. Transfer Characteristics

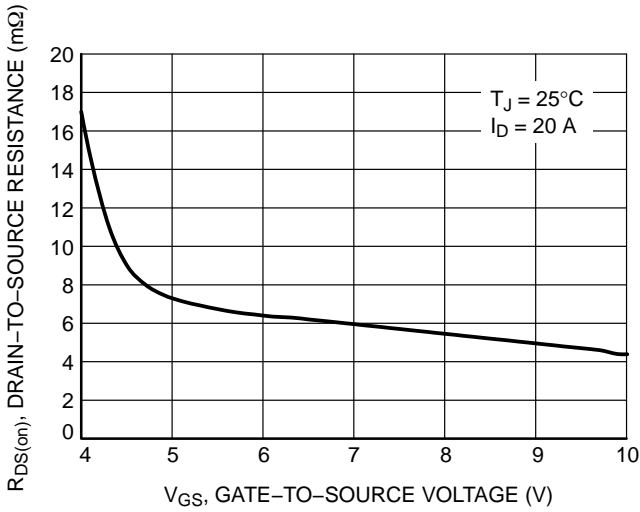


Figure 3. On-Resistance vs. Gate-to-Source Voltage

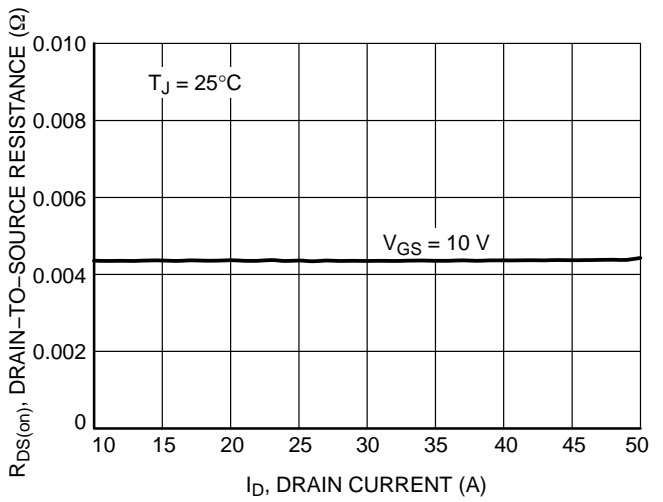


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

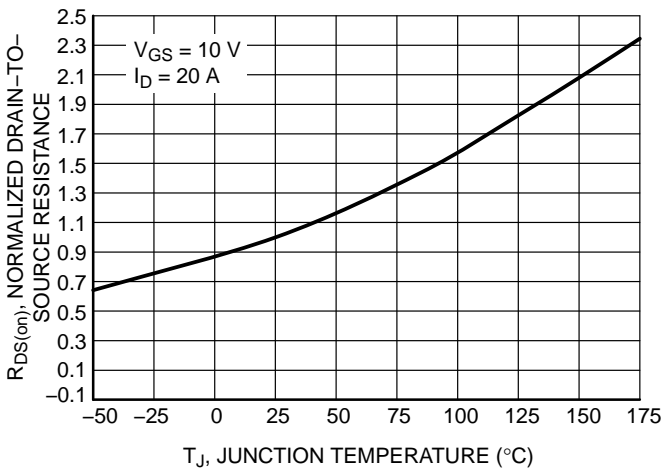


Figure 5. On-Resistance Variation with Temperature

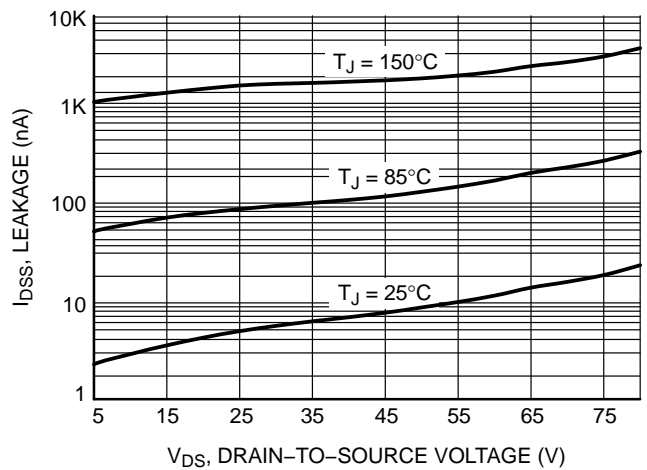


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVMFS6D1N08H

TYPICAL CHARACTERISTICS

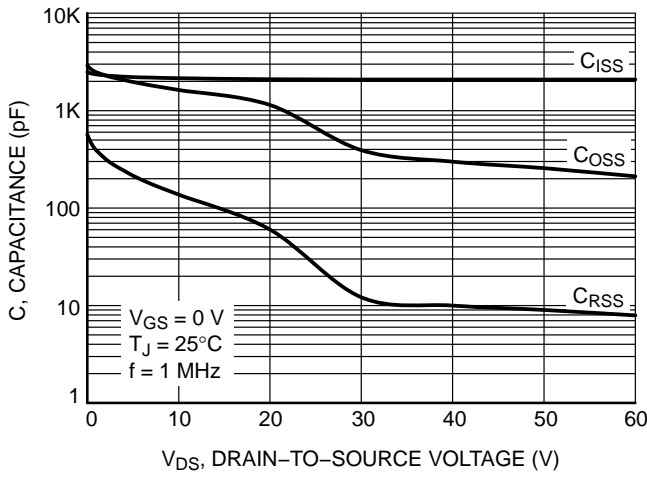


Figure 7. Capacitance Variation

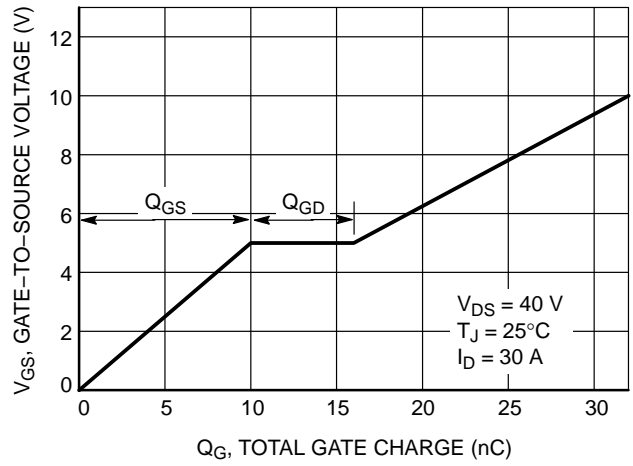


Figure 8. Gate-to-Source Voltage vs. Total Charge

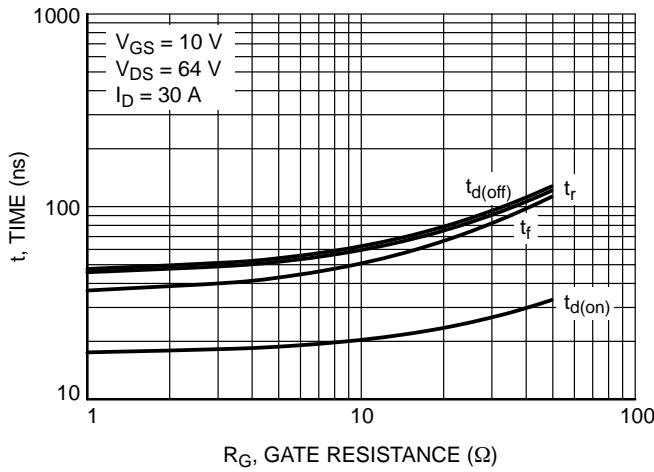


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

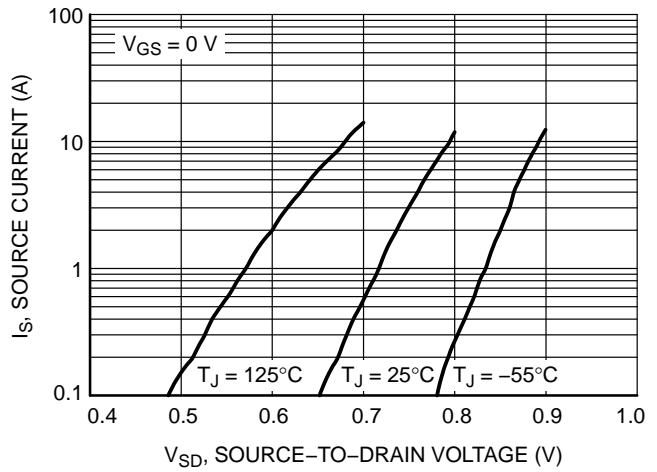


Figure 10. Diode Forward Voltage vs. Current

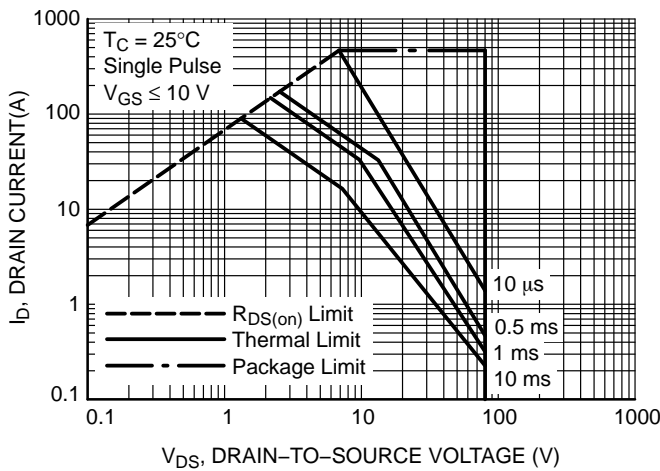


Figure 11. Maximum Rated Forward Biased Safe Operating Area

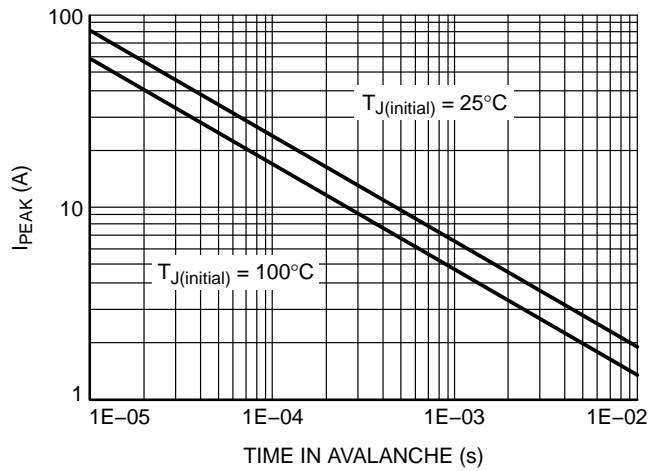


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

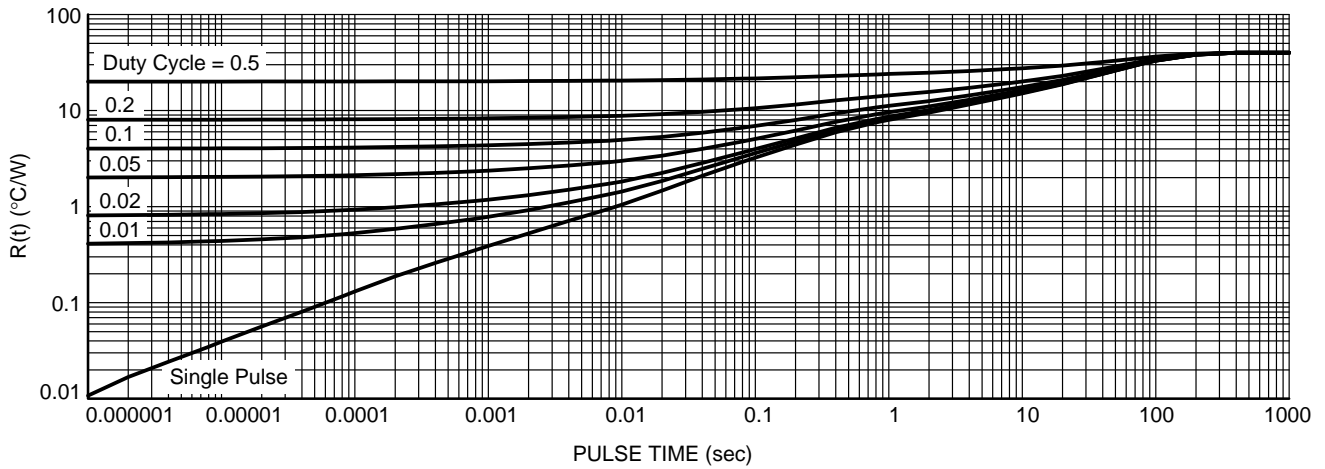


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|------------------|---------|------------------------------------|-----------------------|
| NVMFS6D1N08HT1G | 6D1N08 | DFN5 (Pb-Free) | 1500 / Tape & Reel |
| NVMFSW6D1N08HT1G | W6D1N8 | DFN5 (Pb-Free, Wettable Flanks) | 1500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | 5.00 | 5.15 | 5.30 |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 | 4.20 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.45 | 3.65 | 3.85 |
| e | 1.27 BSC | | |
| G | 0.51 | 0.575 | 0.71 |
| K | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.575 | 0.71 |
| L1 | 0.125 REF | | |
| M | 3.00 | 3.40 | 3.80 |
| θ | 0° | --- | 12° |

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|--------------------------|--|
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| DESCRIPTION: | DFN5 5x6, 1.27P (SO-8FL) | PAGE 1 OF 1 |

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