



PMGD175XNE

30 V, Dual N-channel Trench MOSFET

15 April 2016

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (TSSOP6) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

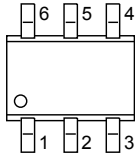
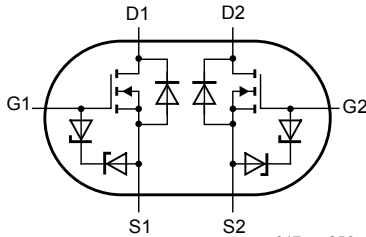
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|--|-----|-----|------|------------|
| Per transistor | | | | | | |
| V_{DS} | drain-source voltage | $T_J = 25\text{ °C}$ | - | - | 30 | V |
| V_{GS} | gate-source voltage | | -12 | - | 12 | V |
| I_D | drain current | $V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$ | [1] | - | 0.95 | A |
| Static characteristics (per transistor) | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 4.5\text{ V}; I_D = 0.9\text{ A}; T_J = 25\text{ °C}$ | - | 211 | 252 | m Ω |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|--|--|
| 1 | S1 | source TR1 |  <p>TSSOP6 (SOT363)</p> |  <p>017aaa256</p> |
| 2 | G1 | gate TR1 | | |
| 3 | D2 | drain TR2 | | |
| 4 | S2 | source TR2 | | |
| 5 | G2 | gate TR2 | | |
| 6 | D1 | drain TR1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| PMGD175XNE | TSSOP6 | plastic surface-mounted package; 6 leads | SOT363 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PMGD175XNE | LU% [1] |

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---------------------------|-------------------------|---|-----|-----|------|------|
| Per transistor | | | | | | |
| V_{DS} | drain-source voltage | $T_j = 25\text{ °C}$ | | - | 30 | V |
| V_{GS} | gate-source voltage | | | -12 | 12 | V |
| I_D | drain current | $V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$ | [1] | - | 0.95 | A |
| | | $V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$ | [1] | - | 0.87 | A |
| | | $V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$ | [1] | - | 0.5 | A |
| I_{DM} | peak drain current | $T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$ | | - | 4 | A |
| P_{tot} | total power dissipation | $T_{amb} = 25\text{ °C}$ | [2] | - | 260 | mW |
| | | | [1] | - | 310 | mW |
| | | $T_{sp} = 25\text{ °C}$ | | - | 905 | mW |
| Per device | | | | | | |
| P_{tot} | total power dissipation | $T_{amb} = 25\text{ °C}$ | [2] | - | 390 | mW |
| T_j | junction temperature | | | -55 | 150 | °C |
| T_{amb} | ambient temperature | | | -55 | 150 | °C |
| T_{stg} | storage temperature | | | -65 | 150 | °C |
| Source-drain diode | | | | | | |
| I_S | source current | $T_{amb} = 25\text{ °C}$ | [1] | - | 0.31 | A |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

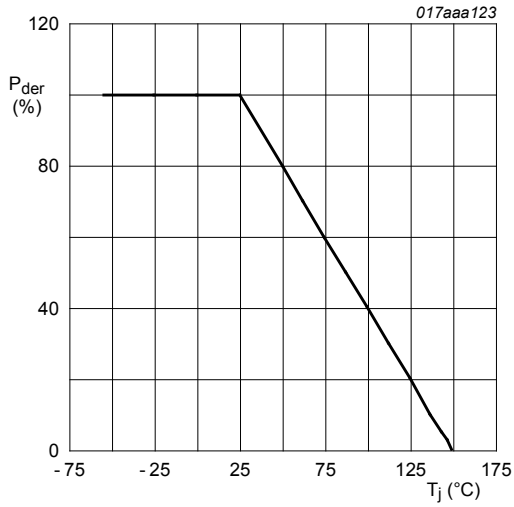


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

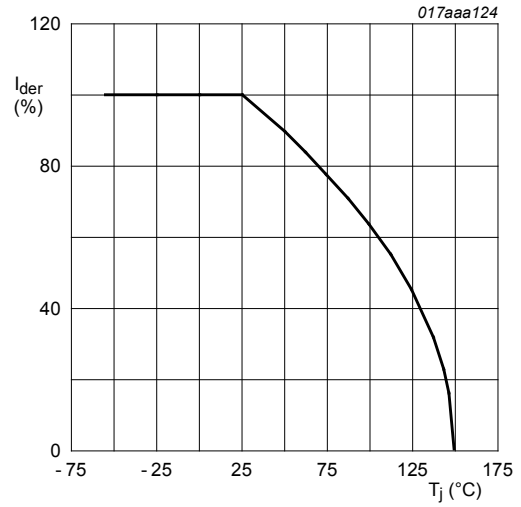


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

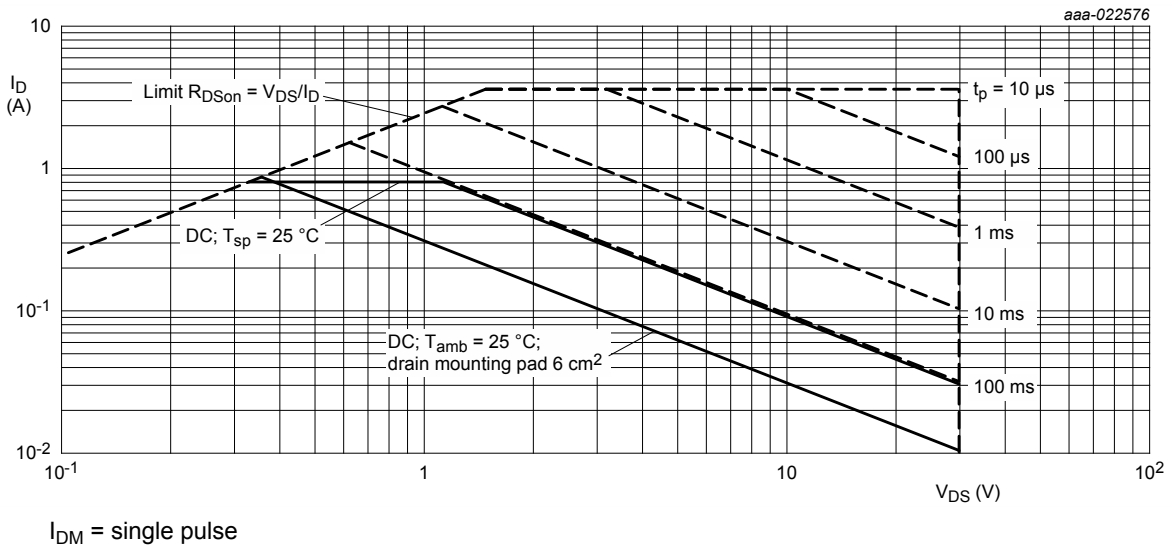


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

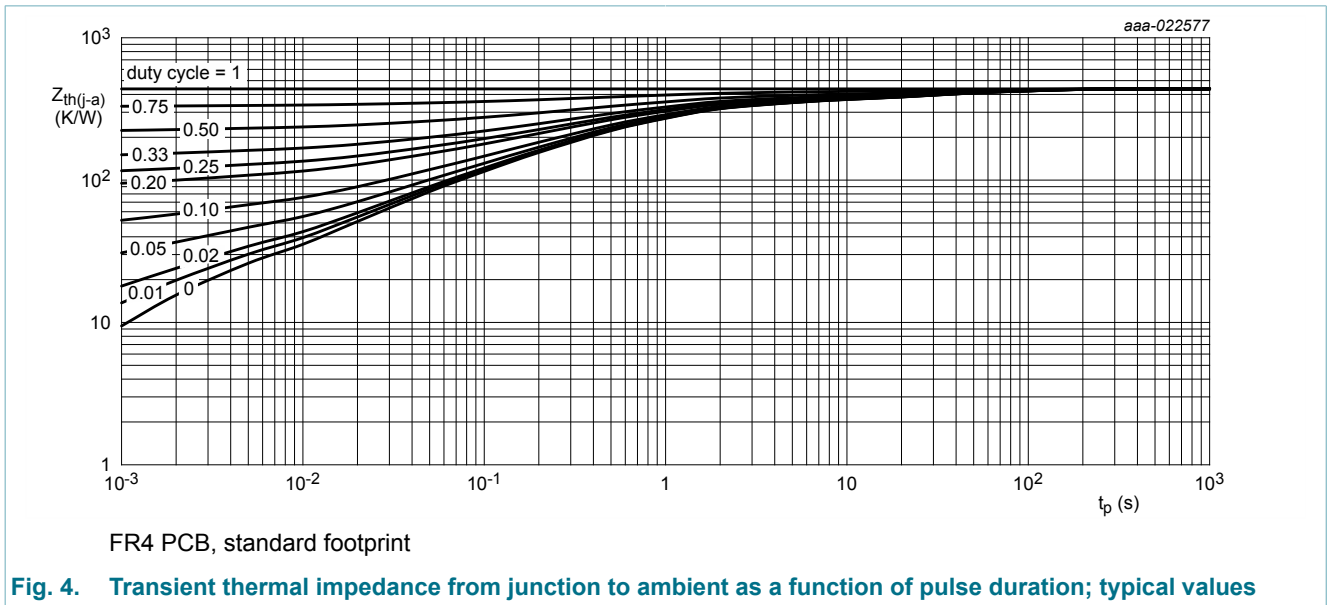
9. Thermal characteristics

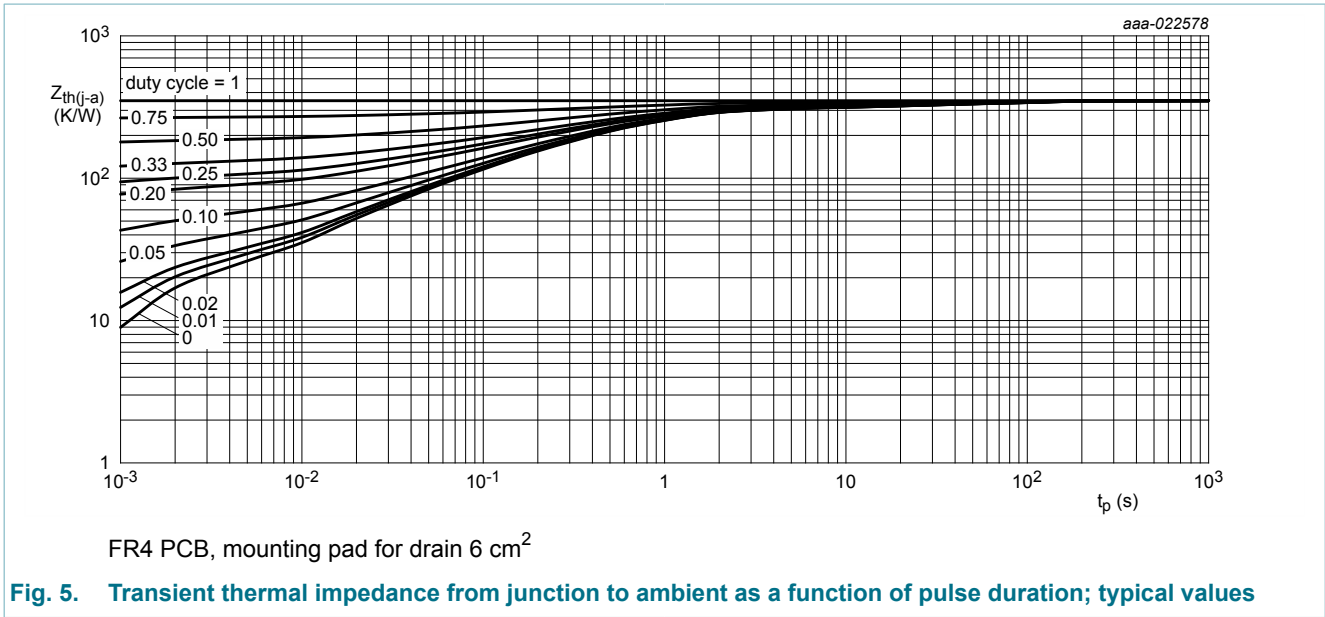
Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------------------|--|---------------------------|-----|-----|-----|-----|------|
| Per transistor | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | 417 | 480 | K/W |
| | | | [2] | - | 352 | 405 | K/W |
| | | in free air; $t \leq 5$ s | [2] | - | 295 | 340 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | 120 | 138 | K/W |
| Per device | | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 320 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².





10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|----------------------------------|---|---|------|------|------------|
| Static characteristics (per transistor) | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | 30 | - | - | V |
| V_{GSth} | gate-source threshold voltage | $I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$ | 0.75 | 1 | 1.25 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | 1 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 12 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | 10 | μA |
| | | $V_{GS} = -12 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | -10 | μA |
| | | $V_{GS} = 4.5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | 5 | μA |
| | | $V_{GS} = -4.5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | - | -5 | μA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 4.5 V$; $I_D = 0.9 A$; $T_j = 25 \text{ }^\circ C$ | - | 211 | 252 | m Ω |
| | | $V_{GS} = 4.5 V$; $I_D = 0.9 A$; $T_j = 150 \text{ }^\circ C$ | - | 344 | 411 | m Ω |
| | | $V_{GS} = 2.5 V$; $I_D = 0.8 A$; $T_j = 25 \text{ }^\circ C$ | - | 267 | 319 | m Ω |
| g_{fs} | forward transconductance | $V_{DS} = 10 V$; $I_D = 0.9 A$; $T_j = 25 \text{ }^\circ C$ | - | 3.5 | - | S |
| Dynamic characteristics (per transistor) | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $V_{DS} = 15 V$; $I_D = 0.9 A$; $V_{GS} = 4.5 V$; $T_j = 25 \text{ }^\circ C$ | - | 1.05 | 1.65 | nC |
| Q_{GS} | gate-source charge | | - | 0.15 | - | nC |
| Q_{GD} | gate-drain charge | | - | 0.27 | - | nC |
| C_{iss} | input capacitance | $V_{DS} = 15 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | 81 | - | pF |
| C_{oss} | output capacitance | | - | 13 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 9 | - | pF |
| $t_{d(on)}$ | turn-on delay time | | $V_{DS} = 15 V$; $I_D = 0.9 A$; $V_{GS} = 4.5 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ C$ | - | 7 | - |
| t_r | rise time | - | | 14 | - | ns |
| $t_{d(off)}$ | turn-off delay time | - | | 17 | - | ns |
| t_f | fall time | - | | 6 | - | ns |
| Source-drain diode (per transistor) | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 0.3 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$ | - | 0.7 | 1.2 | V |

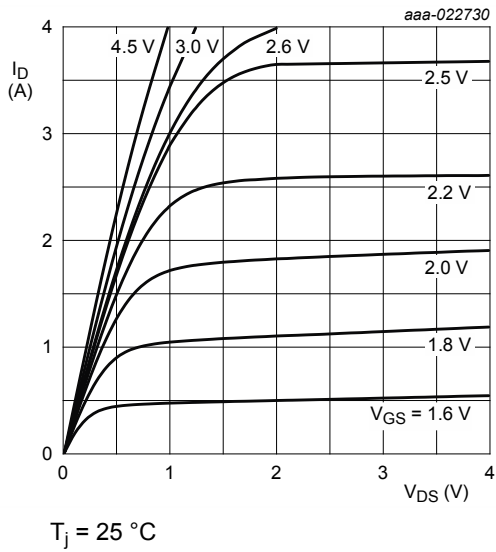


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

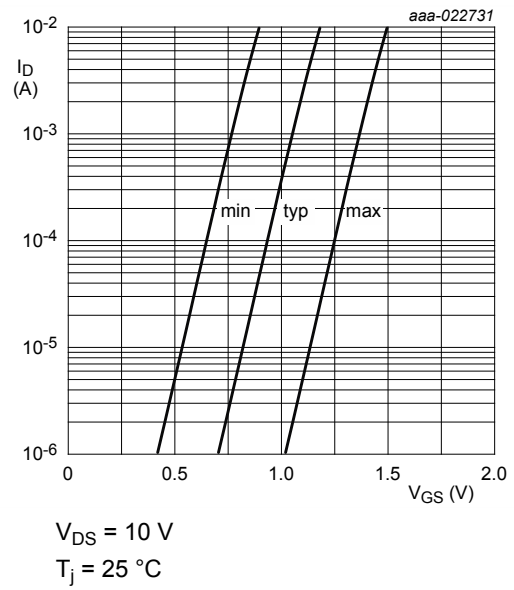


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

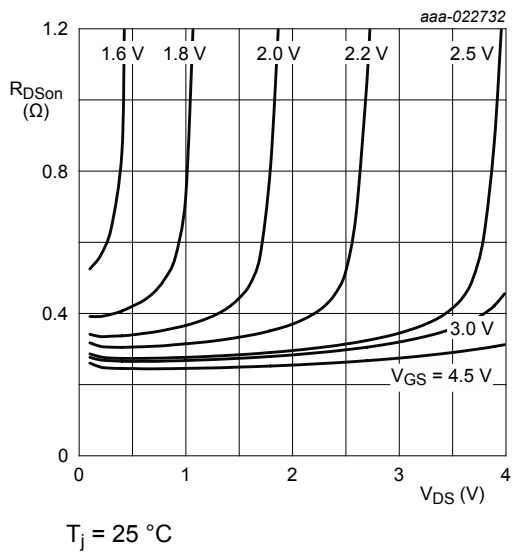


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

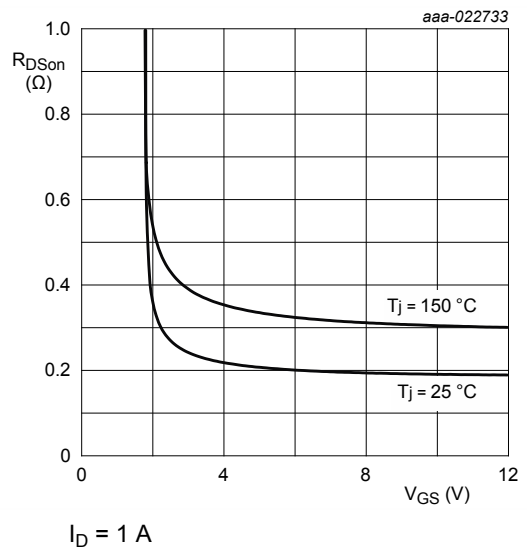


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

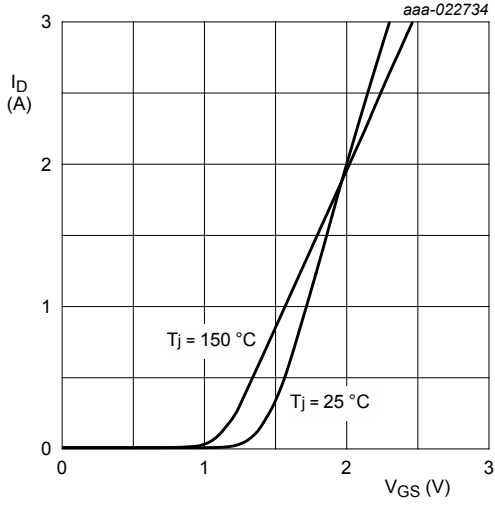


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

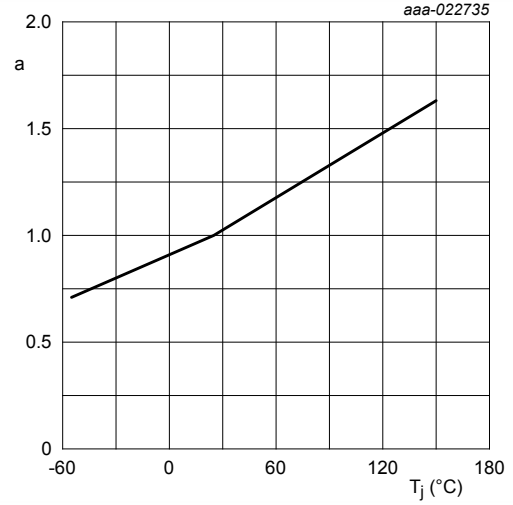


Fig. 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^{\circ}\text{C})}}$$

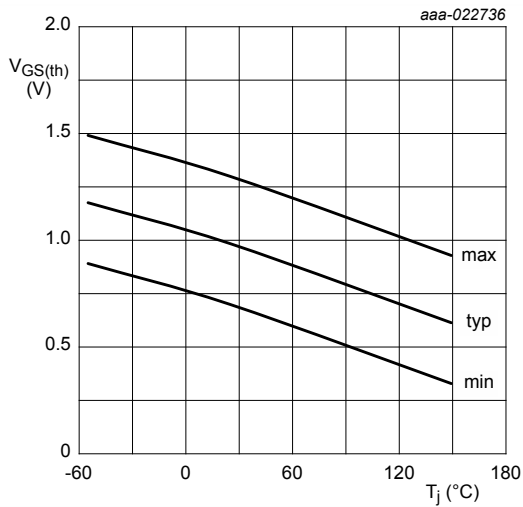


Fig. 12. Gate-source threshold voltage as a function of ambient temperature

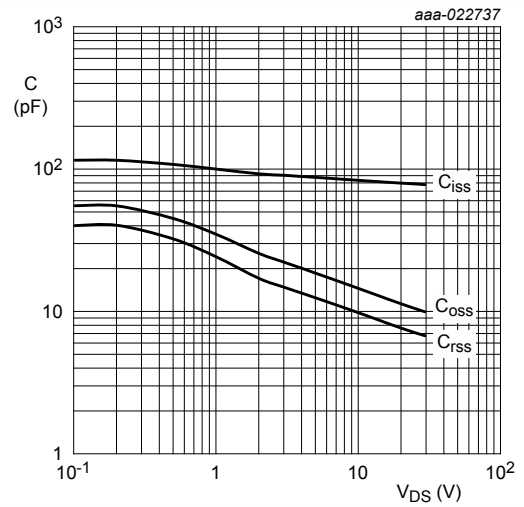
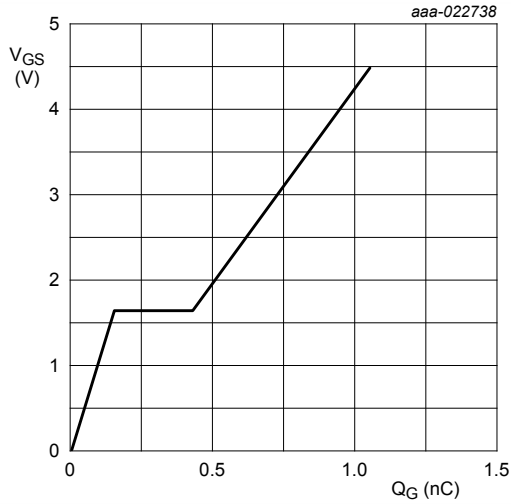


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 15\text{ V}; I_D = 0.91\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

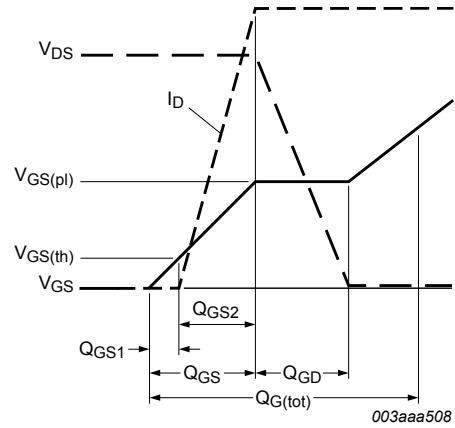
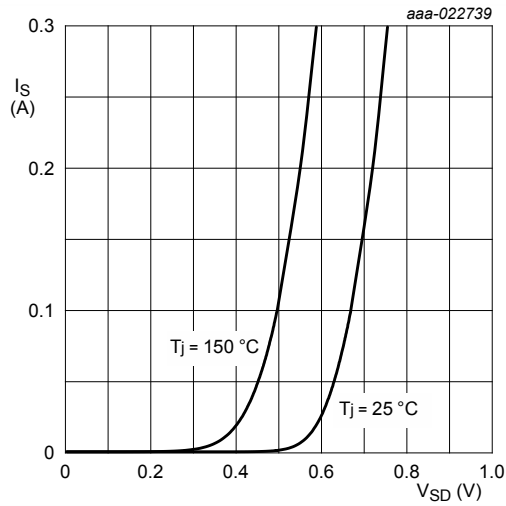


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

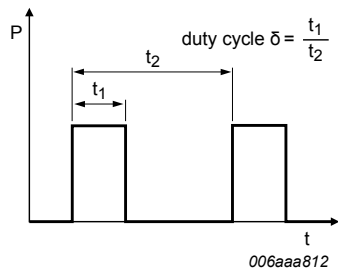


Fig. 17. Duty cycle definition

12. Package outline

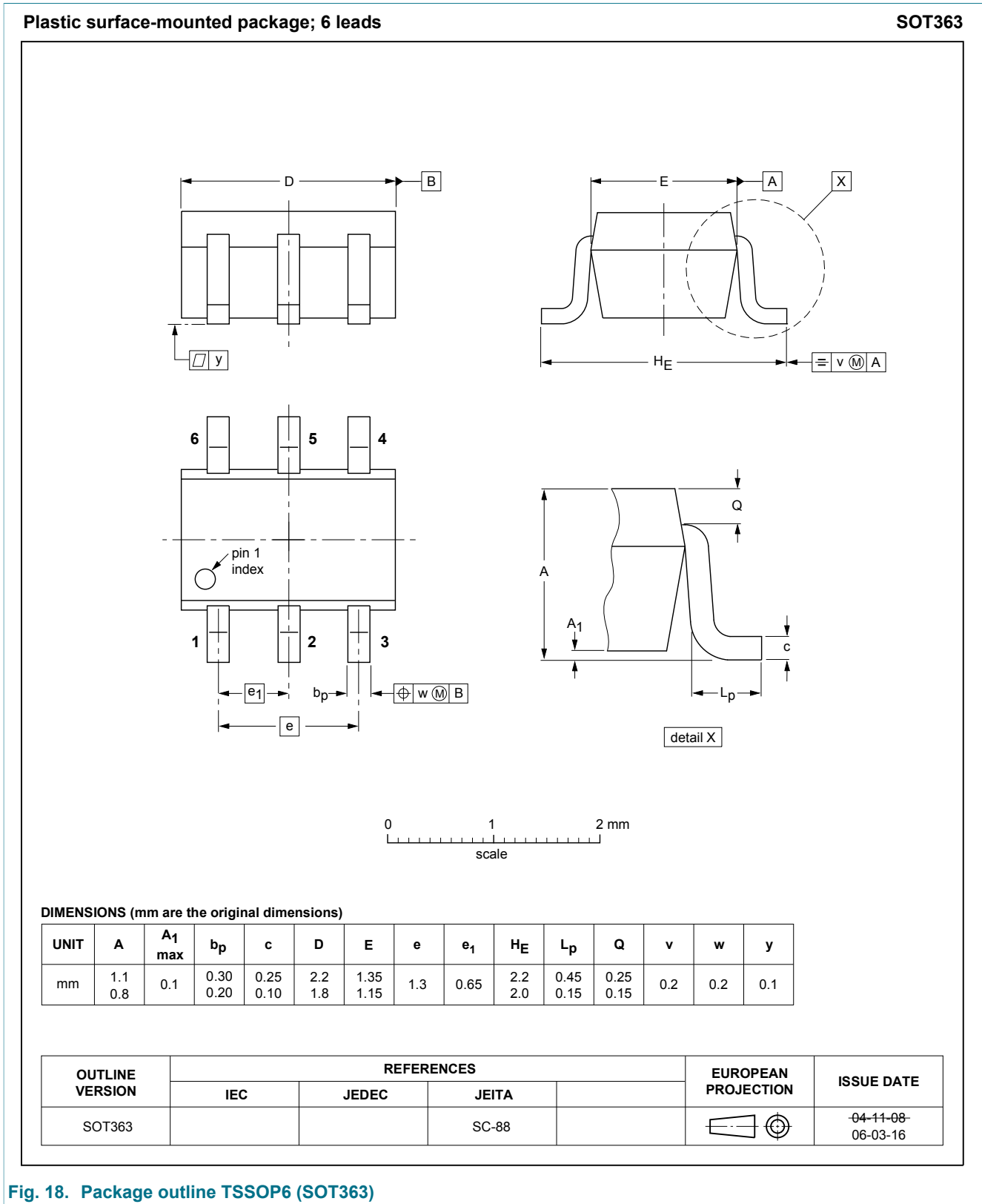


Fig. 18. Package outline TSSOP6 (SOT363)

13. Soldering

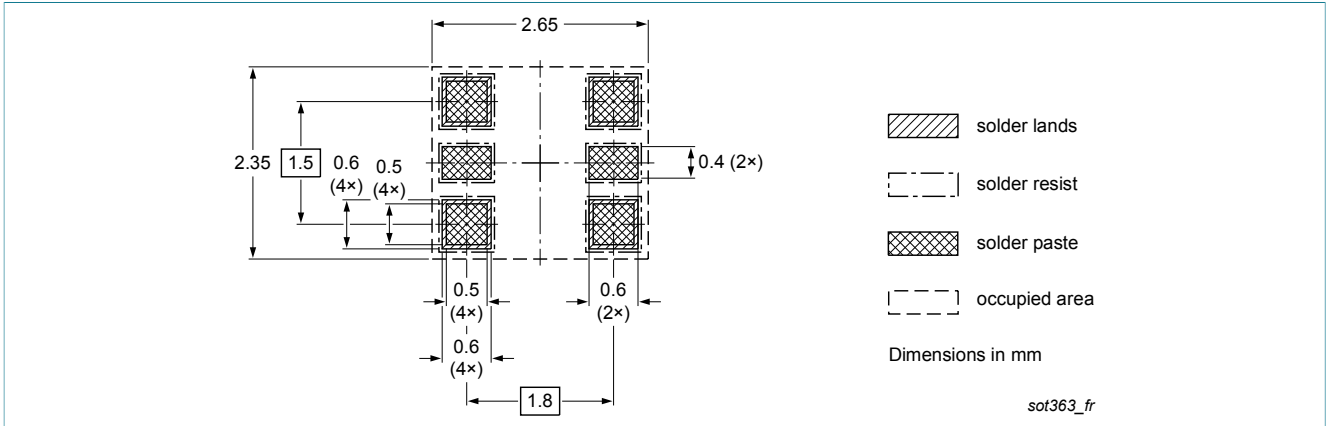


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

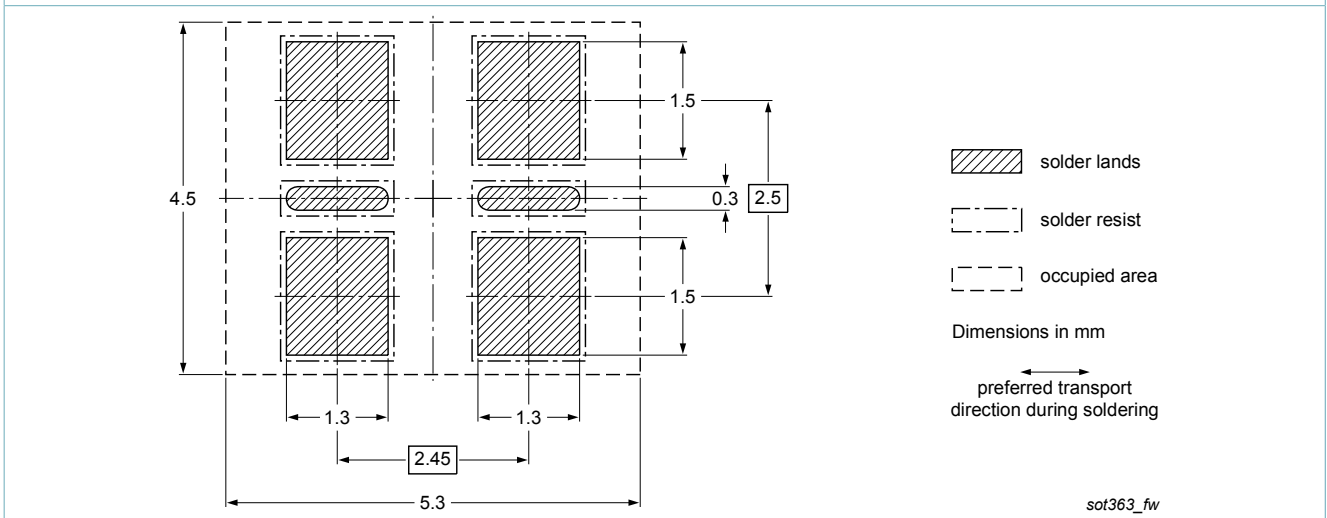


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--------------|--------------------|---------------|------------|
| PMGD175XNE v.1 | 20160415 | Product data sheet | - | - |

15. Legal information

15.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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