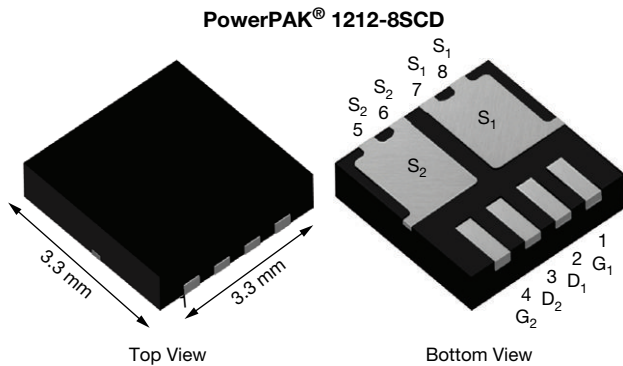


Common Drain Dual N-Channel 25 V (S1-S2) MOSFET



| PRODUCT SUMMARY | |
|--|--------------------|
| V_{S1S2} (V) | 25 |
| $R_{S1S2(on)}$ max. (Ω) at $V_{GS} = 10$ V | 0.0035 |
| $R_{S1S2(on)}$ max. (Ω) at $V_{GS} = 4.5$ V | 0.0056 |
| Q_g typ. (nC) | 16.9 ^g |
| I_{S1S2} (A) | 60 ^{a, h} |
| Configuration | Common drain |

| ORDERING INFORMATION | |
|---------------------------------|--------------------|
| Package | PowerPAK 1212-8SCD |
| Lead (Pb)-free and halogen-free | SiSF02DN-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted) | | | | |
|---|----------------|---------------|----------------------|---|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Drain-source voltage | V_{S1S2} | 25 | V | |
| Gate-source voltage | V_{GS} | +16 / -12 | V | |
| Continuous drain current ($T_J = 150$ °C) | I_{S1S2} | $T_C = 25$ °C | 60 ^h | A |
| | | $T_C = 70$ °C | 60 ^h | |
| | | $T_A = 25$ °C | 30.5 ^{b, c} | |
| | | $T_A = 70$ °C | 24 ^{b, c} | |
| Pulsed drain current ($t = 100$ μ s) | I_{S1S2M} | 140 | | |
| Maximum power dissipation | P_D | $T_C = 25$ °C | 69.4 | W |
| | | $T_C = 70$ °C | 44.4 | |
| | | $T_A = 25$ °C | 5.2 ^{b, c} | |
| | | $T_A = 70$ °C | 3.3 ^{b, c} | |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +150 | °C | |
| Soldering recommendations (peak temperature) ^c | | 260 | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|------------|---------|---------|------|--|
| PARAMETER | SYMBOL | TYPICAL | MAXIMUM | UNIT | |
| Maximum junction-to-ambient ^b | R_{thJA} | 19 | 24 | °C/W | |
| Maximum junction-to-case (drain) | R_{thJC} | 1.4 | 1.8 | | |

Notes

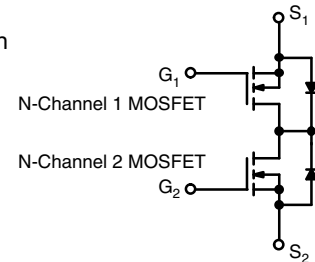
- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8SCD is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 63 °C/W
- Single MOSFET
- Package limited

FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low source-to-source on resistance
- Integrated common-drain n-channel MOSFETs in a compact and thermally enhanced package
- 100 % R_g and UIS tested
- Optimizes circuit layout for bi-directional current flow
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT
 HALOGEN
FREE
APPLICATIONS

- Battery protection switch
- Bi-directional switch
- Load switch





| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | |
|--|----------------|--|--------------------|--------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 25 | - | - | V |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{S1S2} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 1 | - | 2.3 | |
| Gate-source leakage | I_{GSS} | $V_{S1S2} = 0\text{ V}, V_{GS} = +16\text{ V} / -12\text{ V}$ | - | - | ± 100 | nA |
| Zero gate voltage drain current | I_{DSS} | $V_{S1S2} = 25\text{ V}, V_{GS} = 0\text{ V}$ | - | - | 1 | μA |
| | | $V_{S1S2} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$ | - | - | 15 | |
| On-state drain current ^a | $I_{S1S2(on)}$ | $V_{S1S2} \geq 10\text{ V}, V_{GS} = 10\text{ V}$ | 20 | - | - | A |
| Drain-source on-state resistance ^a | $R_{S1S2(on)}$ | $V_{GS} = 10\text{ V}, I_{S1S2} = 7\text{ A}$ | - | 0.0027 | 0.0035 | Ω |
| | | $V_{GS} = 4.5\text{ V}, I_{S1S2} = 5\text{ A}$ | - | 0.0041 | 0.0056 | |
| Forward transconductance ^a | g_{fs} | $V_{S1S2} = 10\text{ V}, I_{S1S2} = 25\text{ A}$ | - | 95 | - | S |
| Dynamic ^{b, c} | | | | | | |
| Input capacitance | C_{iss} | $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | - | 2650 | - | μF |
| Output capacitance | C_{oss} | | - | 940 | - | |
| Reverse transfer capacitance | C_{rss} | | - | 90 | - | |
| Total gate charge | Q_g | $V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$ | - | 37 | 56 | nC |
| | | $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$ | - | 16.9 | 26 | |
| Gate-source charge | Q_{gs} | $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$ | - | 7.6 | - | nC |
| Gate-drain charge | Q_{gd} | | - | 3 | - | |
| Gate resistance | R_g | | $f = 1\text{ MHz}$ | 0.2 | 1.1 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 10\text{ V}, R_L = 2\text{ }\Omega, I_{S1S2} \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$ | - | 12 | 25 | ns |
| Rise time | t_r | | - | 25 | 50 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 26 | 50 | |
| Fall time | t_f | | - | 5 | 10 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 10\text{ V}, R_L = 2\text{ }\Omega, I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$ | - | 24 | 50 | |
| Rise time | t_r | | - | 52 | 100 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 31 | 60 | |
| Fall time | t_f | | - | 9 | 20 | |
| Drain-Source Body Diode Characteristics ^c | | | | | | |
| Continuous source-drain diode current | I_{S1S2} | $T_C = 25\text{ }^\circ\text{C}$ | - | - | 60 | A |
| Pulse diode forward current | I_{S1S2M} | | - | - | 140 | |
| Body diode reverse recovery time | t_{rr} | $I_F = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$ | - | 30 | 60 | ns |
| Body diode reverse recovery charge | Q_{rr} | | - | 19 | 40 | nC |
| Reverse recovery fall time | t_a | | - | 15 | - | ns |
| Reverse recovery rise time | t_b | | - | 15 | - | |

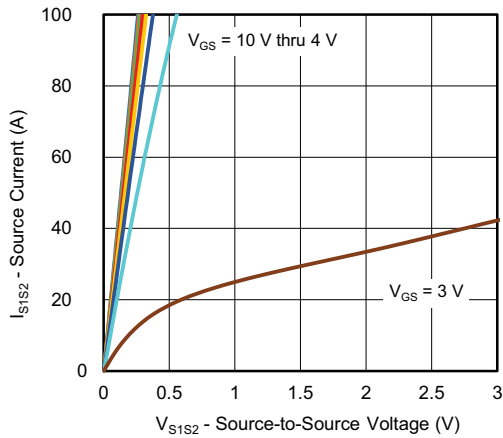
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. On single MOSFET

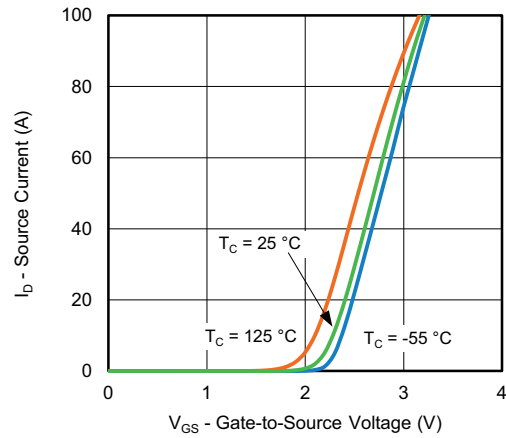
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



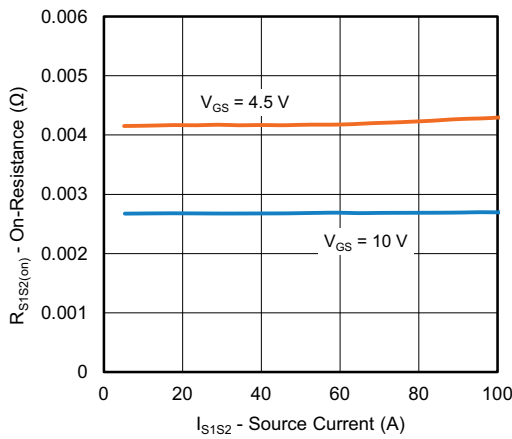
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



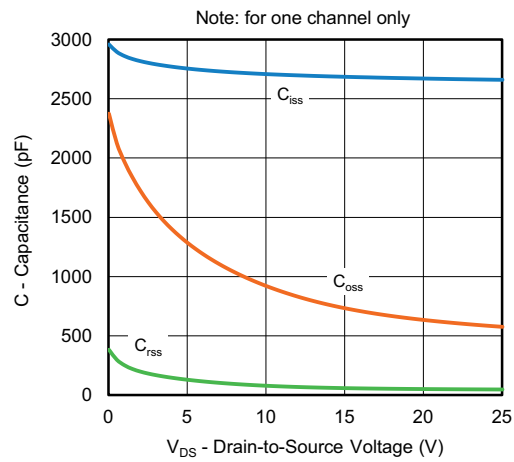
Output Characteristics



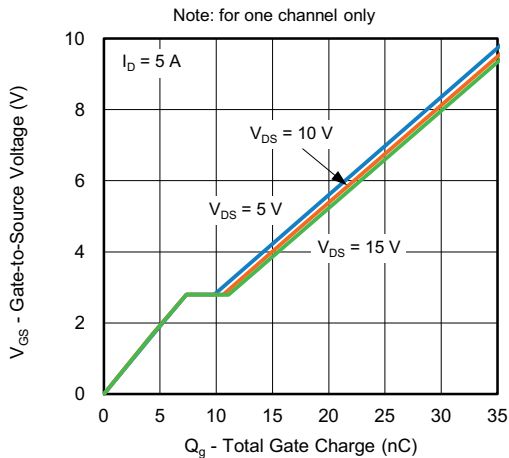
Transfer Characteristics



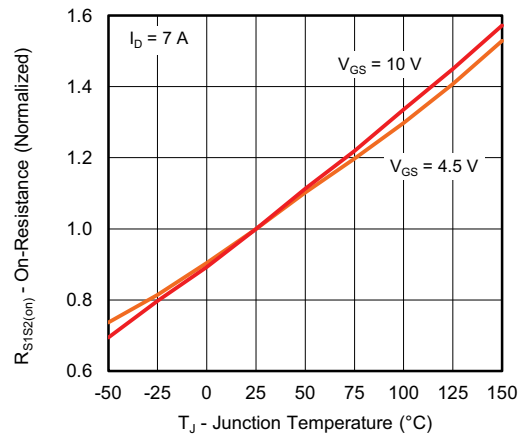
On-Resistance vs. Source Current and Gate Voltage



Capacitance



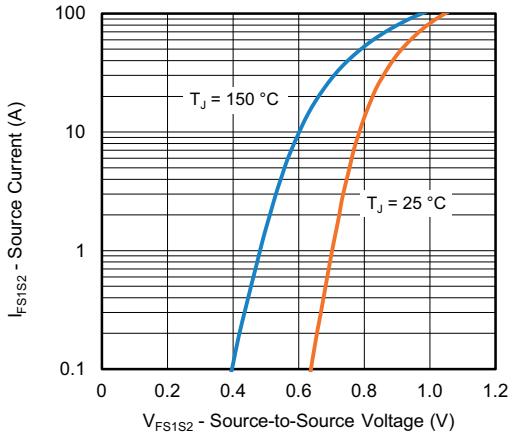
Gate Charge



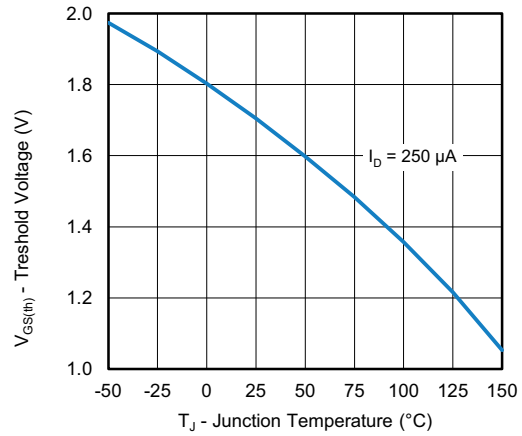
On-Resistance vs. Junction Temperature



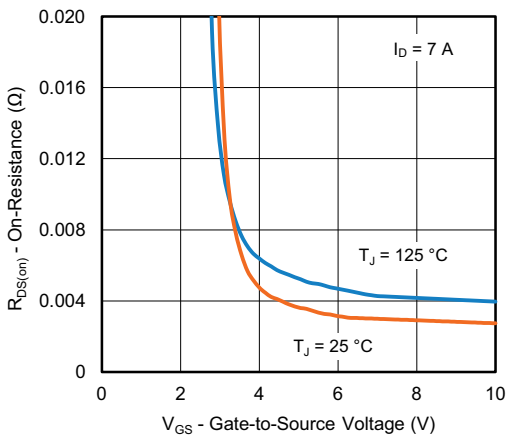
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



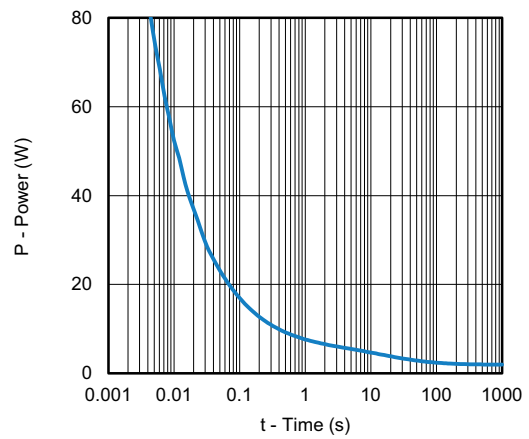
Source-Drain Diode Forward Voltage



Threshold Voltage



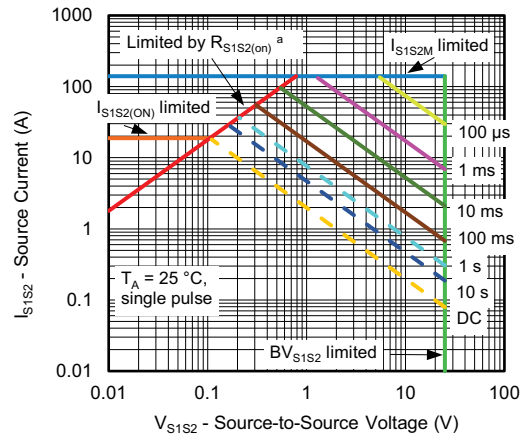
On-Resistance vs. Gate-to-Source Voltage



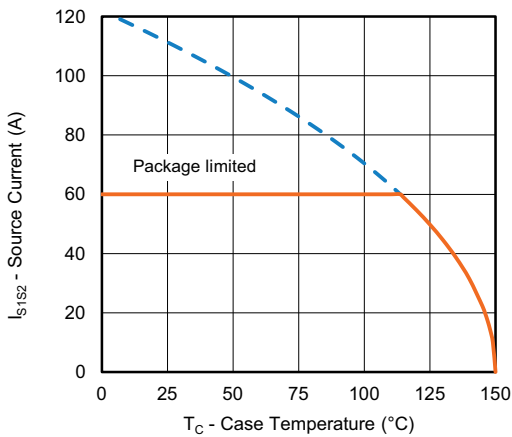
Single Pulse Power, Junction-to-Ambient



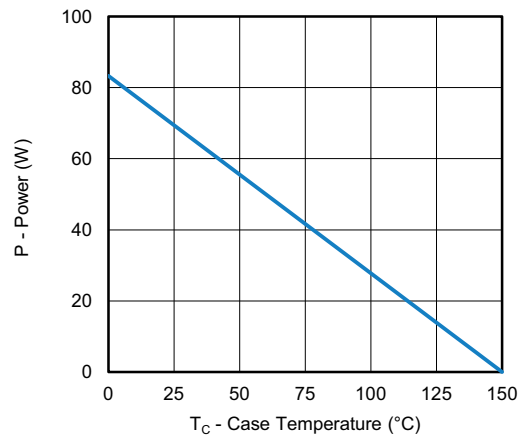
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating ^b



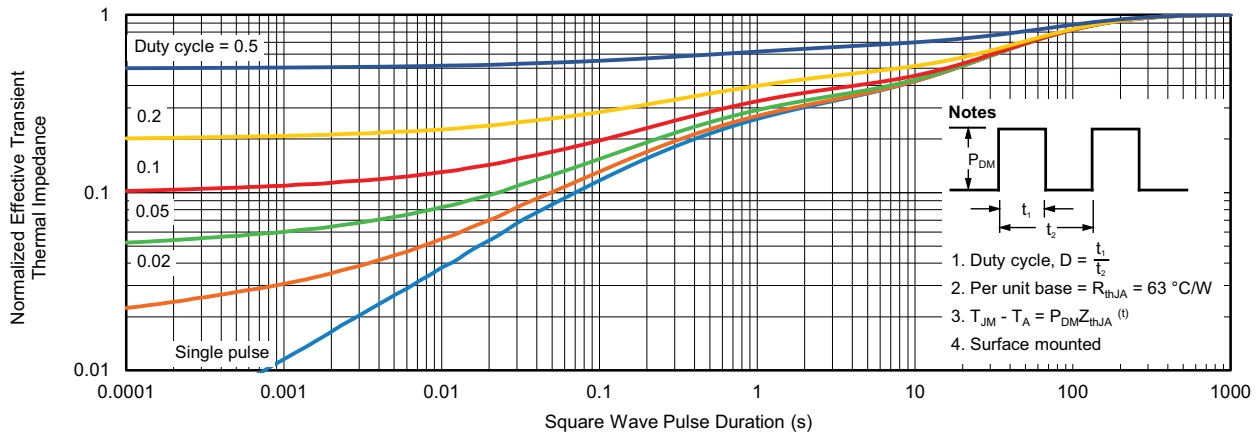
Power, Junction-to-Case

Notes

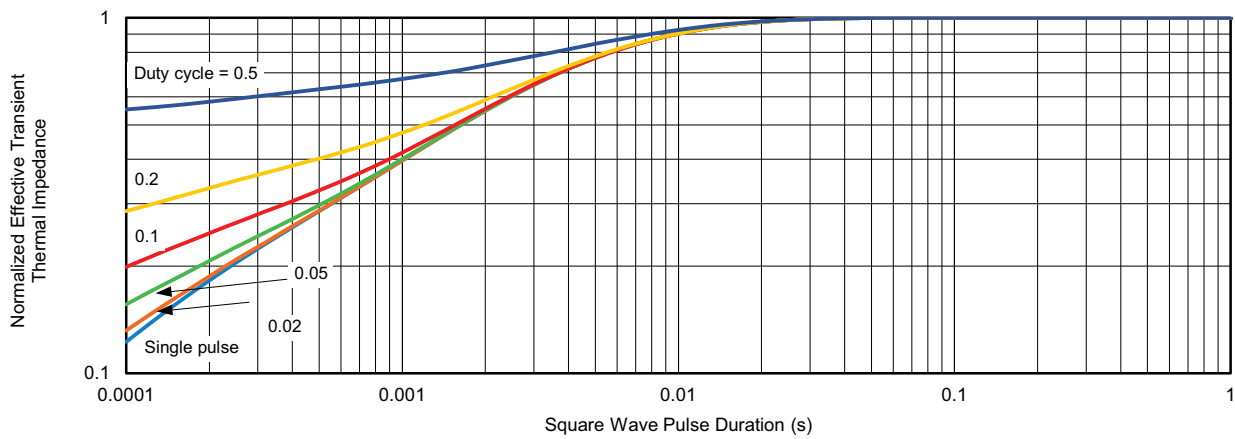
- a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
- b. The power dissipation P_D is based on $T_J \text{ max.} = 150 \text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



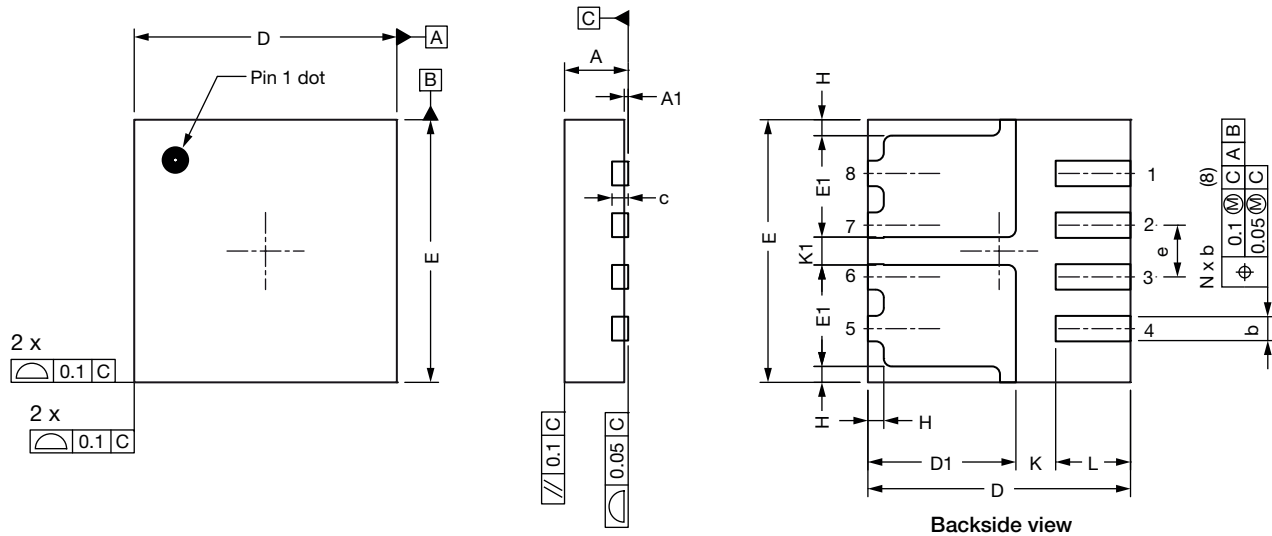
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76933.

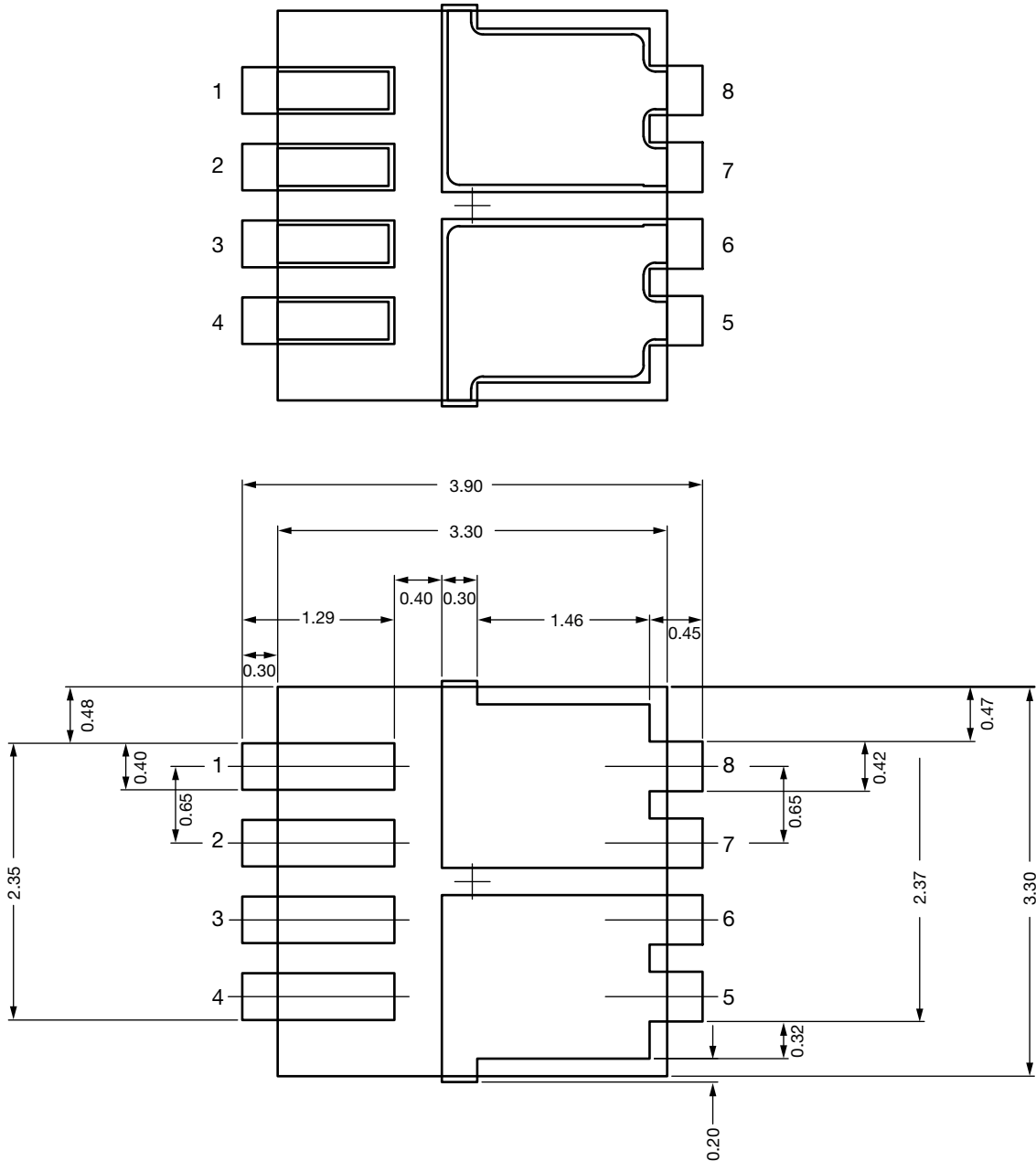
PowerPAK® 1212-8S CD with Flip Chip



| DIM. | MILLIMETERS | | | INCHES | | |
|------|-------------|-----------|------|------------|------------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.027 | 0.029 | 0.031 |
| A1 | 0 | 0.02 | 0.05 | 0 | 0.001 | 0.002 |
| b | 0.27 | 0.32 | 0.37 | 0.011 | 0.013 | 0.015 |
| c | - | 0.20 ref. | - | - | 0.008 ref. | - |
| D | 3.20 | 3.30 | 3.40 | 0.126 | 0.130 | 0.134 |
| D1 | 1.76 | 1.86 | 1.96 | 0.069 | 0.073 | 0.077 |
| E | 3.20 | 3.30 | 3.40 | 0.126 | 0.130 | 0.134 |
| E1 | 1.18 | 1.28 | 1.38 | 0.046 | 0.050 | 0.054 |
| e | 0.60 | 0.65 | 0.70 | 0.024 | 0.026 | 0.028 |
| K | 0.50 typ. | | | 0.020 typ. | | |
| K1 | 0.35 typ. | | | 0.014 typ. | | |
| H | 0.10 | 0.20 | 0.30 | 0.006 | 0.008 | 0.010 |
| L | 0.84 | 0.94 | 1.04 | 0.033 | 0.037 | 0.041 |

ECN: C17-1732-Rev. A, 18-Dec-17
DWG: 6061

Recommended Land Pattern PowerPAK® 1212-8S CD





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