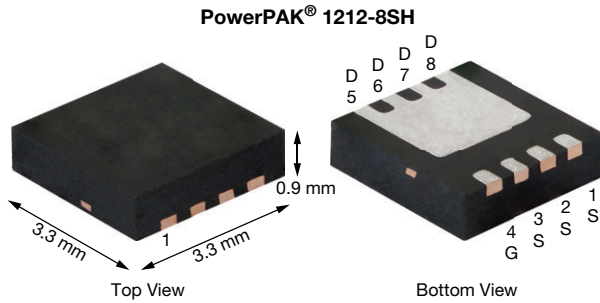


P-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.0123
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.0222
Q_g typ. (nC)	20.5
I_D (A) ^{d, g}	-35
Configuration	Single

FEATURES

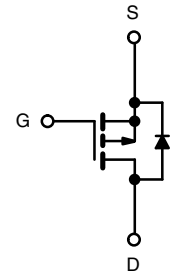
- TrenchFET[®] power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Notebook battery charging
- Notebook adapter switch



P-Channel MOSFET

ORDERING INFORMATION

Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH617DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-30	V
Gate-source voltage	V_{GS}	± 25	V
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	-35 ^d
		$T_C = 70$ °C	-35 ^d
		$T_A = 25$ °C	-13.9 ^{a, b}
		$T_A = 70$ °C	-11.1 ^{a, b}
Pulsed drain current	I_{DM}	-60	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	-35 ^d
		$T_A = 25$ °C	-3 ^{a, b}
Avalanche current	I_{AS}	-29	A
Single-pulse avalanche energy	E_{AS}	42	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	52
		$T_C = 70$ °C	33
		$T_A = 25$ °C	3.7 ^{a, b}
		$T_A = 70$ °C	2.4 ^{a, b}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{e, f}		260	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, c}	R_{thJA}	26	33	°C/W
Maximum junction-to-case	R_{thJC}	1.9	2.4	

Notes

- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- Maximum under steady state conditions is 81 °C/W
- Package limited
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Based on $T_C = 25$ °C

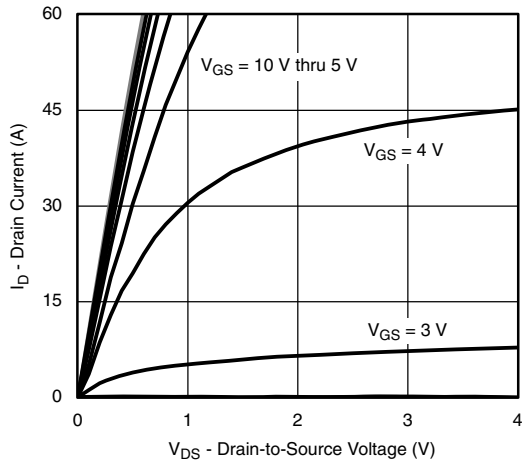
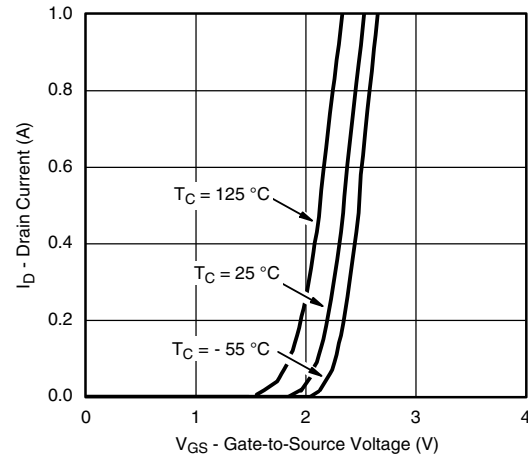
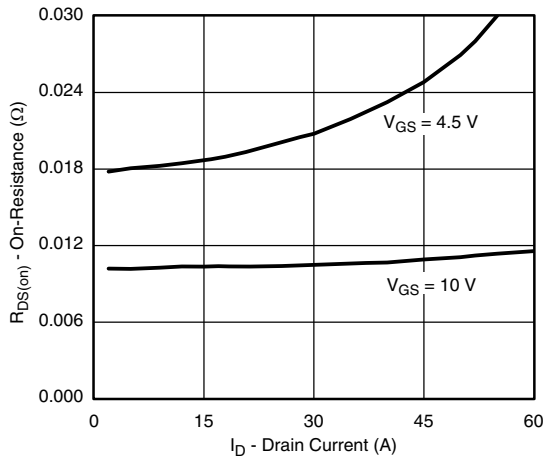
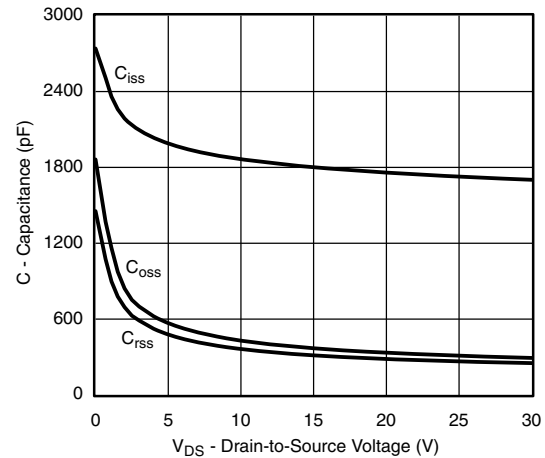
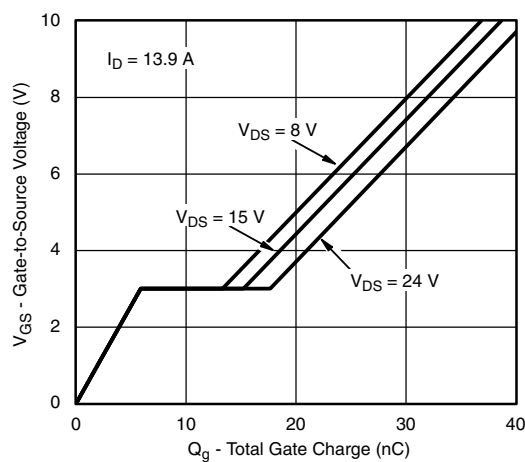
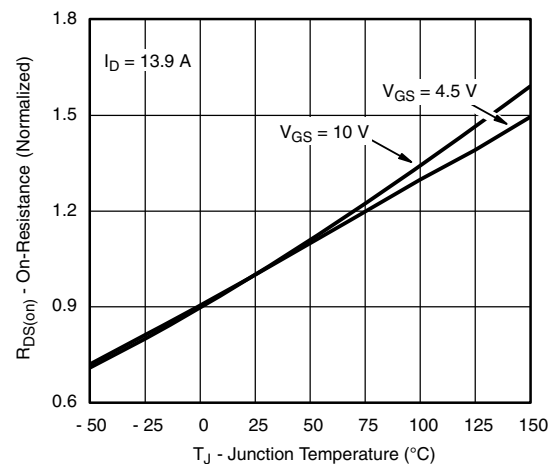


SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$	-	-25	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	4.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.2	-	-2.5	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	-5	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$	-30	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -13.9\text{ A}$	-	0.0103	0.0123	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -10.3\text{ A}$	-	0.0185	0.0222	
Forward transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -13.9\text{ A}$	-	35	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1800	-	pF
Output capacitance	C_{oss}		-	370	-	
Reverse transfer capacitance	C_{rss}		-	312	-	
Total gate charge	Q_g	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -13.9\text{ A}$	-	39	59	nC
		$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -13.9\text{ A}$	-	20.5	31	
Gate-source charge	Q_{gs}	$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -13.9\text{ A}$	-	6	-	
Gate-drain charge	Q_{gd}		-	11	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.4	2	4	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.35\text{ }\Omega$ $I_D \cong -11.1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$	-	11	22	ns
Rise time	t_r		-	9	18	
Turn-off delay time	$t_{d(off)}$		-	32	50	
Fall time	t_f		-	9	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.35\text{ }\Omega$ $I_D \cong -11.1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	-	40	60	ns
Rise time	t_r		-	43	65	
Turn-off delay time	$t_{d(off)}$		-	30	45	
Fall time	t_f		-	11	22	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	-35	A
Pulse diode forward current	I_{SM}		-	-	-60	
Body diode voltage	V_{SD}	$I_S = -11.1\text{ A}, V_{GS} = 0\text{ V}$	-	-0.8	-1.2	V
Body diode reverse recovery time	t_{rr}	$I_F = -11.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	33	50	ns
Body diode reverse recovery charge	Q_{rr}		-	30	45	nC
Reverse recovery fall time	t_a		-	18	-	ns
Reverse recovery rise time	t_b		-	16	-	

Notes

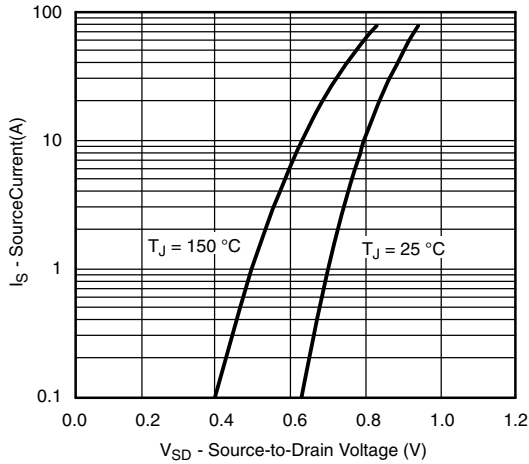
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

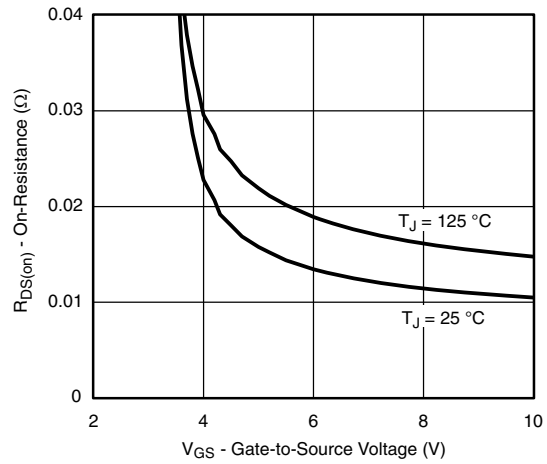
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



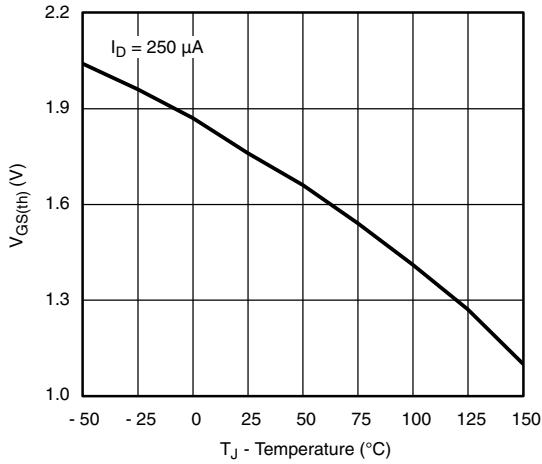
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



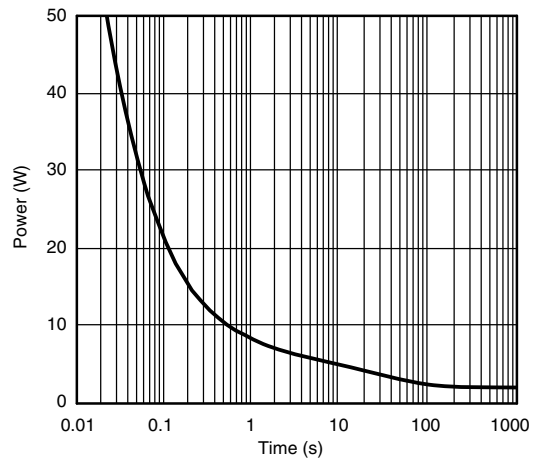
Source-Drain Diode Forward Voltage



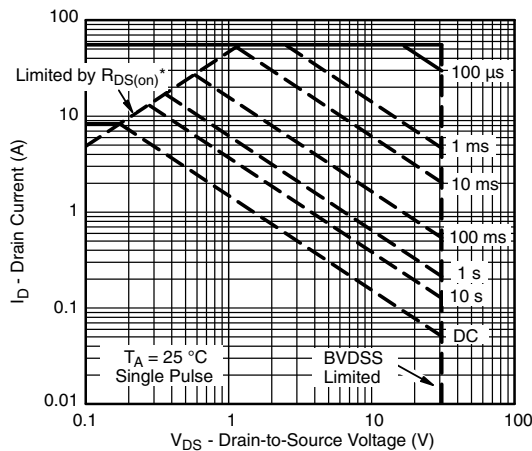
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



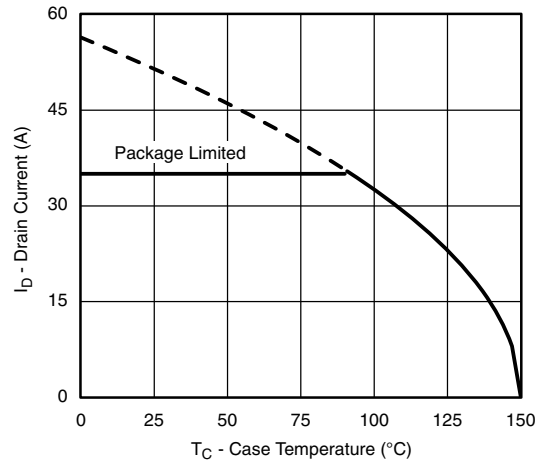
Single Pulse Power, Junction-to-Ambient



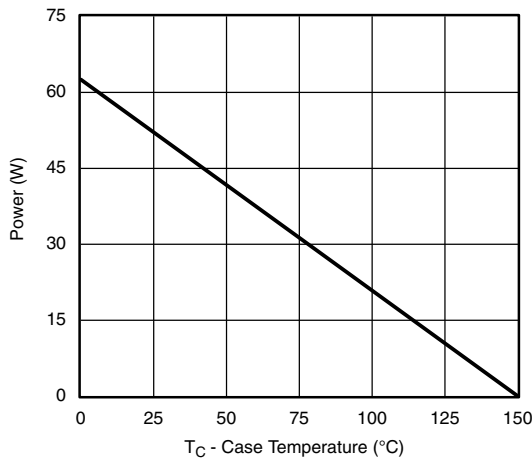
Safe Operating Area



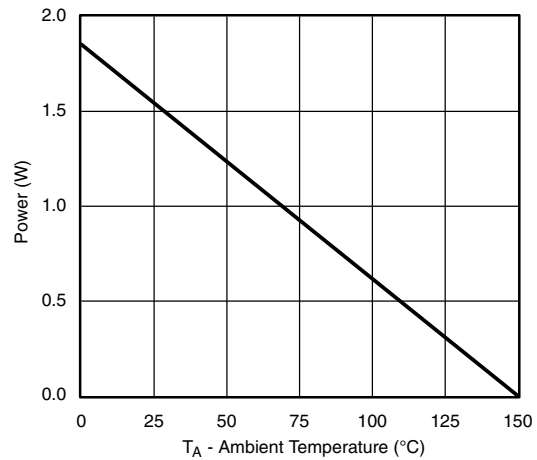
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating^a



Power Derating, Junction-to-Case



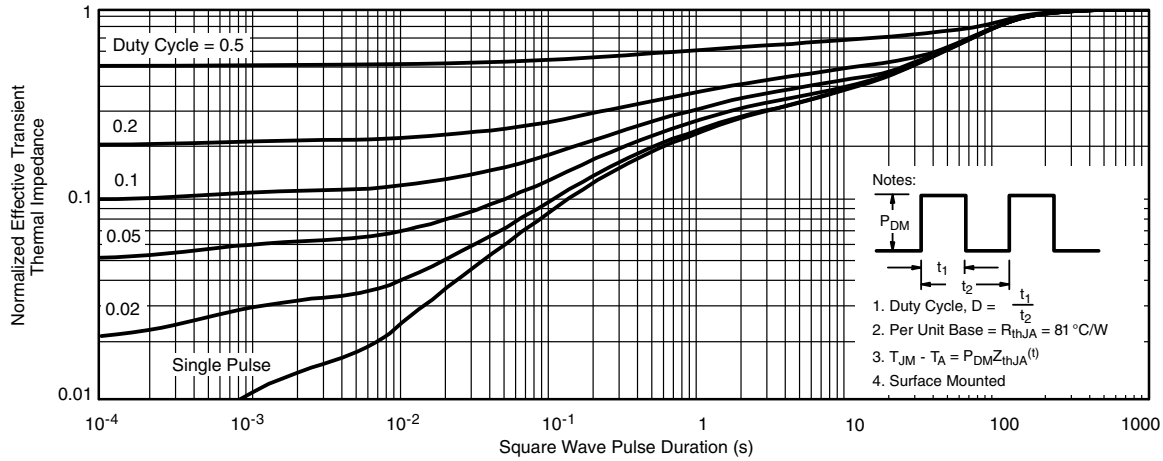
Power Derating, Junction-to-Ambient

Note

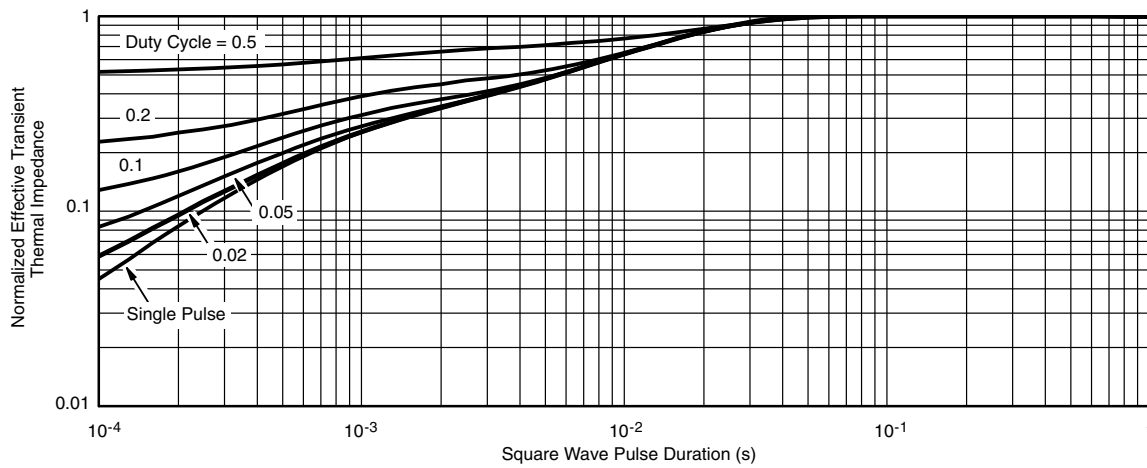
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



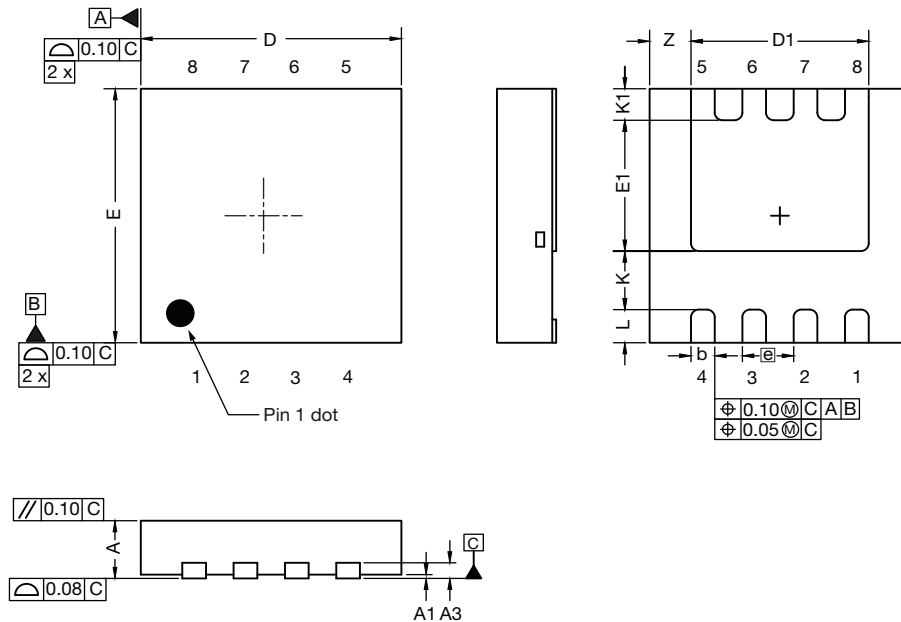
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75900.

Case Outline for PowerPAK[®] 1212-SWLH and PowerPAK[®] 1212-8SH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		
ECN: S20-0930-Rev. C, 07-Dec-2020						
DWG: 6062						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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