NCV8775C

Ultra Low I_q 350 mA LDO Regulator with Reset

The NCV8775C is 350 mA LDO regulator with integrated reset functions dedicated for microprocessor applications. Its robustness allows NCV8775C to be used in severe automotive environments. Ultra low quiescent current as low as 19 μA typical makes it suitable for applications permanently connected to battery requiring ultra low quiescent current with or without load. This feature is especially critical when modules remain in active mode when ignition is off. The NCV8775C contains protection functions as current limit, thermal shutdown.

Features

- Output Voltage Options: 3.3 V and 5 V
- Output Voltage Accuracy: ±2%
- Output Current up to 350 mA
- Ultra Low Quiescent Current: typ 19 μA (max 28 μA)
- Very Wide Range of C_{out} and ESR Values for Stability
- Microprocessor Compatible Control Functions:
  - Reset with Adjustable Delay
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features
  - Current Limitation
  - Thermal Shutdown
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Grade 1 Qualified and PPAP Capable
- EMC Compliant
- These are Pb−Free Devices

Typical Applications

- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain

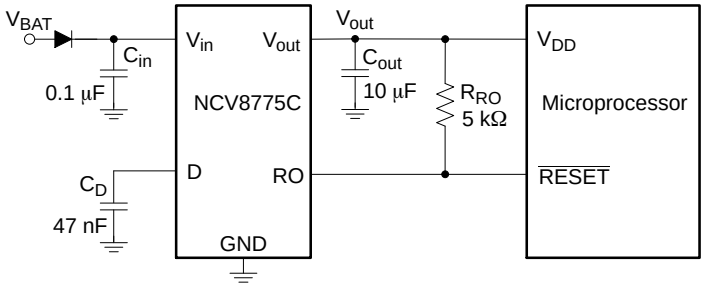

Figure 1. Typical Application Schematic

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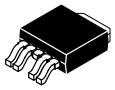
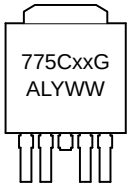
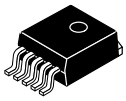
MARKING DIAGRAMS



DPAK−5
DT SUFFIX
CASE 175AA





D²PAK−5
D5S SUFFIX
CASE 936A

xx	= 50 (5.0 V Version) 33 (3.3 V Version)
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

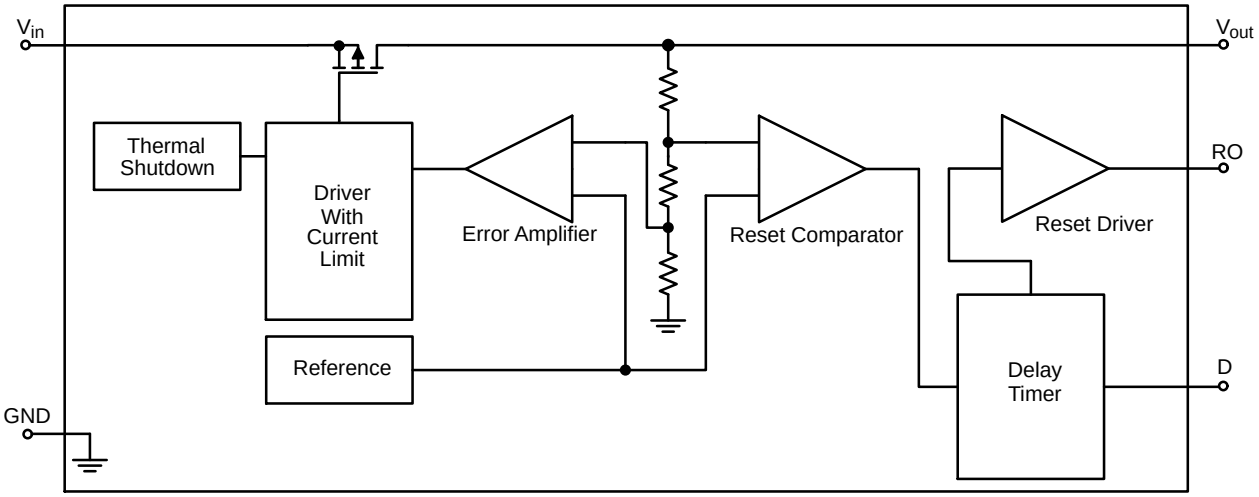


Figure 2. Simplified Block Diagram

PIN CONNECTIONS

Figure 3. Pin Connections

PIN FUNCTION DESCRIPTION

Pin No. DPAK−5 D2PAK−5	Pin Name	Description
1	V_{in}	Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
2	RO	Reset (Open Collector) Output. External Pull−up resistor connected to V_{out}.
3, TAB	GND	Power Supply Ground. Pin 3 internally connected to tab.
4	D	Reset Delay. Timing capacitor to GND for Reset Delay function.
5	V_{out}	Regulated Output Voltage. Connect 10 μF capacitor with ESR < 5 Ω to ground.

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Min	Max	Unit
Input Voltage (Note 1)	DC	V_{in}	−0.3	40	V
Input Voltage (Note 2)	Load Dump − Suppressed	U_s*	−	45	V
Output Voltage		V_{out}	−0.3	7	V
Reset Delay Voltage		V_D	−0.3	7	V
Reset Output Voltage		V_{RO}	−0.3	7	V
Junction Temperature		T_J	−40	150	°C
Storage Temperature		T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−4	4	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1	1	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (JS−001−2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating		Symbol	Min	Max	Unit
Moisture Sensitivity Level	DPAK−5 D2PAK−5	MSL	1 1		−

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS (Note 5)

Rating	Symbol	Value	Unit
Thermal Characteristics, DPAK−5			°C/W
Thermal Resistance, Junction−to−Air (Note 6)	$R_{\theta JA}$	53.5	
Thermal Reference, Junction−to−Lead (Note 6)	$R_{\psi JL1}$	8.2	
Thermal Resistance, Junction−to−Air (Note 7)	$R_{\theta JA}$	23.9	
Thermal Reference, Junction−to−Lead (Note 7)	$R_{\psi JL1}$	7.4	
Thermal Characteristics, D2PAK−5			°C/W
Thermal Resistance, Junction−to−Air (Note 6)	$R_{\theta JA}$	53.3	
Thermal Reference, Junction−to−Lead (Note 6)	$R_{\psi JL1}$	7.6	
Thermal Resistance, Junction−to−Air (Note 7)	$R_{\theta JA}$	23.7	
Thermal Reference, Junction−to−Lead (Note 7)	$R_{\psi JL1}$	6.9	

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
6. Values based on 1s0p board with copper area of 645 mm2 (or 1 in2) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3.
7. Values based on 2s2p board with copper area of 645 mm2 (or 1 in2) of 1 oz copper thickness for inner layers, 2 oz copper thickness for signal layers and FR4 PCB substrate. 4 layers − according to JEDEC51.7.

RECOMMENDED OPERATING RANGE (Note 8)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 9)	V_{in}	4.5	40	V
Junction Temperature	T_J	−40	150	°C

8. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
9. Minimum V_{in} = 4.5 V or (V_{out} + V_{DO}), whichever is higher.

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, C_{in} = 0.1 μF, C_{out} = 10 μF, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C (Notes 10 and 11)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage (Accuracy %) 3.3 V 5.0 V 	 V_{in} = 4.5 V to 40 V, I_{out} = 0.1 mA to 200 mA V_{in} = 4.5 V to 16 V, I_{out} = 0.1 mA to 350 mA V_{in} = 5.6 V to 40 V, I_{out} = 0.1 mA to 200 mA V_{in} = 5.975 V to 16 V, I_{out} = 0.1 mA to 350 mA	V_{out}	 3.234 3.234 4.9 4.9	 3.3 3.3 5.0 5.0	 3.366 3.366 5.1 5.1	V
Line Regulation 3.3 V 5.0 V	 V_{in} = 4.5 V to 28 V, I_{out} = 5 mA V_{in} = 6 V to 28 V, I_{out} = 5 mA	Reg_{line}	−20	0	20	mV
Load Regulation	I_{out} = 0.1 mA to 350 mA	Reg_{load}	−35	10	35	mV
Dropout Voltage (Note 12) 5.0 V 	 I_{out} = 200 mA I_{out} = 350 mA	V_{DO}	 – –	 200 350	 350 600	mV
QUIESCENT CURRENT						
Quiescent Current ($I_q = I_{in} - I_{out}$)	 I_{out} = 0.1 mA, T_J = 25°C I_{out} = 0.1 mA, T_J ≤ 125°C	I_q	 – –	 19 –	 27 28	μA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.96 x V_{out_nom}	I_{LIM}	500	–	1100	mA
Short Circuit Current Limit	V_{out} = 0 V	I_{SC}	500	–	1100	mA
PSRR						
Power Supply Ripple Rejection (Note 13)	f = 100 Hz, 0.5 V_{pp}	PSRR	–	80	–	dB
D (RESET DELAY)						
Reset Charging Current	V_D = 1.0 V	I_D	2.0	4.0	6.5	μA
Upper Timing Threshold		V_{DU}	1.2	1.3	1.4	V
Reset Delay Time	C_D = 47 nF	t_{RD}	10	16	22	ms
Reset Reaction Time		t_{RR}		6.0		μs
RESET OUTPUT RO						
Input Voltage Reset Threshold 3.3 V	V_{in} decreasing, V_{out} > V_{RT}	V_{in_RT}	 –	 3.8	 4.2	V
Output Voltage Reset Threshold	V_{out} decreasing	V_{RT}	90	93	96	%V_{out}
Reset Hysteresis		V_{RH}	–	2.0	–	%V_{out}
Reset Output Low Voltage	V_{out} > 1 V, R_{RO} > 5 kΩ	V_{ROL}	–	0.2	0.4	V
Reset High Level Leakage Current		I_{ROLK}	–	–	5	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 13)		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis (Note 13)		T_{SH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
11. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
12. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.5 V.
13. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

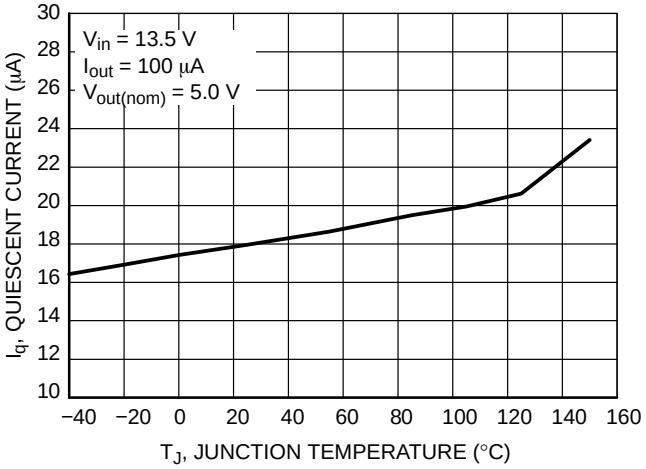


Figure 4. Quiescent Current vs. Junction Temperature

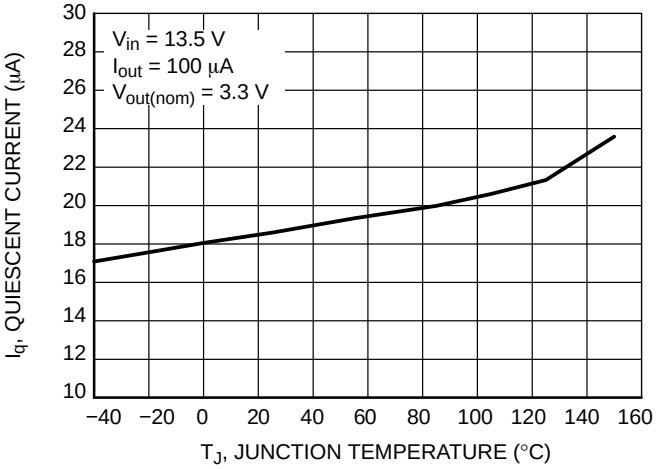


Figure 5. Quiescent Current vs. Junction Temperature

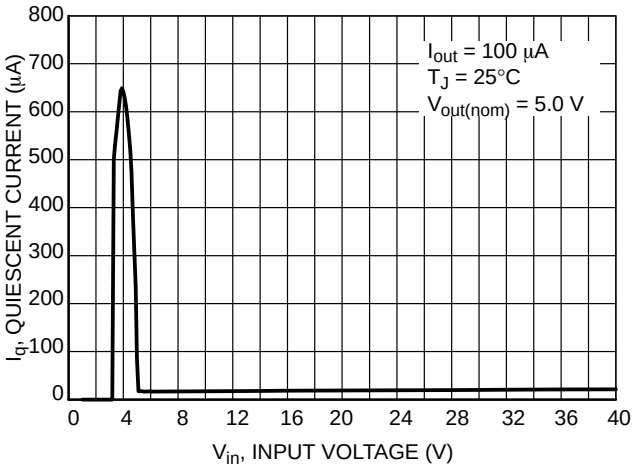


Figure 6. Quiescent Current vs. Input Voltage

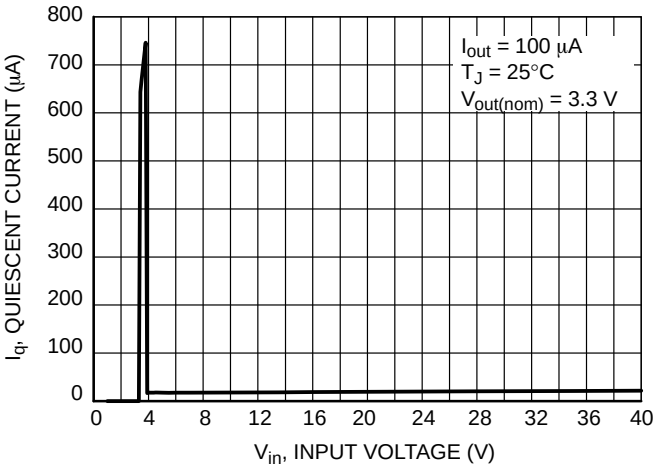


Figure 7. Quiescent Current vs. Input Voltage

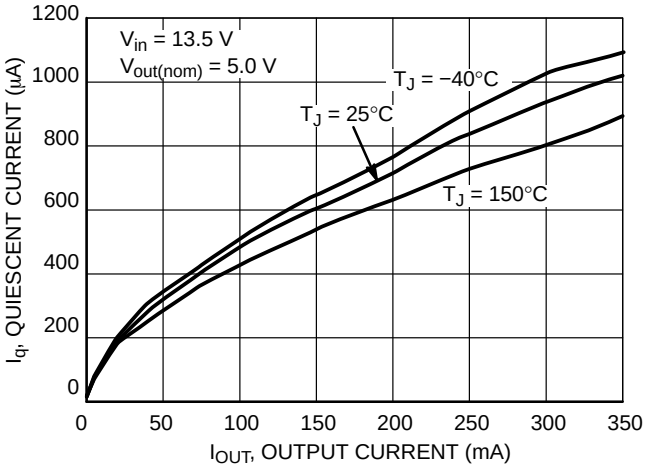


Figure 8. Quiescent Current vs. Output Current

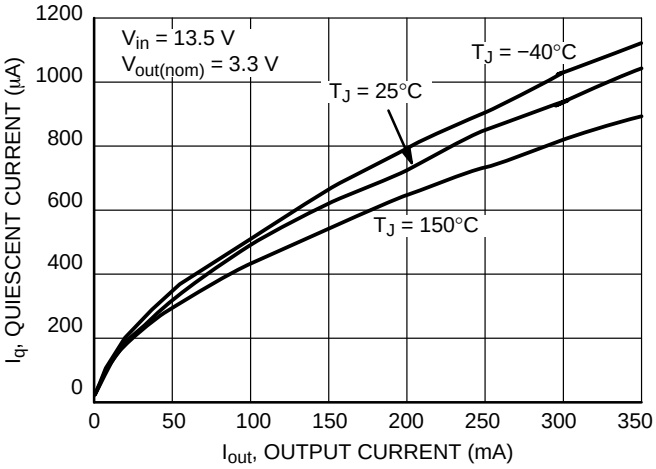


Figure 9. Quiescent Current vs. Output Current

TYPICAL CHARACTERISTICS

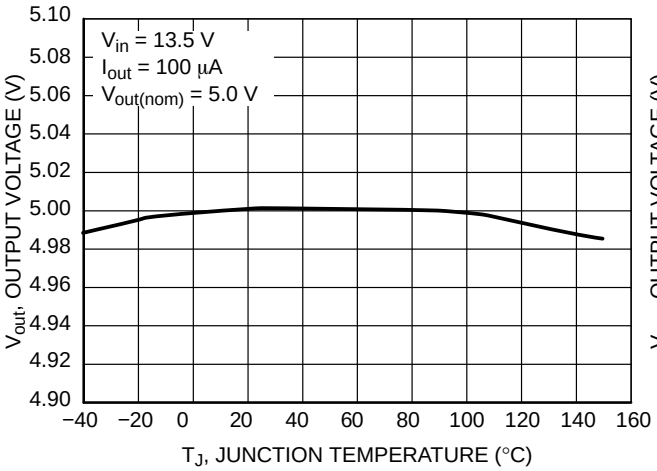


Figure 10. Output Voltage vs. Junction Temperature

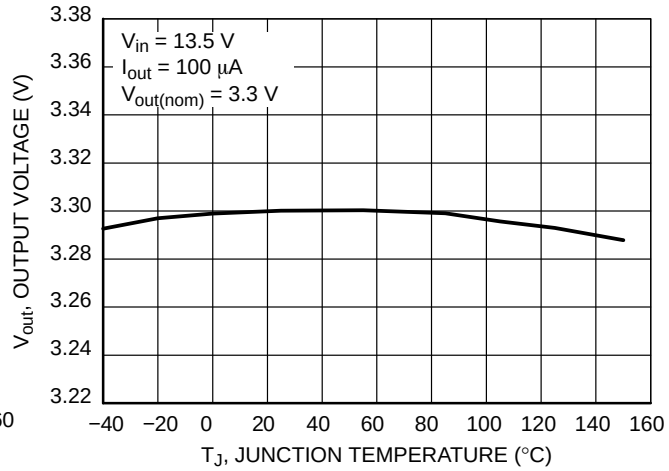


Figure 11. Output Voltage vs. Junction Temperature

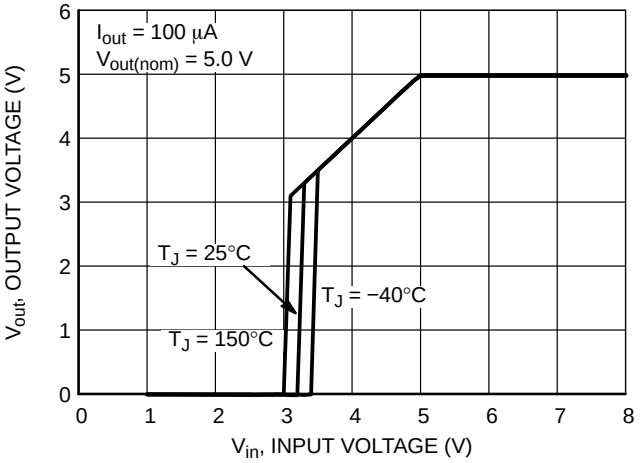


Figure 12. Output Voltage vs. Input Voltage

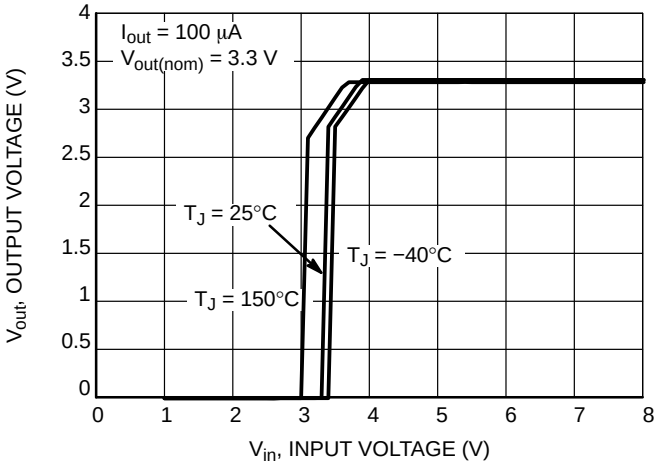


Figure 13. Output Voltage vs. Input Voltage

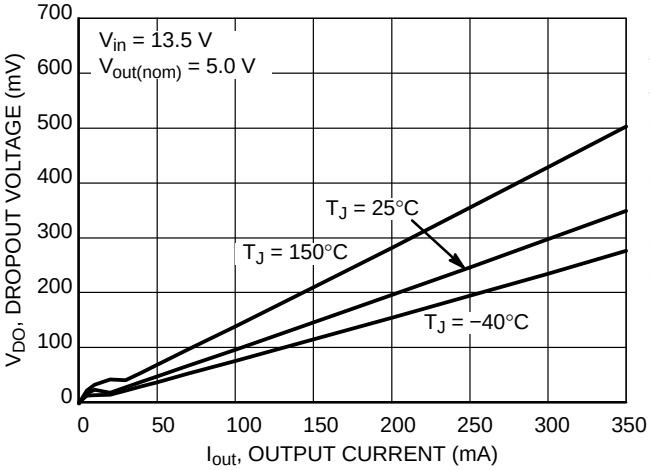


Figure 14. Dropout Voltage vs. Output Current

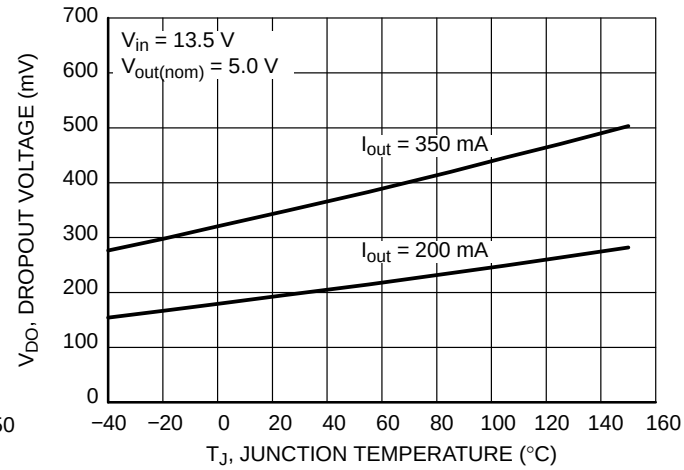


Figure 15. Dropout Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

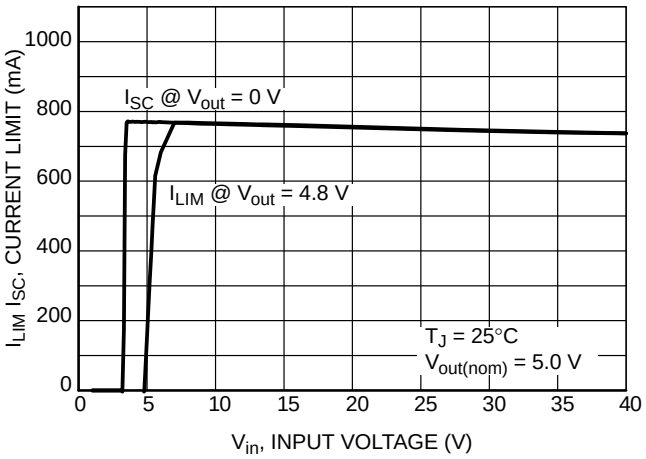


Figure 16. Output Current Limit vs. Input Voltage

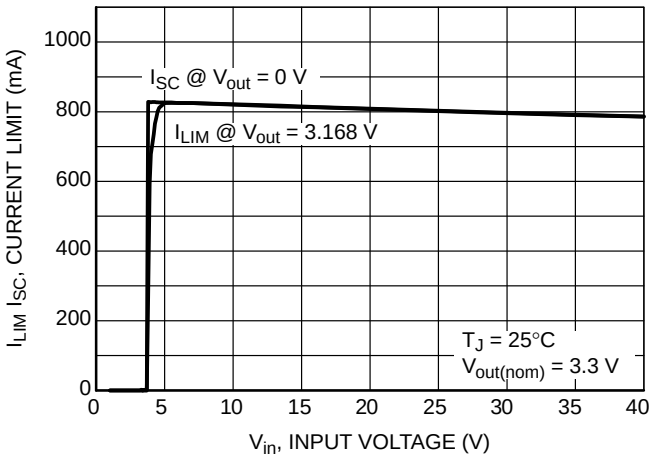


Figure 17. Output Current Limit vs. Input Voltage

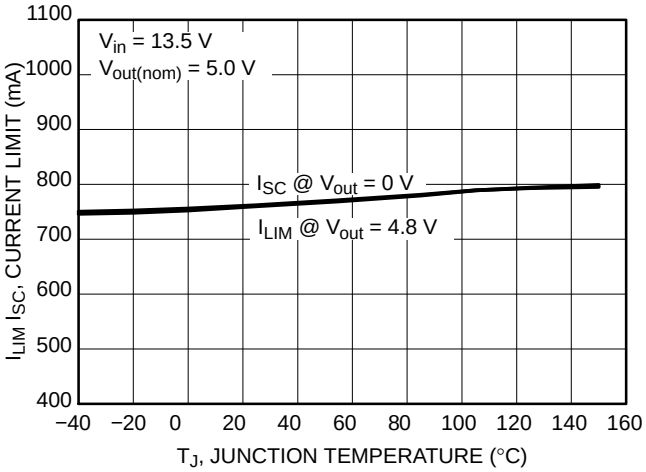


Figure 18. Output Current Limit vs. Junction Temperature

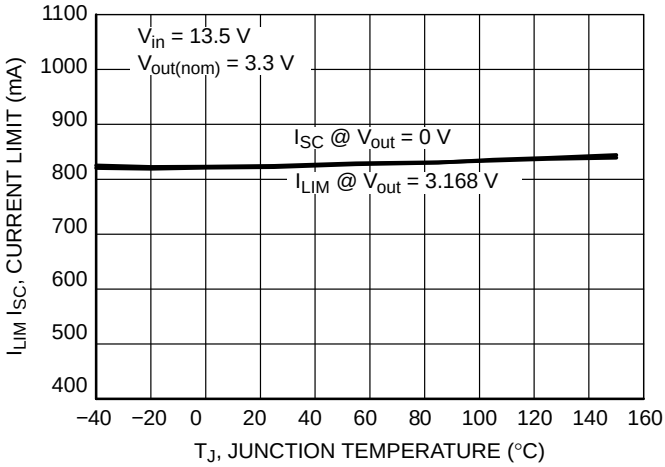


Figure 19. Output Current Limit vs. Junction Temperature

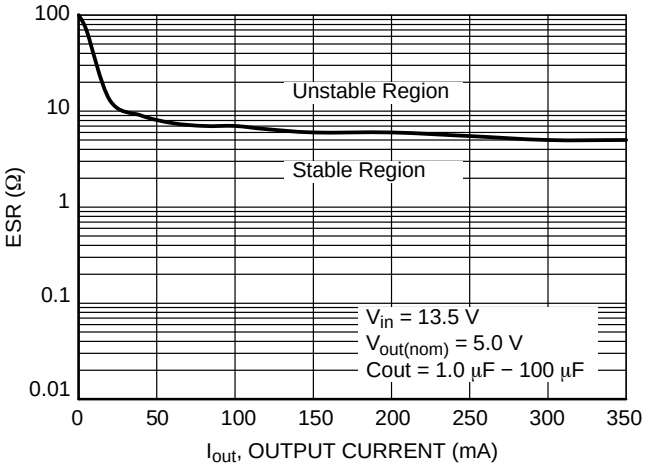


Figure 20. Output Stability with Output Capacitor ESR

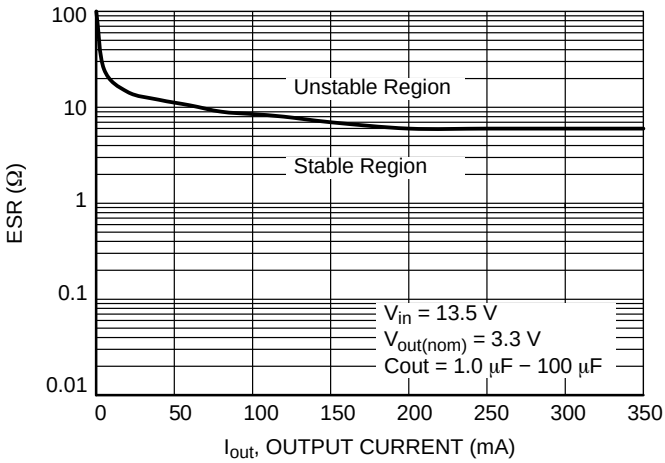


Figure 21. Output Stability with Output Capacitor ESR

TYPICAL CHARACTERISTICS

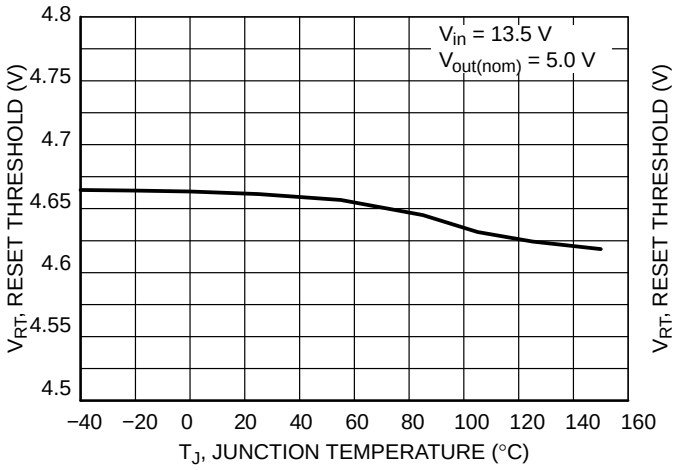


Figure 22. Reset Threshold vs. Junction Temperature

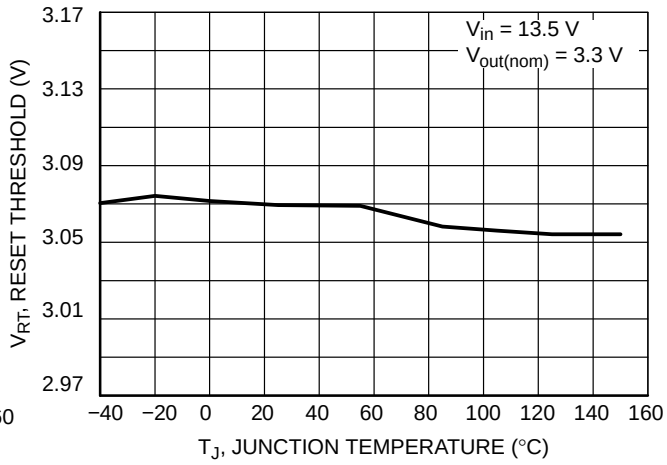


Figure 23. Reset Threshold vs. Junction Temperature

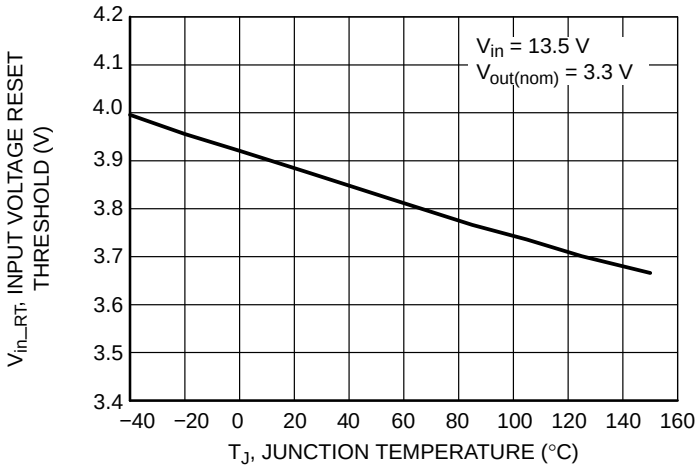


Figure 24. Input Voltage Reset Threshold vs. Junction Temperature

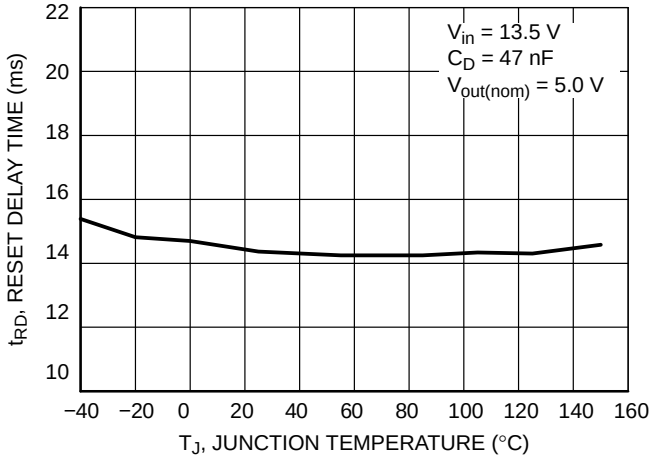


Figure 25. Reset Delay Time vs. Junction Temperature

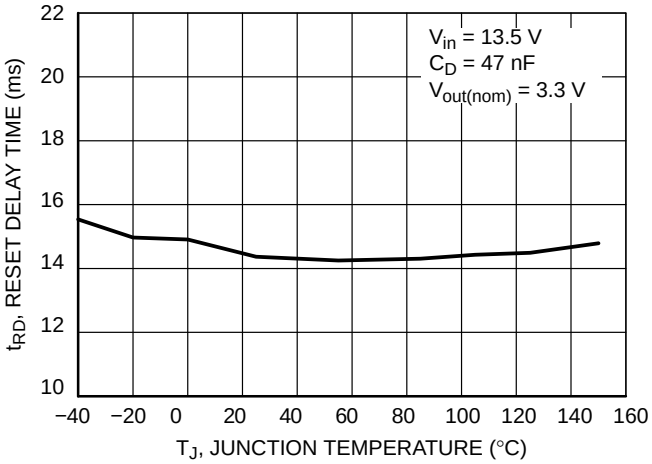


Figure 26. Reset Delay Time vs. Junction Temperature

TYPICAL CHARACTERISTICS

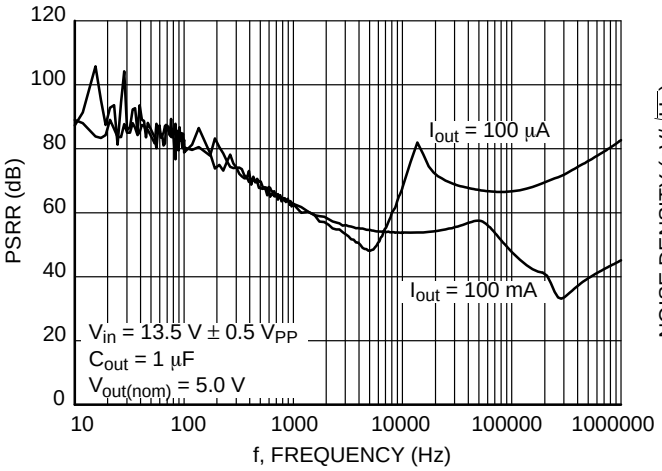


Figure 27. PSRR vs. Frequency

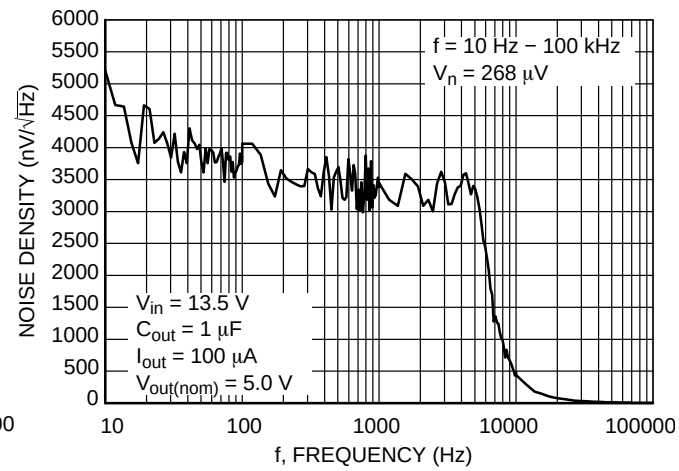


Figure 28. Noise vs. Frequency

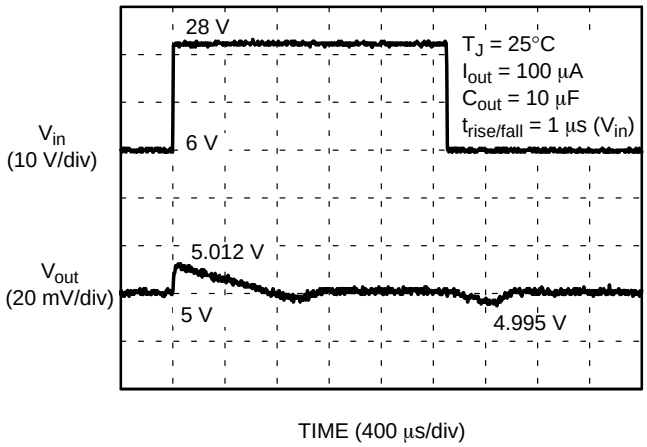


Figure 29. Line Transients

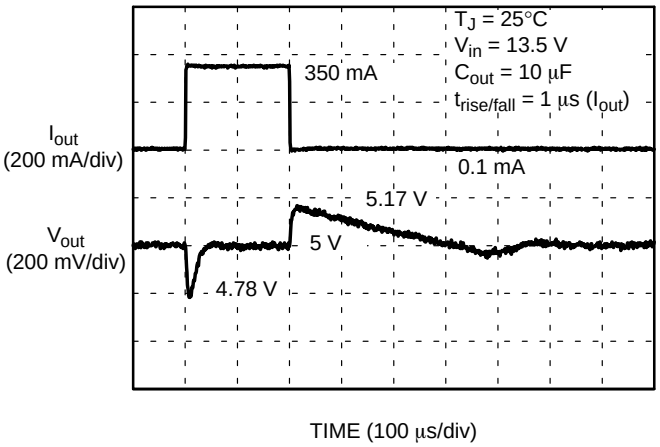


Figure 30. Load Transients

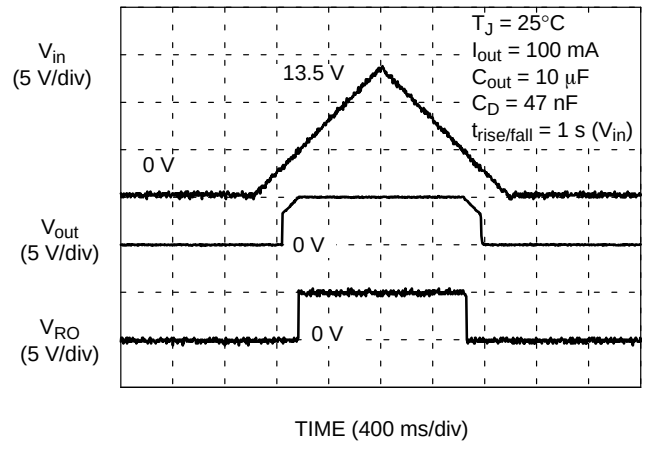


Figure 31. Power Up/Down Response

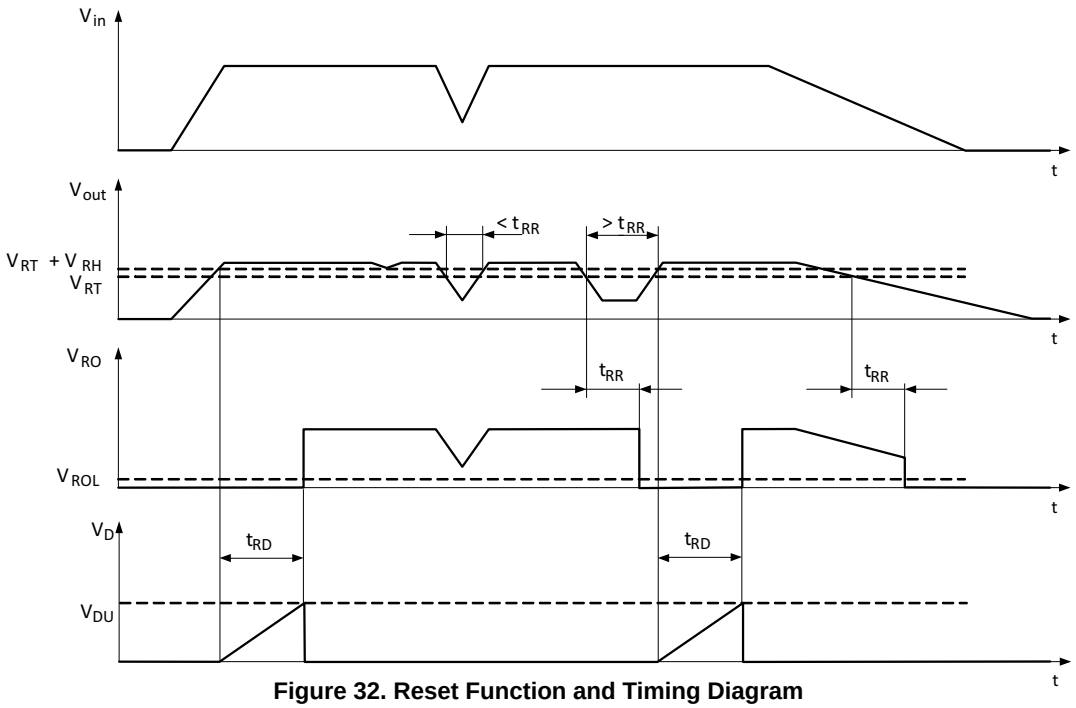


Figure 32. Reset Function and Timing Diagram

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent Current

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current.

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8775C regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figure 4 to Figure 34.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8775C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

Input Capacitor is required if regulator is located far from power supply filter. If extremely fast input voltage transients are expected with slew rate in excess of 4 V/μs then appropriate input filter must be used. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The NCV8775C is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs Output Current is shown in Figures 20 and 21. The minimum output decoupling value is 1 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

Reset Operation

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 32. This is in the form of a logic signal on RO. Output voltage conditions below the Reset threshold cause RO to go low. RO is pulled up to V_{out} by an external resistor, typically 5.0 kΩ in value. Output voltage regulation must be maintained for the delay time before the reset output signals a valid condition. The delay for the reset output is defined as the amount of time it takes the timing capacitor on the delay pin to charge from a residual voltage of 0 V to the upper timing threshold voltage V_{DU} of 1.3 V. The charging current for this is I_D of 4 μA and D pin voltage in steady state is typically 0 V. By using typical IC parameters with a 47 nF capacitor on the D Pin, the following time delay is derived:

$$t_{RD} = C_D \times \frac{V_{DU}}{I_D} \qquad \text{(eq. 1)}$$

$$t_{RD} = 47\ \text{nF} \times \frac{1.3\ \text{V}}{4\ \mu\text{A}} = 15.3\ \text{ms}$$

Other time delays can be obtained by changing the C_D capacitor value. The Delay Time can be reduced by decreasing the capacitance of C_D. Using the formula above, Delay can be reduced as desired. For minimum reset delay time Delay pin must be left open with no PCB trace connected to the pin.

Thermal Considerations

As power in the NCV8775C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8775C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8775C can handle is given by:

$$P_{D(max)} = \frac{\left[T_{J(max)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 2)}$$

Since T_J is not recommended to exceed 150°C, then the NCV8775C soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 2.35 W (for D2PAK−5) when the ambient temperature (T_A) is 25°C. See Figures 33 and 34 for $R_{\theta JA}$ versus PCB area. The power dissipated by the NCV8775C can be calculated from the following equations:

$$P_D = V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 3)}$$

or

$$V_{in(max)} = \frac{P_{D(max)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 4)}$$

NOTE: Items containing I_q can be neglected if $I_{out} >> I_q$.

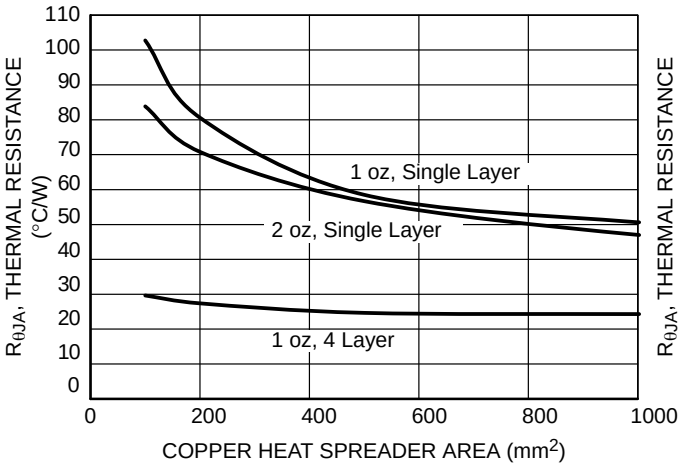


Figure 33. Thermal Resistance vs. PCB Copper Area (DPAK−5)

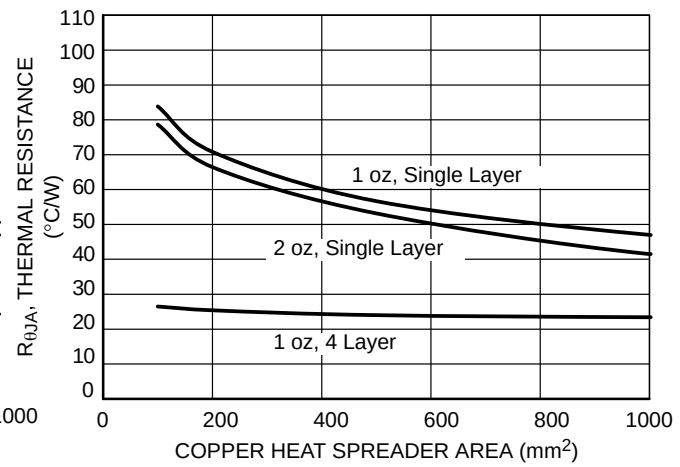


Figure 34. Thermal Resistance vs. PCB Copper Area (D2PAK−5)

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external filter components, especially the output capacitor, as near as possible to the device to increase EMC performance.

The NCV8775C is not developed in compliance with ISO26262 standard. If application is safety critical then the above application example diagram shown in Figure 35 can be used.

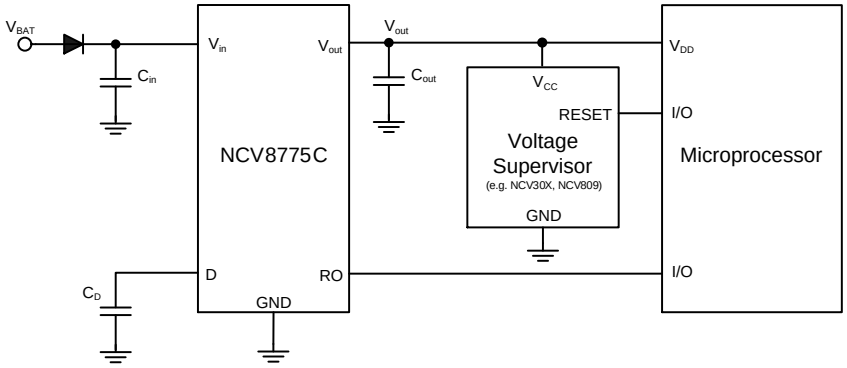


Figure 35. NCV8775C Application Diagram

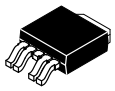
ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV8775CDT33RKG	3.3 V	DPAK−5 (Pb−Free)	2500 / Tape & Reel
NCV8775CDT50RKG	5.0 V	DPAK−5 (Pb−Free)	2500 / Tape & Reel
NCV8775CDS33R4G	3.3 V	D2PAK−5 (Pb−Free)	800 / Tape & Reel
NCV8775CDS50R4G	5.0 V	D2PAK−5 (Pb−Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

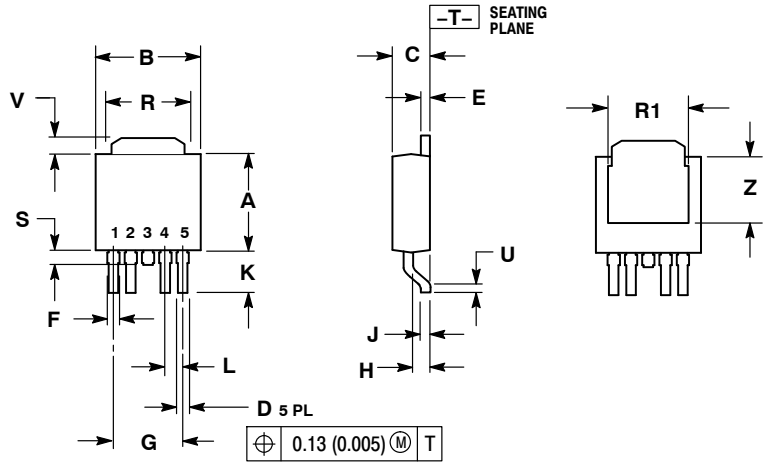
ON Semiconductor®



DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

DATE 15 MAY 2014

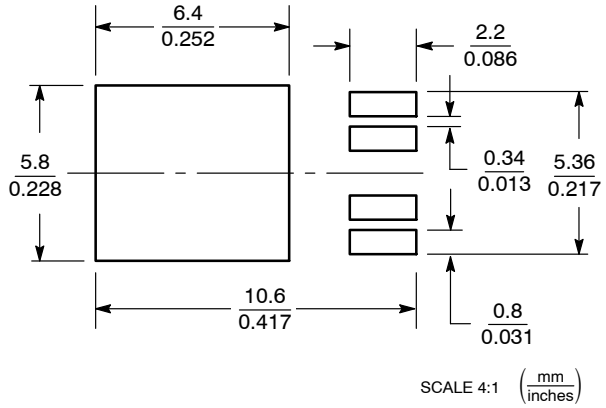
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

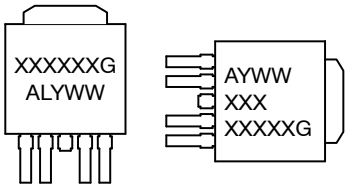
RECOMMENDED SOLDERING FOOTPRINT*



SCALE 4:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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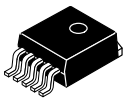
DESCRIPTION:	**DPAK−5 CENTER LEAD CROP**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

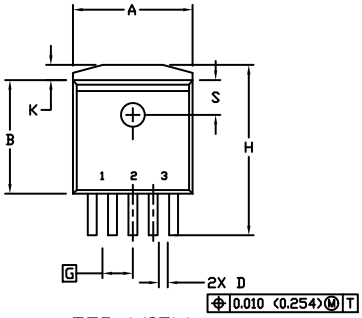
ON Semiconductor®



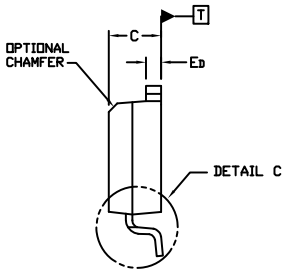
D²PAK 5−LEAD
CASE 936A−02
ISSUE E

DATE 28 JUL 2021

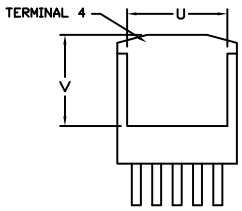
SCALE 1:1



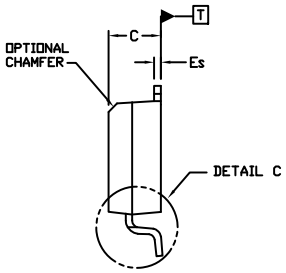
TOP VIEW



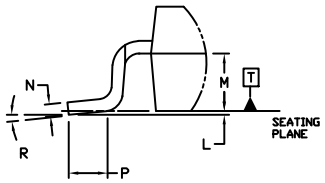
SIDE VIEW
DUAL GUAGE CONSTRUCTION



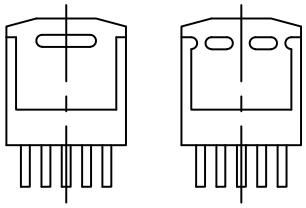
BOTTOM VIEW



SIDE VIEW
SINGLE GUAGE CONSTRUCTION



DETAIL C
TIP LEADFORM
ROTATED 90° CW

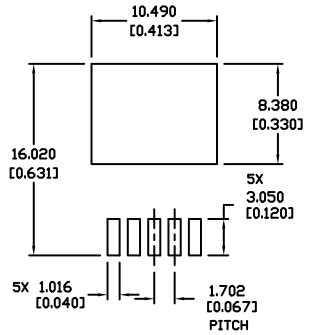


BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

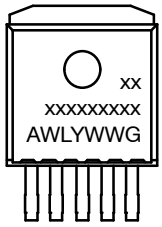
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D2PAK 5−LEAD**	**PAGE 1 OF 1**

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For additional information, please contact your local Sales Representative

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