# Negative Voltage SPDT Switch

The NLHV4157N is an advanced CMOS analog switch fabricated with silicon gate CMOS technology. The device passes analog and digital negative voltages that may vary across the full power–supply range (from  $V_{EE}$  to GND).

#### **Features**

- Operating Voltage Range:  $V_{EE} = -12 \text{ V}$  to -4 V
- Switch Signal Voltage Range:  $V_{IS} = V_{EE}$  to GND
- Positive Control Signal Voltage:  $V_{IN} = 0$  to 3.3 V
- Low ON Resistance:  $R_{ON} \le 5 \Omega$  @  $V_{EE} = -10 \text{ V}$
- Latch-up Performance Exceeds 200 mA
- Available in: SC-88 6-Pin Package
- These Devices are Pb–Free, Halogen–Free/BFR-Free and are RoHS–Compliant

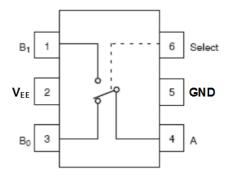


Figure 1. Pin Assignment and logic Diagram



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## MARKING DIAGRAM



SC-88 DF SUFFIX CASE 419B



HW = Device Code
M = Date Code\*
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

#### **FUNCTION TABLE**

Select Input	Function
L	B0 Connected to A
Н	B1 Connected to A

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NLHV4157NDFT2G	SC-88	3000 / Tape &
	(Pb-Free)	Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

#### **MAXIMUM RATINGS**

Symbol	Ra	ating	Value	Unit
V <sub>EE</sub>	DC Supply Voltage		-13 to +0.5	V
V <sub>IS</sub>	Analog Input Voltage (Note 1)	V <sub>EE</sub> -0.5 to +0.5	V	
V <sub>IN</sub>	Digital Select Input Voltage (Note 1)		-0.5 to +3.6	V
I <sub>IOK</sub>	Switch Input/Output diode current		±50	mA
I <sub>IK</sub>	Select input diode current	-50	mA	
P <sub>D</sub>	Power Dissipation in Still Air	60	mW	
TL	Lead Temperature, 1 mm from Case to	for 10 seconds	260	°C
TJ	Junction Bias Under Bias		150	°C
MSL	Moisture Sensitivity		Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 30% – 35%	UL94-V0 (0.125 in)	°C
ΙL	Latch-up Current (Note1)	Below GND and above V <sub>EE</sub> at 125°C	±200	mA
		Below GND and above $V_{\text{EE}}$ at 25°C	±300	1
T <sub>s</sub>	Storage Temperature		-65 to +150	°C
$\theta_{JA}$	Thermal Resistance		400	°C/W
ESD	ESD Protection	Human Body Model	3000	V
		Machine Model	150	7

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output voltage ratings may be exceeded if the input and output diode current ratings are observed.

## **RECOMMENDED OPERATING CONDITIONS** (Note 2)

Symbol	Parameter		Max	Unit
$V_{EE}$	DC Supply Voltage	-12	-4	V
V <sub>S</sub>	Switch Input / Output Voltage (B0, B1, A)	$V_{EE}$	GND	V
$V_{IN}$	Digital Select Input Voltage		3.3	V
$T_A$	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Transition Rise or Fall Time (Select Input)	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

<sup>2.</sup> Select input must be held HIGH or LOW, it must not float.

DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND; Typical characteristics are T<sub>A</sub> at 25°C.)

				<u>-</u> -	55° to 125	°C	]
Symbol	Parameter	Condition	V <sub>EE</sub> , V	Min	Тур	Max	Unit
SELECT IN	PUT						
V <sub>IH</sub>	Minimum High-Level		-12	1.8		3.3	V
	Input Voltage		-10	1.6		3.3	1
			-8	1.4		3.3	1
			-6	1.2		3.3	1
			-4	1.0		3.3	1
V <sub>IL</sub>	Maximum Low-Level		-12	0		0.8	V
	Input Voltage		-10	0		0.7	1
			-8	0		0.6	1
			-6	0		0.5	1
			-4	0		0.4	1
I <sub>IN</sub>	Maximum Input Leakage	V <sub>IN</sub> = 3.3 V or GND	-10		±0.2	±50	μΑ
	Current	V <sub>IN</sub> = 3.3 V or GND, test at 25°C only	-10			±0.5	1
POWER SU	JPPLY			L			
I <sub>CC</sub>	Maximum Quiescent Supply Current	Select = 3.3 V or GND, V <sub>IS</sub> = V <sub>EE</sub> or GND	-10 to -4		25	80	μΑ
ANALOG S	WITCH		•			•	
R <sub>ON</sub> Maximum ON	Maximum ON		-12		2.6	4.5	Ω
	Resistance (Note 3)		-10		3.0	5	1
			-8		3.5	5.8	1
			-6		4.5	7.5	1
		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IS} = V_{EE} \text{ to GND}$ $I_O \le 5 \text{ mA}$	-4		9	15	
R <sub>FLAT</sub>	ON Resistance	$V_{IN} = V_{IL}$ or $V_{IH}$	-12		0.4		Ω
	Flatness (Notes 3, 4, 6)	$V_{IS} = V_{EE}$ to GND $I_O \le 10$ mA	-10		1.2		1
			-8		1.7		1
			-6		2.5		1
		$V_{IN} = V_{IL}$ or $V_{IH}$ $V_{IS} = V_{EE}$ to GND $I_O \le 5$ mA	-4		6		
$\Delta R_{ON}$	R <sub>ON</sub> Mismatch	$I_A = -10 \text{ mA}, V_{Bn} = -8.4 \text{ V}$	-12		0.2		Ω
	Between (Notes 3, 4, 5)	$I_A = -10 \text{ mA}, V_{Bn} = -7 \text{ V}$	-10		0.2	1	1
		$I_A = -10 \text{ mA}, V_{Bn} = -5.6 \text{ V}$	-8		0.25		1
		$I_A = -10 \text{ mA}, V_{Bn} = -4.2 \text{ V}$	-6		0.25	1	1
	$I_A = -5 \text{ mA}, V_{Bn} = -2.8 \text{ V}$	-4		0.3	1	1	
I <sub>NC(OFF)</sub> , I <sub>NO(OFF)</sub>	NC or NO OFF Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or $V_{IH}$ , $V_{Bn} = GND$ , $V_A = V_{EE}$ to $GND$	-10		±1.0	±20	μΑ
I <sub>COM(ON)</sub>	COM ON Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or $V_{IH}$ ; $V_A = GND V$ or $V_{EE}$ ; $V_{B1} = GND$ or $V_{EE}$ with $V_{B0}$ floating, or $V_{B0} = GND$ or $V_{EE}$ with $V_{B1}$ floating	-10		±2.0	±20	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower

of the voltages on the two (A or B Ports).

4. Parameter is characterized but not tested in production.

ΔR<sub>ON</sub> = R<sub>ON</sub>min measured at identical V<sub>EE</sub>, temperature and voltage levels.
 Flatness is defined as the difference between the maximum and minimum value of ON Resistance over the specified range of conditions.

## AC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND; Typical characteristics are T<sub>A</sub> at 25°C.)

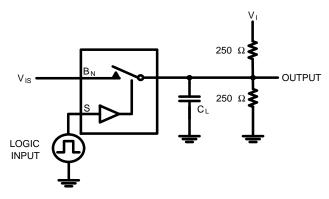
				-	-55° to 125°	С	
Symbol	Parameter	Condition	V <sub>EE</sub> , V	Min	Тур	Max	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay, Bus to Bus (Note 8) (A to B <sub>n</sub> )	C <sub>L</sub> = 100 pF (Figures 2, 3)	−12 to −4			2	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Switch Enable Time	C <sub>L</sub> = 100 pF (Figures 2, 3)	-12			220	ns
	Turn-On Time (A to B <sub>n</sub> )		-10			175	
	(/ ( to D <sub>n</sub> )		-8			165	
			-6			165	
			-4			200	
$t_{PLZ},t_{PHZ}$	Switch Disable Time	C <sub>L</sub> = 100 pF (Figures 2, 3)	-12			225	ns
	Turn-Off Time (A to B <sub>n</sub> )		-10			155	
	(/ ( to D <sub>n</sub> )		-8			150	
			-6			120	
			-4			145	
t <sub>B</sub>	Switch Break Time	$R_L = 50 \Omega$ , $C_L = 100 pF$ , $V_{IS} = -2.5 V$ (Figure 4)	-12	5		60	ns
		V <sub>IS</sub> = -2.5 V (Figure 4)	-10	5		60	
			-8	10		75	
			-6	10		90	
			-4	40		135	
t <sub>POR</sub>	Power ON Reset Time	Measured from V <sub>EE</sub> = -4 V	−12 to −4			20	μS
Q	Charge Injection	$C_L = 1 \text{ nF, } V_{GEN} = 0 \text{ V,}$	-12		170		рС
	(Note 7)	$R_{GEN} = 0 \Omega $ (Figure 5)	-10		120		
			-8		95		
			-6		55		
			-4		40		
OIRR	Off-Isolation (Note 9)	$R_L = 50 \Omega$ , $f = 10 MHz$ (Figure 6)	−12 to −4		-33		dB
Xtalk	Crosstalk	$R_L = 50 \Omega$ , $f = 10 MHz$ (Figure 7)	−12 to −4		-42		dB
BW	-3 dB Bandwidth	$R_L = 50 \Omega$ (Figure 10)	−12 to −4		200		MHz

## **CAPACITANCES** (Note 10)

Symbol	Parameter	Test Conditions	Typical @ 25°C	Unit
C <sub>IN</sub>	Input Capacitance, Select Inputs	V <sub>EE</sub> = −12 V	6	pF
C <sub>IOB</sub>	B-Port OFF Capacitance	$V_{EE} = -10 \text{ V}$	45	pF
C <sub>IOA_ON</sub>	A Port Capacitance when Switch is Enabled	V <sub>EE</sub> = −10 V	100	pF

 $<sup>10.</sup>T_A = +25$ °C, f = 1 MHz, Capacitance is characterized but not tested in production.

Guaranteed by Design.
 This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the ON Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
 Off Isolation = 20 log10 [VA/VBn].



Note: Input V<sub>IS</sub> driven by 50  $\Omega$  source terminated by 50  $\Omega$ . Note: C<sub>L</sub> includes load and stray capacitance. Input PRR = 100 kHz, t<sub>W</sub> = 5  $\mu$ s.

Parameter	V <sub>I</sub>	V <sub>IS</sub>
t <sub>PLH</sub> / t <sub>PHL</sub>	Open	Source
t <sub>PZL</sub> / t <sub>PLZ</sub>	GND	V <sub>EE</sub>
t <sub>PZH</sub> / t <sub>PHZ</sub>	2 x V <sub>EE</sub>	GND

Figure 2. AC Test Circuit

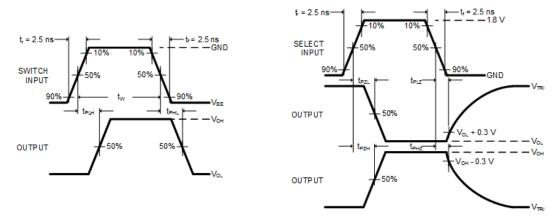


Figure 3. AC Test Waveforms

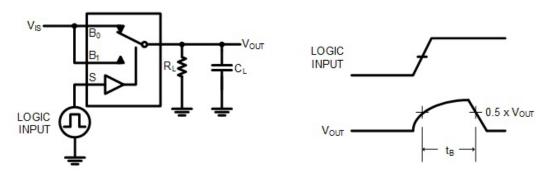


Figure 4. Switch Break Interval Timing

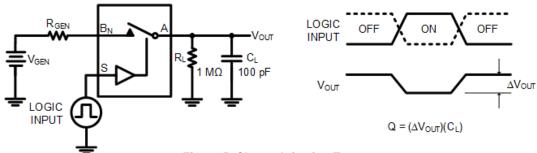


Figure 5. Charge Injection Test

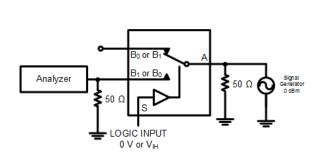


Figure 6. Off Isolation

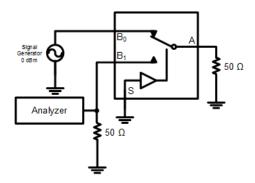


Figure 7. Crosstalk

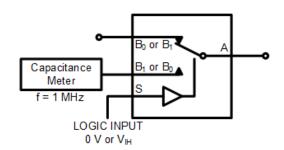


Figure 8. Channel Off Capacitance

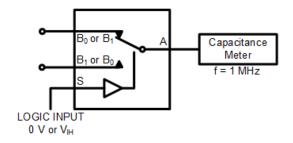


Figure 9. Channel On Capacitance

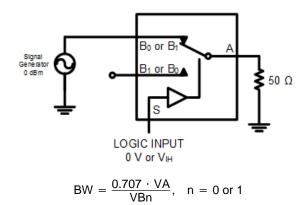


Figure 10. Bandwidth

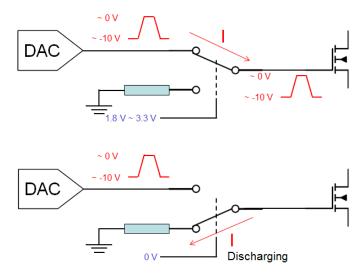
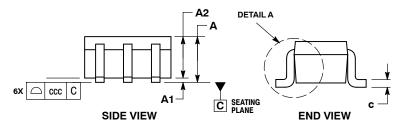


Figure 11. Typical Application

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**DATE 11 DEC 2012** 





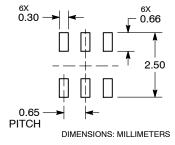
# NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
   CONTROLLING DIMENSION: MILLIMETERS
- CONTROLLING DIMENSION: MILLIMETERS.
  DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH,
- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H. DATUMS A AND B ARE DETERMINED AT DATUM H. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.

- DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION 6 AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

	MIL	LIMETE	RS		INCHES	3
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α			1.10			0.043
A1	0.00		0.10	0.000		0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
С	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
е	0.65 BSC			0	.026 BS	С
L	0.26	0.36	0.46	0.010	0.014	0.018
L2		0.15 BS	C		0.006 BS	SC
aaa	0.15				0.006	
bbb	0.30				0.012	
ccc		0.10			0.004	
ddd		0.10			0.004	

#### **RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## **GENERIC MARKING DIAGRAM\***



XXX = Specific Device Code

= Date Code\* = Pb-Free Package

(Note: Microdot may be in either location)

- \*Date Code orientation and/or position may vary depending upon manufacturing location.
- \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

## **STYLES ON PAGE 2**

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## SC-88/SC70-6/SOT-363 CASE 419B-02 ISSUE Y

**DATE 11 DEC 2012** 

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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