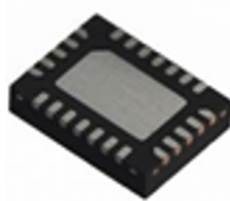


## Programmable buck converter for USB power delivery



QFN24L 3 x 4 mm

### Features

- Input voltage range 6.0 V to 26.4 V
- Internal power MOS synch rectification
- Internal compensation
- I<sup>2</sup>C bus controlled
- V<sub>out</sub> settings: 3 V to 20 V with 20 mV (min.) steps
- Slew rate control (max. 30 mV/us)
- Cable drop compensation
- I<sub>out</sub> settings: 0.1 A to 3 A with 50 mA steps
- Embedded discharge function
- Two programmable switching frequencies with optional clock dithering
- Watchdog timer set by I<sup>2</sup>C
- Configurable interrupt pin
- Soft-start
- Power-on pin
- Programmable constant current limit
- OVP, IPEAK and overtemperature protections
- Short-circuit protection
- Undervoltage lockout
- Available in QFN24L 3 x 4 package

#### Product status link

STPD01

#### Product summary

|                   |              |
|-------------------|--------------|
| <b>Order code</b> | STPD01PUR    |
| <b>Package</b>    | QFN24L 3 x 4 |

### Applications

- AC adapters
- USB hubs
- PC monitors
- Smart TV
- USB-PD power distribution

### Description

The STPD01 is a programmable synchronous buck converter suitable to provide power supply in applications following USB power delivery specifications.

The device provides those voltages required by USB power delivery systems as stated in USB PD 3.0 spec up to 60 W output power (20 V, 3 A).

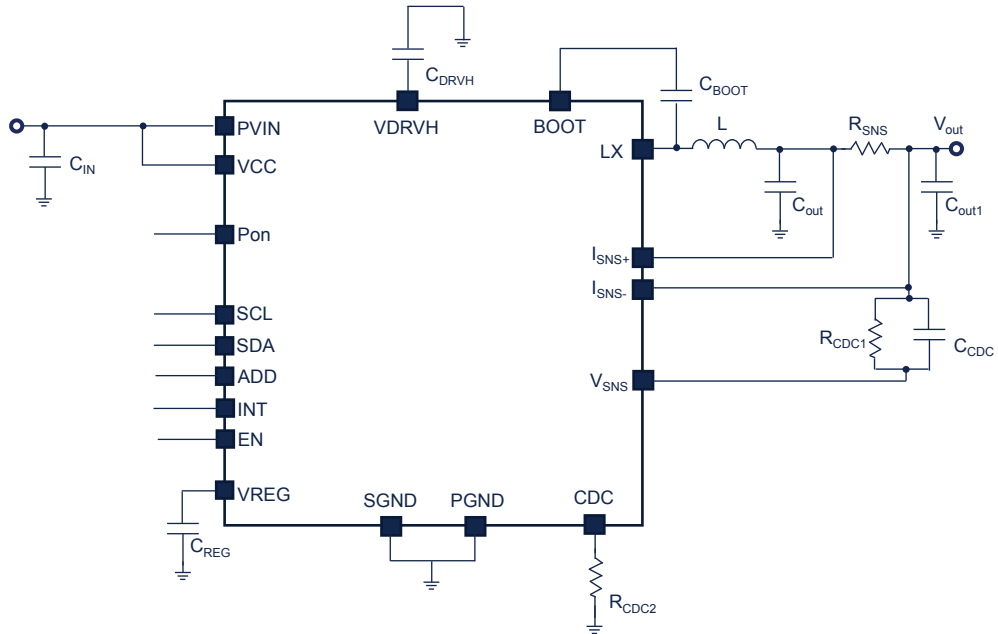
The different levels of output voltage and current limitation can be set dynamically through I<sup>2</sup>C interface.

Overvoltage, overcurrent and overtemperature protections are included in the device.

A programmable watchdog improves the robustness and the safety of the complete system.

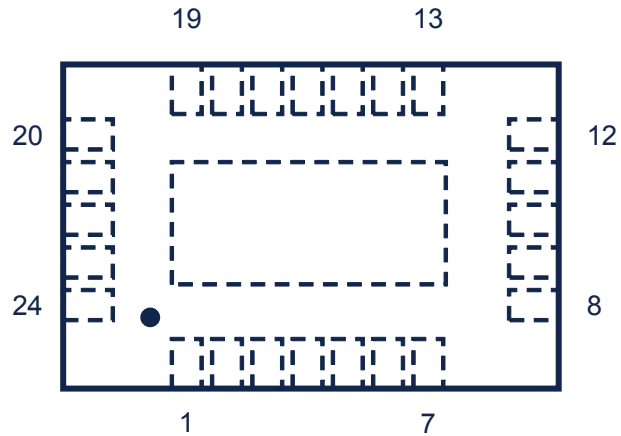
Finally, the device is available in QFN24L 3 x 4 mm<sup>2</sup>.

# 1 Application schematic

**Figure 1. STPD01 typical application schematic**

**Table 1. Bill of material**

| Symbol                  | Value                   | Description       | Note                                    |
|-------------------------|-------------------------|-------------------|---|
| $R_{SNS}$               | 25 m $\Omega$ 1%        |                   |   |
| L                       | 10 $\mu$ H              | Low DCR           |   |
| $C_{IN}$                | 47 $\mu$ F              | Ceramic capacitor |   |
| $C_{BOOT}$              | 100 nF                  | Ceramic capacitor |   |
| $C_{OUT}$               | 68-100 $\mu$ F          | Ceramic capacitor | Spec USB PD                             |
| $C_{OUT1}$              | 10-22 $\mu$ F           | Ceramic capacitor |   |
| R <sub>CDC1</sub>       | 10 k $\Omega$           |                   |   |
| R <sub>CDC2</sub>       | Function of $R_{CABLE}$ |                   | See Section 7.2 Cable drop compensation |
| CDRVH, C <sub>REG</sub> | 1 $\mu$ F               | Ceramic capacitor |   |

## 2 Pin configuration (top through view)

**Figure 2. Pin configuration (top through view)**

**Table 2. Pin description**

| Position | Name    | Description   |
|----------|---------|---|
| 1        | SDA     | I <sup>2</sup> C data   |
| 2        | SCL     | I <sup>2</sup> C clock  |
| 3        | ADD     | I <sup>2</sup> C address selection (cannot be left floating)  |
| 4        | INT     | Interrupt pin (open drain output)   |
| 5        | EN      | Enable pin. Internally pulled up to VREG  |
| 6        | VDRIVEH | High-side driver supply. Connect to a bypass capacitor  |
| 7        | VCC     | Analog supply input   |
| 8        | PVIN    | Power supply input  |
| 9        | PVIN    | Power supply input  |
| 10       | PGND    | Power ground  |
| 11       | PGND    | Power ground  |
| 12       | PGND    | Power ground  |
| 13       | LX      | Switching node  |
| 14       | LX      | Switching node  |
| 15       | LX      | Switching node  |
| 16       | BOOT    | Connect the bootstrap capacitor (0.1 $\mu$ F) between this pin and LX   |
| 17       | Pon     | Power-on (open drain output). Pulled high when Vout reaches the regulation value after startup                            |
| 18       | VREG    | Internal LDO regulator voltage pin (connect 1 $\mu$ F capacitor between this pin and GND)                                 |
| 19       | ISNS+   | Positive connection for the current sensing resistor. Connect to GND if not used  |
| 20       | ISNS-   | Negative connection for the current sensing resistor. Connect to GND if not used  |
| 21       | VSNS    | Output voltage sensing pin. Used also for cable drop compensation see <a href="#">Section 7.2 Cable drop compensation</a> |
| 22       | CDC     | Cable drop compensation programming pin   |

| Position | Name | Description  |
|----------|------|--|
| 23       | NC   | Not connected. Leave floating  |
| 24       | SGND | Signal ground  |
|          | EP   | Exposed pad for heat dissipation, to be electrically connected to Power ground |

### 3 Maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol   | Parameter                                 | Test conditions   | Value              | Unit |
|--|---|---|--------------------|------|
| PVIN   | Input supply                              | DC voltage  | -0.3 to +28        | V    |
| VCC  | Analog input supply                       | DC voltage  | -0.3 to PVIN + 0.3 | V    |
| I <sub>SNS+</sub> , I <sub>SNS-</sub> , V <sub>SNS</sub> | Sensing inputs                            | DC voltage  | -0.3 to PVIN + 0.3 | V    |
| I <sub>SNS+</sub> , I <sub>SNS-</sub>                    | Differential voltage between sensing pins | DC voltage  | 0 to 3             | V    |
|  | Current sourced by the pin                | V <sub>ISNS+</sub> = V <sub>ISNS-</sub> < 0,<br>(DC and AC) | 10                 | mA   |
| LX   | Switching node                            | DC voltage  | -0.3 to PVIN + 0.3 | V    |
| BOOT   | BOOT voltage vs. GND                      | DC voltage  | -0.3 to 34         | V    |
|  | BOOT voltage vs. LX                       | DC voltage  | -0.3 to 6          | V    |
| VDRIVEH  | Internal power supply                     | DC voltage  | -0.3 to 6          | V    |
| VREG   | Internal LDO regulator voltage pin        | DC voltage  | -0.3 to 6          | V    |
| INT, SDA, SCL, ADD, EN, Pon                              | Logic pins voltage                        | DC voltage  | -0.3 to 6          | V    |
| CDC  | Analog pins voltage                       | DC voltage  | -0.3 to 2.5        | V    |
| PGND, SGND   | GND voltage                               | DC voltage  | -0.3 to +0.3       | V    |
| ESD  | Human body model                          | JS-001-2012   | ±2000              | V    |

**Table 4. Thermal data**

| Symbol                           | Parameter                                    | QFN 3x4 24L | Unit |
|----------------------------------|--|-------------|------|
| R <sub>THJA</sub> <sup>(1)</sup> | Junction to ambient board thermal resistance | 31          | °C/W |
| T <sub>J</sub>                   | Operating junction temperature               | -40 to +125 | °C   |
| T <sub>STG</sub>                 | Storage temperature                          | -65 to +150 | °C   |
| T <sub>LEAD</sub>                | Lead temperature (soldering 10 s.)           | 260         | °C   |

1. Standard FR4 4 layer PCB board.

## 4 Electrical characteristics

**Table 5. Recommended operating conditions**

| Symbol             | Parameter             | Min.         | Typ. | Max. | Unit |
|--------------------|-----------------------|--------------|------|------|------|
| PVIN               | Input voltage         | 6            | 24   | 26.4 | V    |
| VCC                | Analog supply voltage | Same as PVIN |      |      |      |
| VSNS               | Output voltage        | 3            |      | 22   | V    |
| ISNS+, ISNS-       | Current sensing pins  | 0            |      | 22   | V    |
| Iout               | Output current        |              |      | 3    | A    |
| EN, Pon            | Analog pins           |              |      | 5    | V    |
| SDA, SCL, ADD, INT | Digital pins          |              |      | 5    | V    |

( $T_A = 25\text{ °C}$ ,  $V_{CC}=V_{IN} = 24\text{ V}$  unless otherwise specified)

**Table 6. Electrical characteristics**

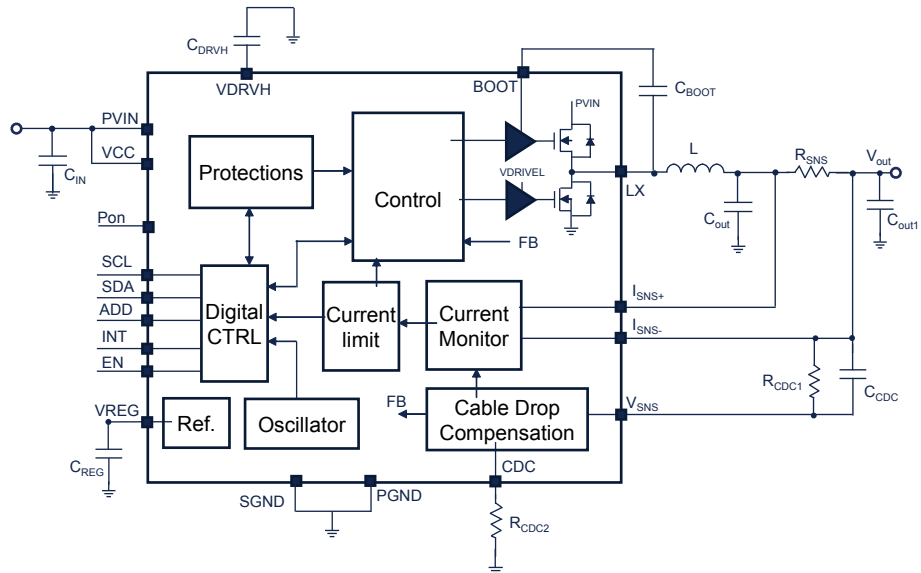
| Symbol               | Parameter   | Test conditions  | Min. | Typ. | Max. | Unit  |
|----------------------|---|--|------|------|------|-------|
| <b>Power section</b> |   |  |      |      |      |       |
| I <sub>IN</sub>      | Active supply current <sup>(1)</sup>                                  | F <sub>sw</sub> =500 kHz, EN=HIGH, no inductor, I <sub>SNS+</sub> =0, I <sub>SNS-</sub> =0, V <sub>SNS</sub> =4.8 V, reg 0x01 = 0x1D |      | 12   | 18   | mA    |
|                      |   | F <sub>sw</sub> =750 kHz, EN=HIGH, no inductor, I <sub>SNS+</sub> =0, I <sub>SNS-</sub> =0, V <sub>SNS</sub> =4.8 V, reg 0x01 = 0x1D |      | 16   | 22   | mA    |
|                      | No switching supply current <sup>(1)</sup>                            | EN=HIGH, no inductor, I <sub>SNS+</sub> =0, I <sub>SNS-</sub> =0, LX=HiZ, V <sub>SNS</sub> =GND                                      |      | 0.9  | 2    | mA    |
|                      | Shutdown supply current <sup>(1)</sup>                                | EN=GND   |      | 16   | 25   | µA    |
| UVLO <sub>H</sub>    | Operating start voltage   | Detect PV <sub>IN</sub> rising   |      |      | 5.5  | V     |
| UVLO <sub>L</sub>    | Operating stop voltage  | Detect PV <sub>IN</sub> falling  | 5.0  |      |      | V     |
| VREG                 | Internal power supply voltage   | I <sub>reg</sub> = 0 mA  | 3.5  | 3.8  | 4.0  | V     |
| VSNS                 | Output voltage accuracy <sup>(2)</sup>                                |  | -2   |      | +2   | %     |
| Vout <sub>SR</sub>   | Vout transition slew rate   | Absolute value   |      |      | 30   | mV/µs |
| ΔV <sub>out</sub>    | Dynamic overshoot/undershoot during voltage transition <sup>(2)</sup> | See Section 7.5 Vout transition  | -0.5 |      | 0.5  | V     |
| R <sub>ONHS</sub>    | High-side FET on-resistance   | I <sub>LX</sub> = 100 mA   |      | 50   |      | mΩ    |
| R <sub>ONLS</sub>    | Low-side FET on-resistance  | I <sub>LX</sub> = 100 mA   |      | 50   |      | mΩ    |
| SS <sub>SLOPE</sub>  | Soft-start slope  |  |      | 2.5  |      | V/ms  |
| F <sub>SW</sub>      | Switching frequency   | T <sub>J</sub> = 25 °C, reg 0x05 : bit2=0  |      | 500  |      | kHz   |
|                      |   | T <sub>J</sub> = 25 °C, reg 0x05 : bit2=1  |      | 750  |      |       |
| DC                   | Duty cycle  |  | 10   |      | 99   | %     |
| I <sub>DSC</sub>     | Output discharge current  |  |      | 60   |      | mA    |
| Pon                  | Pon threshold (% of VOUT)   | Lower  |      | 95   |      | %     |
|                      |   | Upper  |      | 105  |      | %     |
|                      | Pon deglitch  |  |      | 5    |      | ms    |

| Symbol                               | Parameter  | Test conditions   | Min. | Typ. | Max. | Unit |
|--------------------------------------|--|---|------|------|------|------|
| $I_{pk}$                             | Inductor current limit thresholds                                | Positive  |      | 5    |      | A    |
| $I_{valley}$                         |  | Negative  |      | 3.5  |      |      |
| OVP                                  | Overvoltage protection threshold (VSNS/Vnom)                     | VSNS sensed voltage vs. nominal vout set in the reg 0x00  | 1.1  | 1.15 |      | V/V  |
|                                      | OVP deglitch   |   |      | 5    |      | ms   |
|                                      | OVP masking time during Vout transition or fault                 | Start-to-end transition   | 275  | 300  |      | ms   |
| CC <sub>th</sub>                     | Constant current threshold (I <sub>out</sub> /I <sub>lim</sub> ) | R <sub>sense</sub> = 25 mΩ, 1% precision, 0.5<I <sub>out</sub> <3 A                                       |      | 1.00 |      | A/A  |
| SCP                                  | Short-circuit protection   | Percentage of VSNS  |      | 20   |      | %    |
|                                      | Short-circuit timer  |   |      | 300  |      | ms   |
| OTP                                  | Overtemperature protection threshold <sup>(2)</sup>              |   |      | 165  |      | °C   |
|                                      | OTP hysteresys   |   |      | 30   |      | °C   |
| TW                                   | Thermal warning  | Reg 0x02  |      | 150  |      | °C   |
|                                      | TW hysteresys  |   |      | 10   |      | °C   |
| $\eta$                               | Efficiency <sup>(2)</sup>  | V <sub>out</sub> = 5 V, I <sub>out</sub> = 1.5 A, F <sub>sw</sub> =500 kHz                                |      | 89   |      | %    |
|                                      |  | V <sub>out</sub> = 9 V, I <sub>out</sub> = 1.5 A, F <sub>sw</sub> =500 kHz                                |      | 93   |      |      |
|                                      |  | V <sub>out</sub> = 15 V, I <sub>out</sub> = 1.5 A, F <sub>sw</sub> =500 kHz                               |      | 95   |      |      |
|                                      |  | V <sub>out</sub> = 20 V, I <sub>out</sub> = 1.5 A, F <sub>sw</sub> =500 kHz                               |      | 96   |      |      |
| SCL <sub>f</sub>                     | SCL clock frequency  |   |      |      | 400  | kHz  |
|                                      | Cable drop compensation  | R <sub>CDC1</sub> = 10 kΩ, R <sub>CDC2</sub> = 24 kΩ, R <sub>SENSE</sub> = 25 mΩ, I <sub>LOAD</sub> = 1 A |      | 450  |      | mV   |
|                                      | Cable drop tolerance   |   | -30  |      | +30  | %    |
|                                      | Cable drop saturation  |   |      | 1    |      | V    |
|                                      | ISNS+, ISNS- Bias current  | V <sub>ISNS+</sub> = V <sub>ISNS-</sub> = 20 V  |      | 100  |      | μA   |
| EN                                   | ON threshold   |   | 1.2  |      |      | V    |
|                                      | OFF threshold  |   |      |      | 0.35 |      |
| I <sub>EN</sub>                      | Enable current   | EN = GND  |      | 3    | 5    | μA   |
| <b>Logic section (SCL, SDA pins)</b> |  |   |      |      |      |      |
| VOL                                  | Low level output voltage   | I <sub>SINK</sub> = 2 mA  |      |      | 0.2  | V    |
| VIH                                  | High level threshold voltage                                     |   | 1.2  |      |      | V    |
| VIL                                  | Low level threshold voltage                                      |   |      |      | 0.35 | V    |
| I <sub>lk</sub>                      | Leakage current  | V <sub>pullup</sub> = 3.3 V   |      | 1    |      | uA   |
| <b>INT, PON pins</b>                 |  |   |      |      |      |      |
| Vod                                  | Output voltage   | I <sub>SINK</sub> = 2 mA  |      |      | 0.1  | V    |
| Iod                                  | Leakage current  | V <sub>pullup</sub> = 5 V   |      |      | 1    | uA   |

1. Cumulative current from PVIN and V<sub>CC</sub>.
2. Not tested in production.

## 5 Block diagram

Figure 3. STPD01 block diagram





## 6 Typical performance characteristics

Figure 4. Efficiency ( $V_{in} = V_{cc} = 24\text{ V}$ ,  $CC = 0x1F$ ,  $F_{sw} = 500\text{kHz}$ )

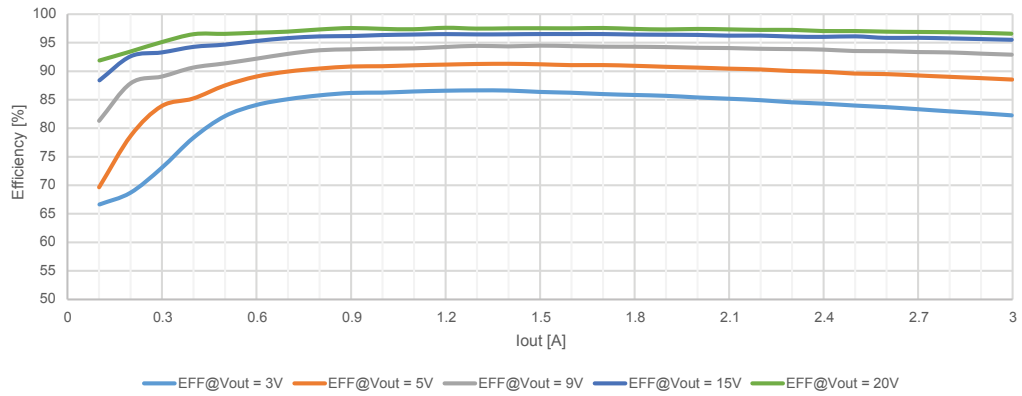


Figure 5. System  $P_{LOSS}$  ( $V_{in} = V_{cc} = 24\text{ V}$ ,  $CC = 0x1F$ ,  $F_{sw} = 500\text{ kHz}$ )

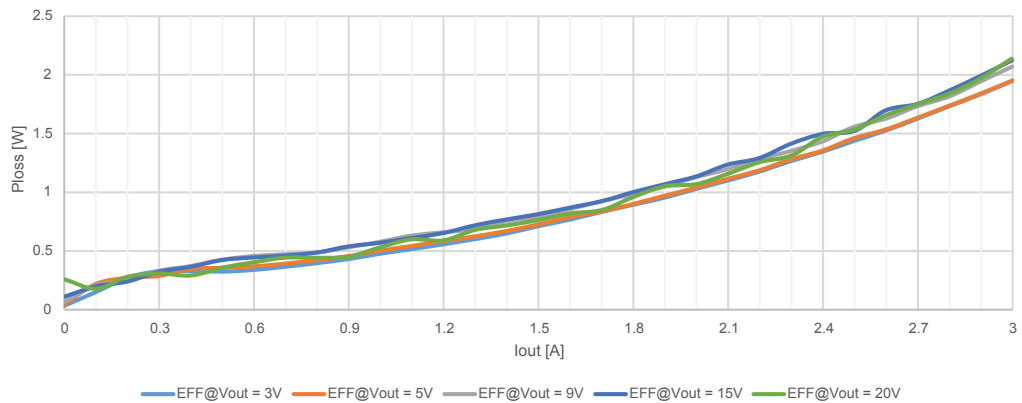
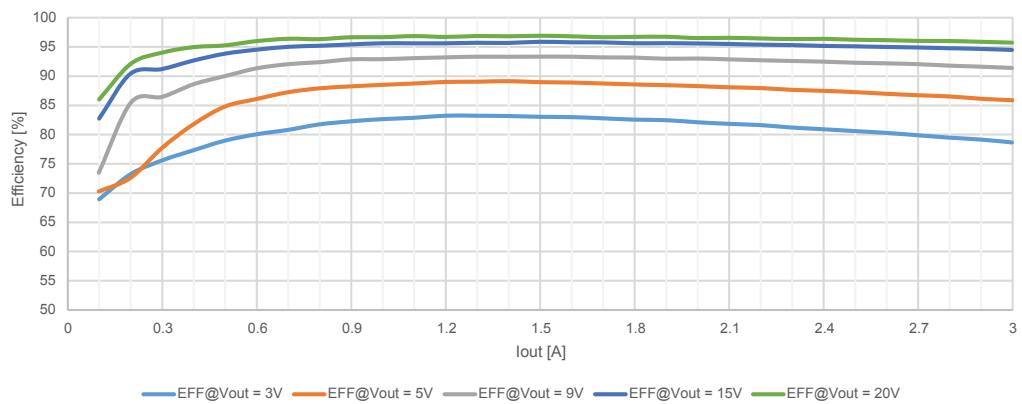
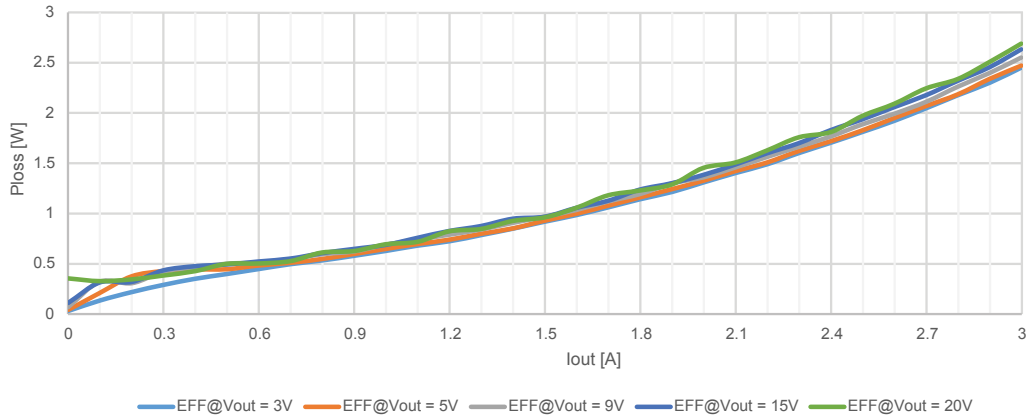
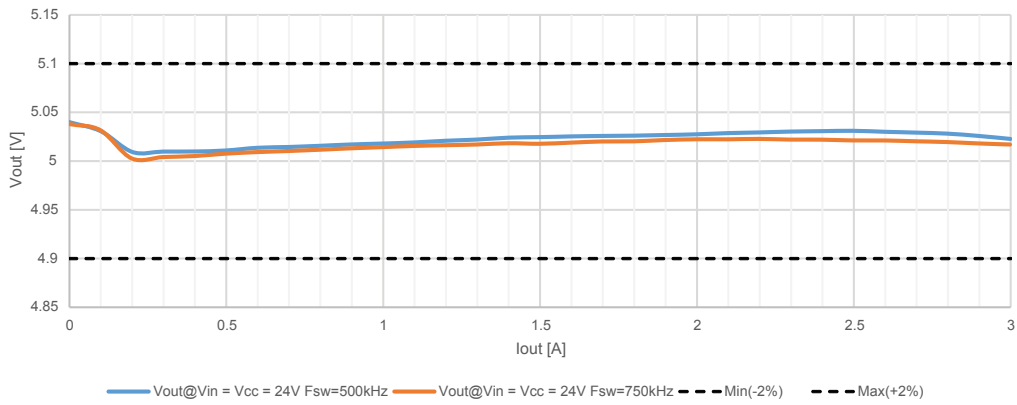
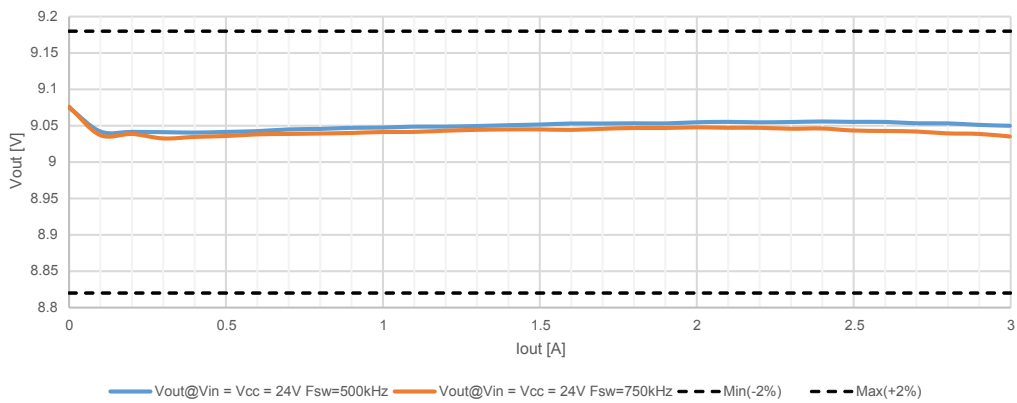
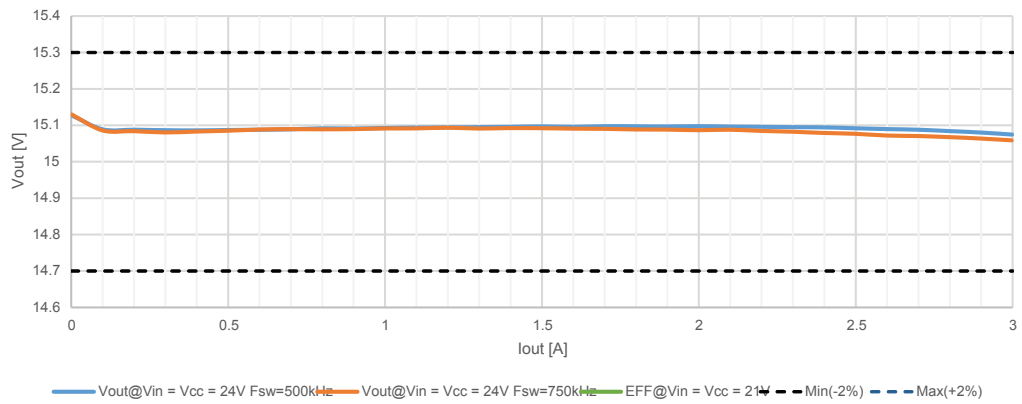
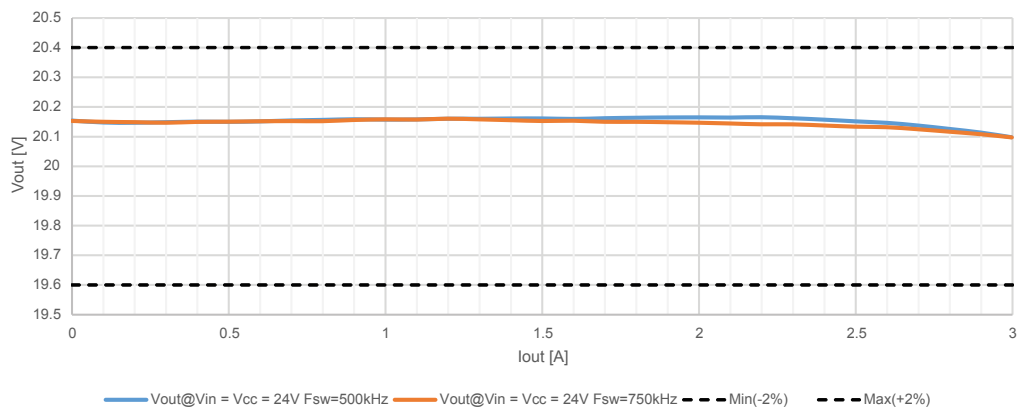
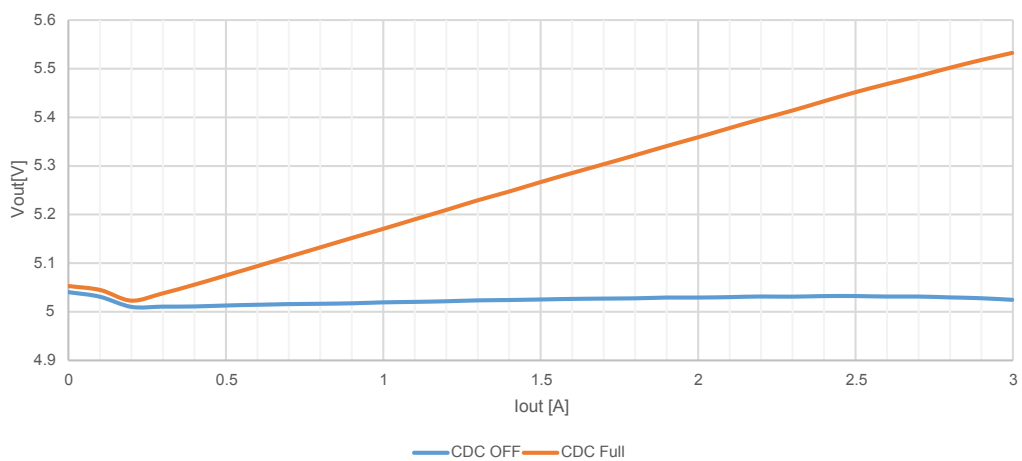
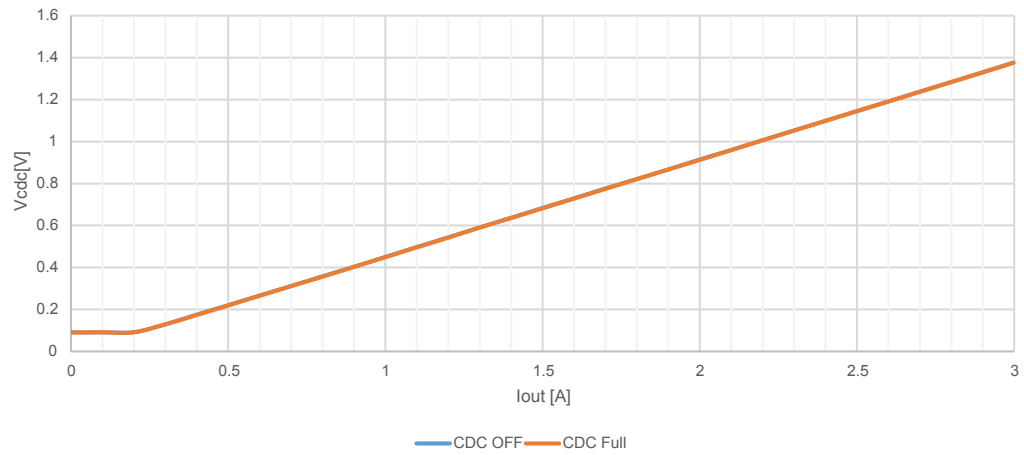
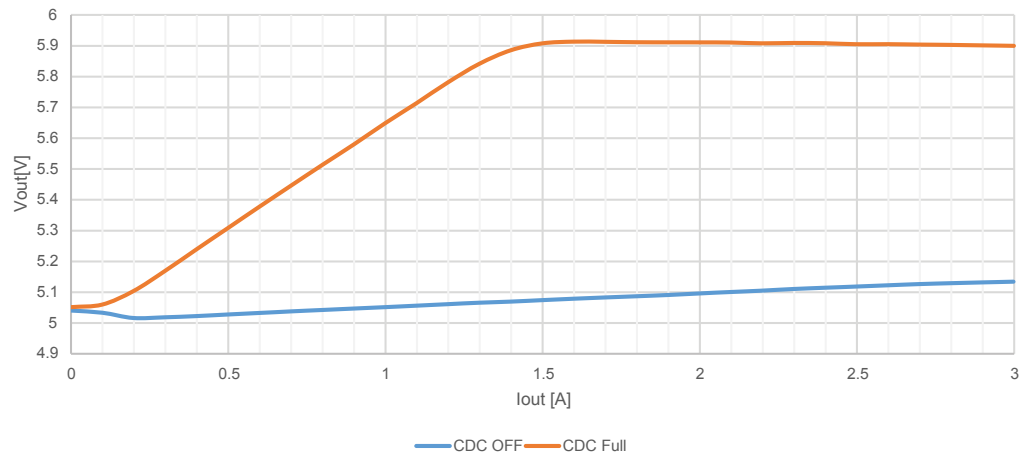
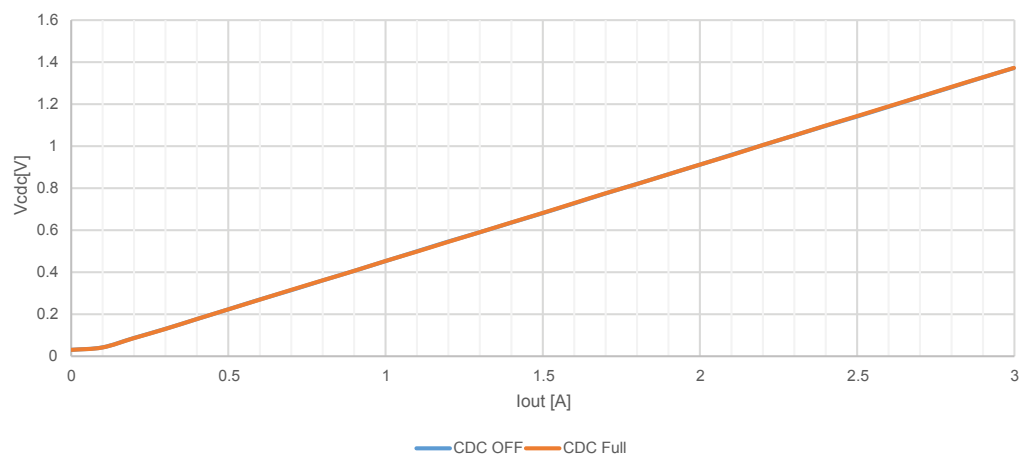


Figure 6. Efficiency ( $V_{in} = V_{cc} = 24\text{ V}$ ,  $CC = 0x1F$ ,  $F_{sw} = 750\text{ kHz}$ )

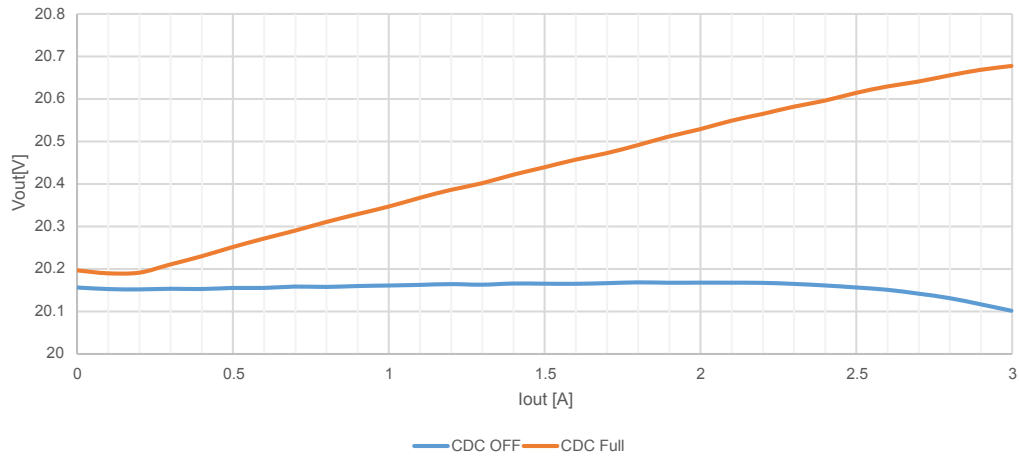


**Figure 7. System  $P_{LOSS}$  ( $V_{in} = V_{CC} = 24\text{ V}$ ,  $CC = 0x1F$ ,  $F_{sw} = 750\text{ kHz}$ )**

**Figure 8.  $V_{OUT}$  vs. load ( $V_{in} = V_{CC} = 24\text{ V}$ ,  $V_{out} = 0x64$  (5 V),  $CC = 0x1F$ )**

**Figure 9.  $V_{OUT}$  vs. load ( $V_{in} = V_{CC} = 24\text{ V}$ ,  $V_{out} = 0xB0$  (9 V),  $CC = 0x1F$ )**


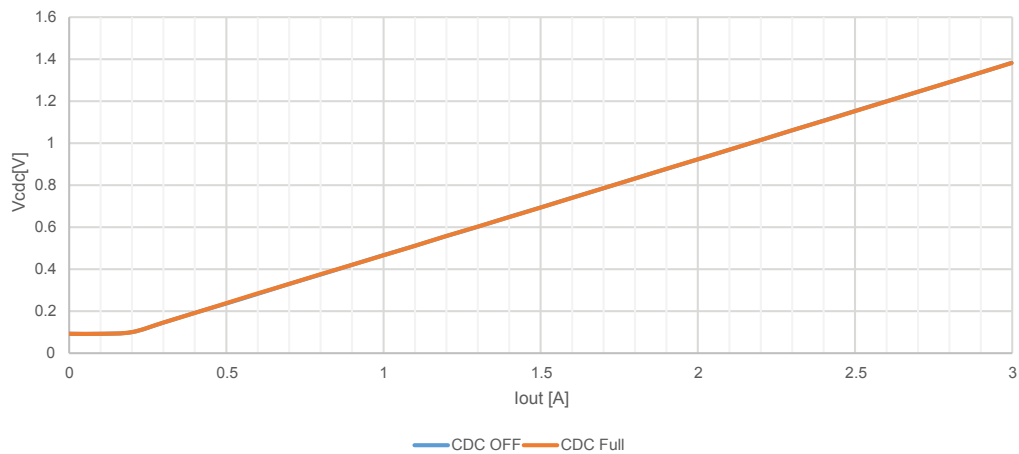
**Figure 10. VOUT vs. load (Vin = VCC = 24 V, Vout = 0xD8 (15 V), CC = 0x1F)**

**Figure 11. VOUT vs. load (Vin = VCC = 24 V, Vout = 0xF1 (20 V), CC = 0x1F)**

**Figure 12. VOUT vs. load, with cable drop compensation on (Vin = VCC = 24 V, Vout = 0x64 (5 V), CC = 0x1F, Rcdc2 = 24 kΩ, Fsw = 500 kHz)**


**Figure 13. VCDC vs. load ( $V_{in} = V_{CC} = 24\text{ V}$ ,  $V_{out} = 0x64\text{ (5 V)}$ ,  $CC = 0x1F$ ,  $R_{cdc2} = 24\text{ k}\Omega$ ,  $F_{sw} = 500\text{ kHz}$ )**

**Figure 14. VOUT vs. load, with cable drop compensation on ( $V_{in} = V_{CC} = 24\text{ V}$ ,  $V_{out} = 0x64\text{ (5 V)}$ ,  $CC = 0x1F$ ,  $R_{cdc2} = 6.8\text{ k}\Omega$ ,  $F_{sw} = 500\text{ kHz}$ )**

**Figure 15. VCDC vs. load ( $V_{in} = V_{CC} = 24\text{ V}$ ,  $V_{out} = 0x64\text{ (5 V)}$ ,  $CC = 0x1F$ ,  $R_{cdc2} = 6.8\text{ k}\Omega$ ,  $F_{sw} = 500\text{ kHz}$ )**


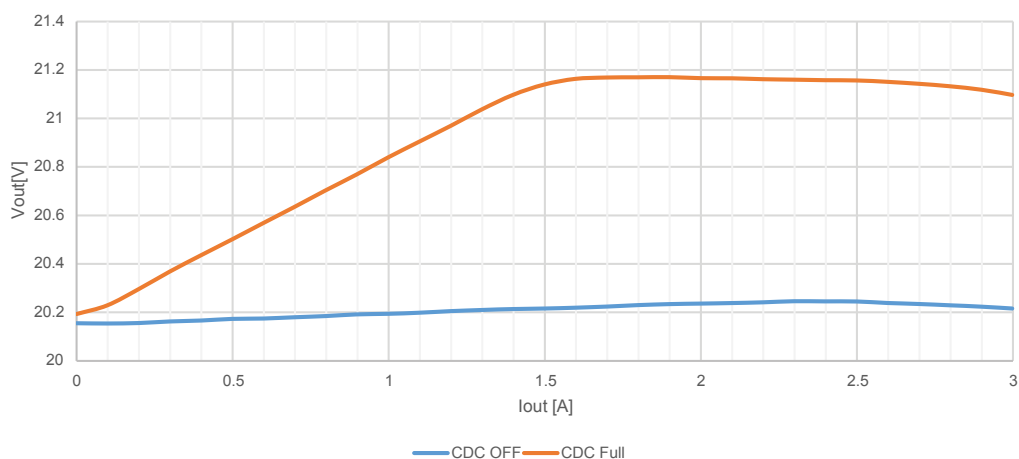
**Figure 16. VOUT vs. load, with cable drop compensation on (Vin = VCC = 24 V, Vout = 0xF1 (20 V), CC = 0x1F, R<sub>cdc2</sub> = 24 kΩ, F<sub>sw</sub> = 500 kHz)**

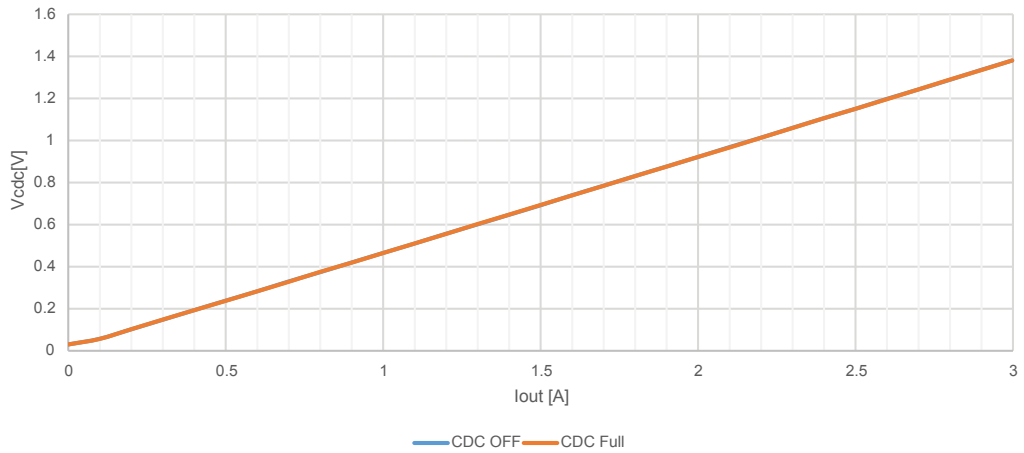
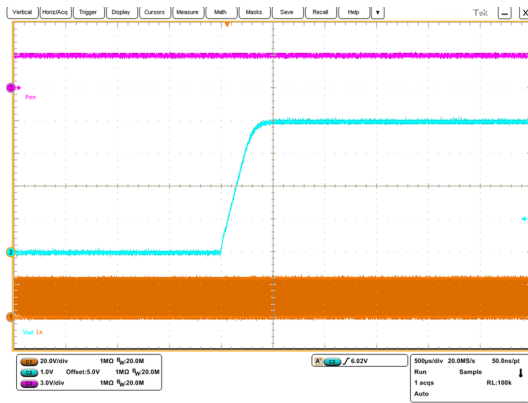
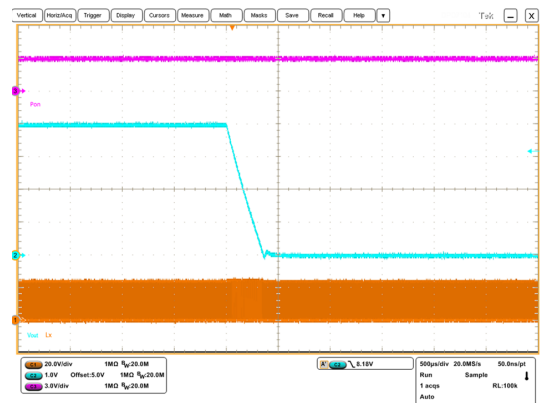
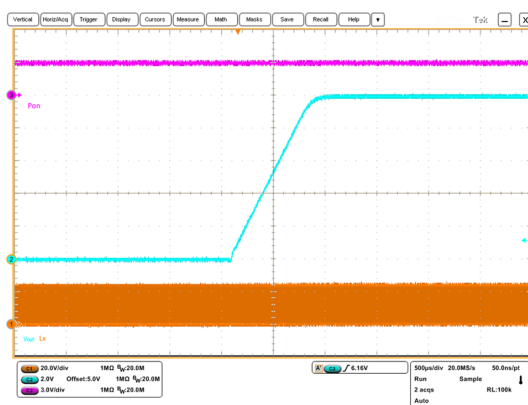
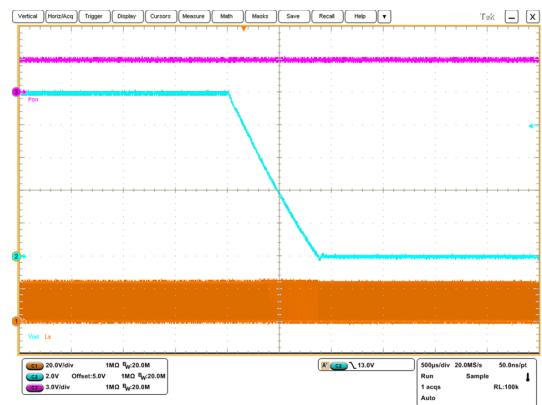


**Figure 17. VCDC vs. load (Vin = VCC = 24 V, Vout = 0xF1 (20 V), CC = 0x1F, R<sub>cdc2</sub> = 24 kΩ, F<sub>sw</sub> = 500 kHz)**

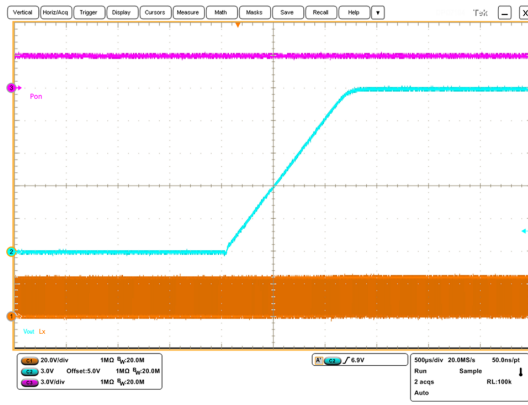


**Figure 18. VOUT vs. load, with cable drop compensation on (Vin = VCC = 24 V, Vout = 0xF1 (20 V), CC = 0x1F, R<sub>cdc2</sub> = 6.8 kΩ, F<sub>sw</sub> = 500 kHz)**

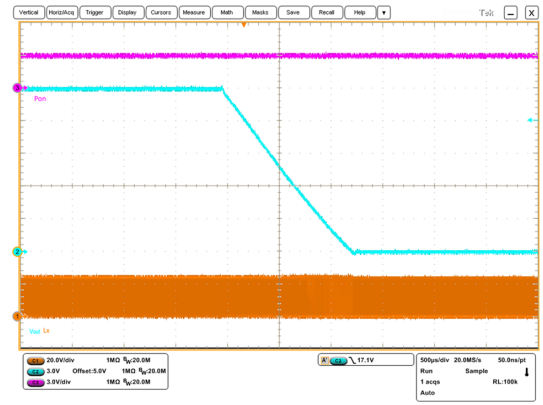


**Figure 19. V<sub>cdc</sub> vs. load (V<sub>in</sub> = V<sub>CC</sub> = 24 V, V<sub>out</sub> = 0xF1 (20 V), CC = 0x1F, R<sub>cdc2</sub> = 6.8 kΩ, F<sub>sw</sub> = 500 kHz)**

**Figure 20. V<sub>OUT</sub> transition (V<sub>in</sub> = V<sub>CC</sub> = 24 V, V<sub>out</sub> = 0x64 (5 V) to 0xB0 (9 V), CC = 0x1F, load = 500 mA, F<sub>sw</sub> = 500 kHz)**

**Figure 21. V<sub>OUT</sub> transition (V<sub>in</sub> = V<sub>CC</sub> = 24 V, V<sub>out</sub> = 0xB0 (9 V) to 0x64 (5 V), CC = 0x1F, load = 500 mA, F<sub>sw</sub> = 500 kHz)**

**Figure 22. V<sub>OUT</sub> transition (V<sub>in</sub> = V<sub>CC</sub> = 24 V, V<sub>out</sub> = 0x64 (5 V) to 0xD8 (15 V), CC = 0x1F, load = 500 mA, F<sub>sw</sub> = 500 kHz)**

**Figure 23. V<sub>OUT</sub> transition (V<sub>in</sub> = V<sub>CC</sub> = 24 V, V<sub>out</sub> = 0xD8 (15 V) to 0x64 (5 V), CC = 0x1F, load = 500 mA, F<sub>sw</sub> = 500 kHz)**


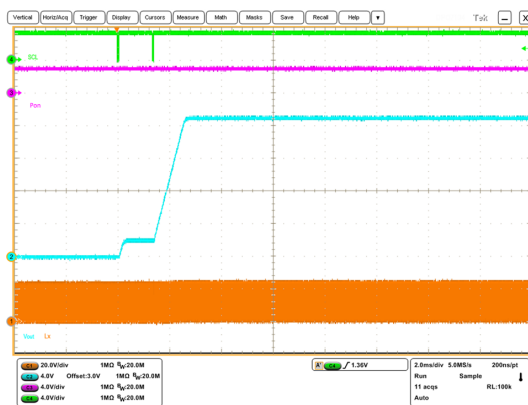
**Figure 24.** VOUT transition (Vin = VCC = 24 V, Vout = 0x64 (5 V) to 0xF1 (20 V), CC = 0x1F, load = 500 mA, F<sub>sw</sub> = 500 kHz)



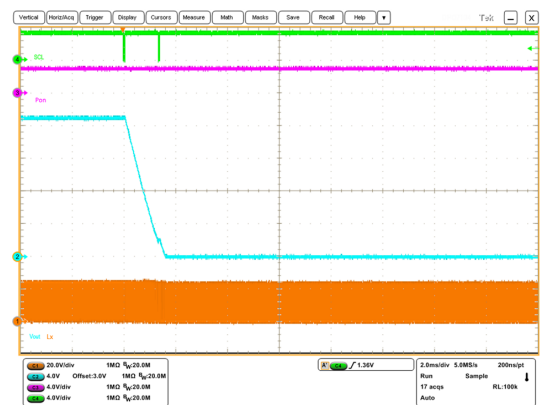
**Figure 25.** VOUT transition (Vin = VCC = 24 V, Vout = 0xF1 (20 V) to 0x64 (5 V), CC = 0x1F, load = 500 mA, F<sub>sw</sub> = 500 kHz)



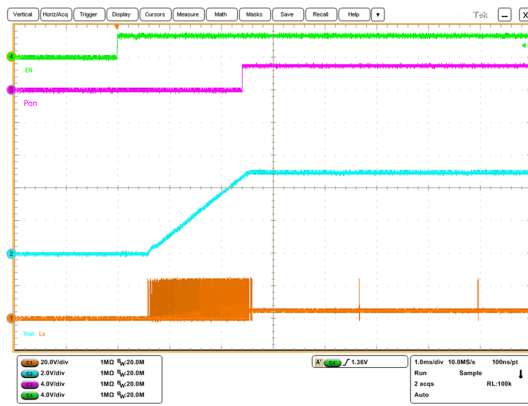
**Figure 26.** VOUT transition (Vin = VCC = 24 V, Vout = 0x00 (3 V) to 0x64 (5 V) to 0xF1 (20 V), CC = 0x1F, load = 500 mA, F<sub>sw</sub> = 500 kHz)



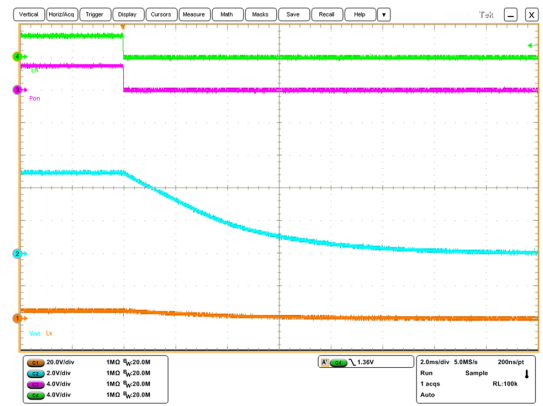
**Figure 27.** VOUT transition (Vin = VCC = 24 V, Vout = 0xF1 (20 V) to 0x64 (5 V) to 0x00 (3 V), CC = 0x1F, load = 500 mA, F<sub>sw</sub> = 500 kHz)



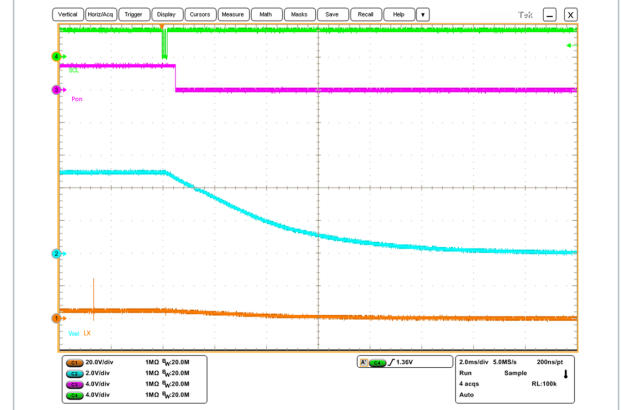
**Figure 28.** Enable startup (Vin = VCC = 24 V, Vout = 0x64 (5 V), no load)



**Figure 29.** Enable shutdown (Vin = VCC = 24 V, Vout = 0x64 (5 V), no load)



**Figure 30. Digit enable startup ( $V_{in} = V_{CC} = 24\text{ V}$ ,  $V_{out} = 0x64\text{ (5 V)}$ , no load)**

**Figure 31. Digit enable shutdown ( $V_{in} = V_{CC} = 24\text{ V}$ ,  $V_{out} = 0x64\text{ (5 V)}$ , no load)**




## 7 Operation description

### 7.1 Enable

The device can be forced into shutdown mode by pulling the enable pin low. In this condition, the I<sup>2</sup>C interface is switched off.

Once the EN pin voltage exceeds the threshold value, then the device immediately switches on following the start-up sequence.

#### 7.1.1 Digital enable

The device can be enabled/disabled using the external pin EN, which switches off the DC-DC, the oscillator and the digital core completely.

Optionally, the DC-DC can be switched off by the DIG\_EN bit in I<sup>2</sup>C register (0x06), but in this case the digital core is kept partially ON to allow the I<sup>2</sup>C to wake up the device.

Table 7. Functional modes

| Dig_EN bit | EN pin | I <sup>2</sup> C interface | DC-DC state | Pon        |
|------------|--------|----------------------------|-------------|------------|
| -          | Low    | OFF                        | Stop        | Functional |
| Low        | High   | Functional                 | Stop        | Functional |
| High       | High   | Functional                 | Operating   | Functional |

### 7.2 Cable drop compensation

In some applications, the output voltage needs to be increased proportionally to load current to compensate the potential voltage drop across copper tracks (and output cable). The compensation acts by altering the current flowing in the high-side of the voltage feedback resistor divider. The resulting compensation voltage is expressed as follows:

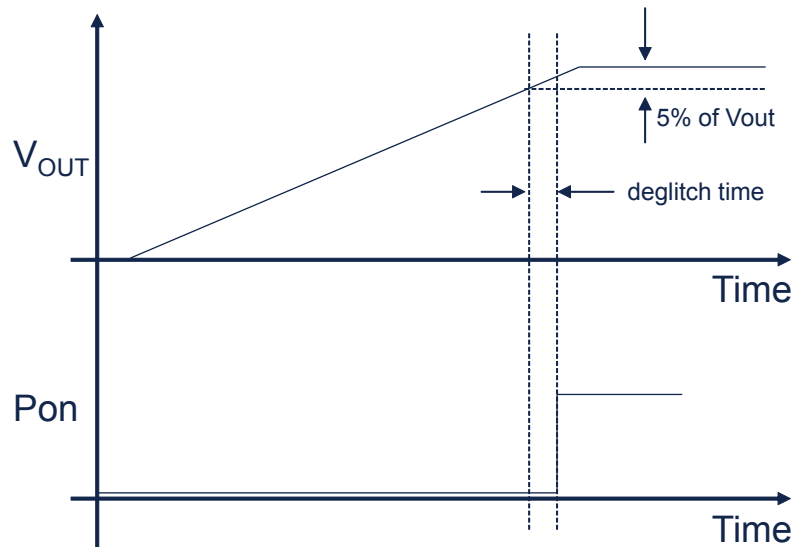
$$\Delta V_{out} = k \cdot I_{LOAD} \cdot R_{SENSE} \cdot (R_{CDC1}/R_{CDC2}) \quad (1)$$

where the parameter k is 18 and R<sub>CDC2</sub> depends on the cable resistance, with R<sub>CDC1</sub> being typically 10 kOhm.

The cable drop compensation loop should be very slow to avoid potential disturbance to the voltage loop. This can be achieved by a proper choice of R<sub>CDC1</sub> and C<sub>CDC</sub>.



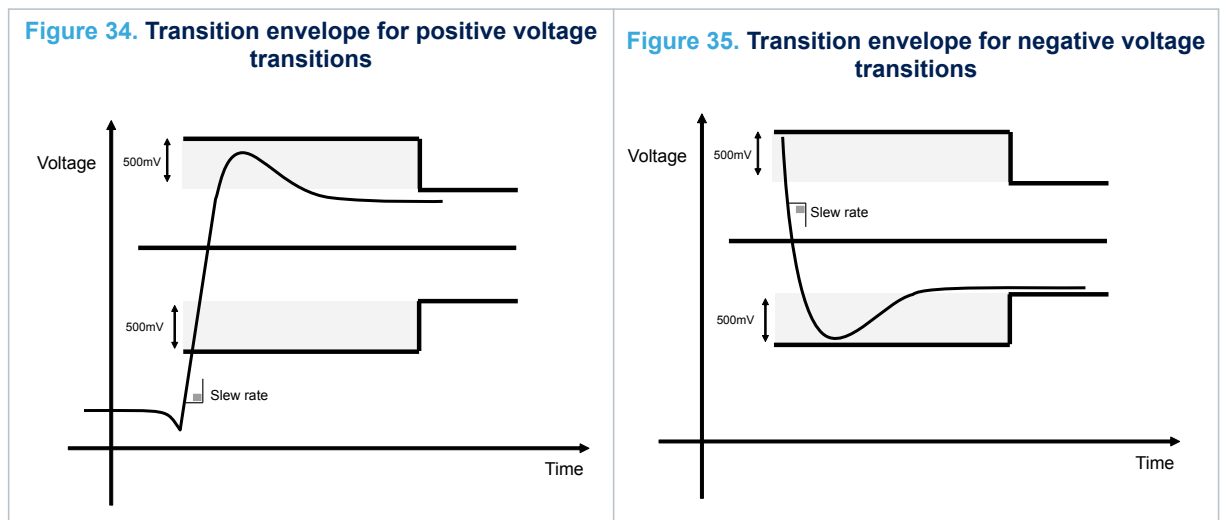
Figure 33. Deglitch time



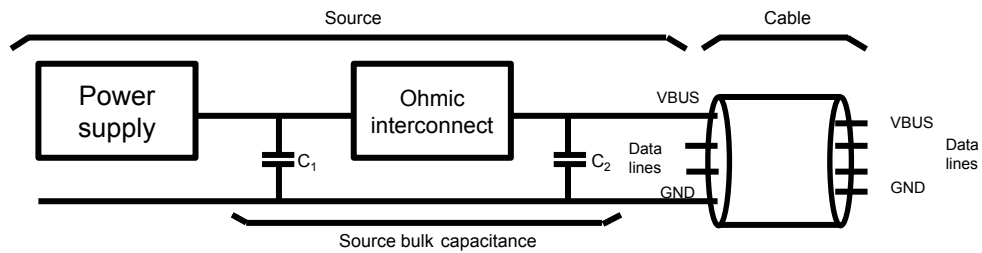
## 7.5 Vout transition

The Vout transitions are performed forcing the device into PWM mode in order to guarantee the max. slew rate reported in the EC table (see Table 6. Electrical characteristics).

During the transitions, the voltage level overcomes the limits defined by the  $\pm 2\%$  precision. Therefore an extra margin of 500 mV (max.) is allowed for about 300 ms and OVP is masked in order to avoid false alarms.



The maximum slew rate is guaranteed with the output capacitance value defined in the USB-PD spec. as follows:

**Figure 36. Placement of source bulk capacitance**


where  $C_1$  and  $C_2$  can be either a single capacitor, a capacitor bank or a distributed capacitance having a minimum value (total) of 10  $\mu\text{F}$ .

## 7.6 Clock dithering

To reduce EMI emission, the clock frequency dithers by 5% around its nominal value thus reducing the noise mean amplitude. This also randomly spreads the switching currents of many different STPD01 in a multi-port system.

## 7.7 Programmable watchdog

The STPD01 includes a watchdog function. The watchdog timer is enabled in the register 0x06. During this time, if there is no communication between the host and the STPD01, an interrupt is generated in the INT pin if not masked. Once the interrupt is activated, the host has 100 ms (default value) to send a command on the I<sup>2</sup>C to the STPD01 address, otherwise the registers 0x00, 0x01 and 0x05 are reset at their default values.

The interrupt is reset after the first I<sup>2</sup>C access.

This watchdog function can be disabled setting the bit 1 in register 0x06.

## 7.8 Protections

The device is equipped with some protections summarized in the following table

**Table 8. Protections**

| Protection                       | Function   | INT pin STATUS | Pon pin STATUS  |
|----------------------------------|--|----------------|---|
| OVP (overvoltage protection)     | Active as soon as the device is enabled and PVIN/VCC voltage valid is present (above the UVLO level), even during the soft-start. The protection is triggered when the voltage sensed on the VSNS pin rises over the OVP threshold. See Section 7.8.1 Overvoltage protection for more details.   | LOW            | Pon goes low if Vout rises above 5% of the value set (deglitched for 5 ms). Also, in case EN pin is low, the Pon is low |
| CC (constant current function)   | Active as soon as the device is in regulation (so, at the ends of the soft-start). This function is triggered when the output current is over the $CC_{th}$ threshold and the device acts to overcome the voltage regulation loop to limit the output current. The VOUT drops below the programmed level.  | LOW            | HIGH  |
| OTP (overtemperature protection) | Active as soon as the device is enabled and PVIN/VCC voltage valid is present (above the UVLO level), even during the soft-start. The protection is triggered when the internal temperature is over the OTP threshold and the device acts by suddenly switching off both HS and LS MOSFET. The VOUT bits (reg 0x00) and $I_{lim}$ bits (reg 0x01) are reset. Discharge is activated if enabled by the dedicated bit. | LOW            | HIGH  |

| Protection                     | Function  | INT pin STATUS | Pon pin STATUS |
|--------------------------------|---|----------------|----------------|
|                                | The device follows a soft-start procedure when the temperature is below 135 °C with default output voltage value.   |                |                |
| SCP (short-circuit protection) | Active as soon as the device is in regulation (at the ends of the soft-start). The protection is triggered when the output voltage is under the SCP threshold and the $I_{pk}$ threshold is detected. The device acts by suddenly switching off both HS and LS MOSFET.<br><br>The device follows a soft-start procedure after 300 ms with default output voltage value. The VOUT bits (reg 0x00) and $I_{lim}$ bits (reg 0x01) are reset.     | LOW            | HIGH           |
| IPK (inductor peak current)    | Active as soon as the device is enabled and PVIN/VCC voltage valid is present (above the UVLO level), even during the soft-start.<br><br>The condition is checked cycle-by-cycle on the high-side and triggered once the current cross the $I_{PK}$ threshold.<br><br>The device reacts switching asynchronously (independent from oscillator frequency) between $I_{pk}$ and $I_{valley}$ with a given slope, dependent on L and $C_{out}$ . | LOW            | HIGH           |

### 7.8.1 Overvoltage protection

Overvoltage protection behaves in different ways depending on the state of the device.

#### Case A) OV during Vout transition

- In case an OV occurs during a Vout transition, the output voltage must be reset to 5 V ( $V_{safe}$ ). Therefore, the following process applies:  
 OV event longer than deglitch time => REG 0x00 = 0x64 => after blanking time, the half-bridge is put in high impedance if the OV condition is still present.  
 In case OV lasts less than deglitch time, the event is filtered.

#### Case B) OV during steady-state

- Case B1) Vout=5 V**  
 If OV event is detected, the half-bridge is just put in high impedance until the condition disappears.
- Case B2) Vout different than 5 V**  
 The following process applies:  
 OV event longer than deglitch time => REG 0x00 = 0x64 => after blanking time, the half-bridge is put in high impedance if the OV condition is still present.  
 In case OV lasts less than deglitch time, the event is filtered.

## 7.9 Interrupt functionality

The interrupt output is activated on the edge of the fault and is reset once the fault disappears. To keep track of the fault, the corresponding bit in the INT\_LTCH register is set.

Such interrupt management process allows multiple interrupt tracking. The I<sup>2</sup>C master reads the INT\_LTCH register and optionally can read the INT\_STAT to check if some fault is still active.

## 7.10 Switching frequency

The STPD01 allows two possible programmable switching frequencies (by I<sup>2</sup>C): 500 kHz (default) and 750 kHz (reg 0x05 bit 2).

### 7.11 Pulse skip

At light loads, the device works in discontinuous conduction mode. Zero-cross comparator is implemented to detect when the coil current crosses the zero during  $T_{OFF}$  (i.e. low-side MOSFET on). During the sleep periods of the DCM operations both power MOSFETs are off and the efficiency is improved according to that. Moreover, the sleep period is a function of the load.

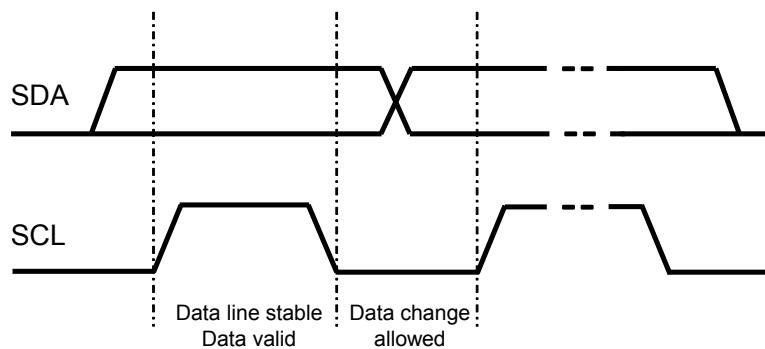
Since the device works at almost fixed frequency (only 500 kHz or 750 kHz are selectable by I<sup>2</sup>C) with fixed minimum  $T_{on}$  typically 100 ns and wide PVIN range, up to 26.4 V, pulse skipping operation occurs to guarantee the proper regulation to light load (or no load conditions).

In addition, the pulse skip threshold (i.e. the voltage the device enters the pulse skip operation) can be properly selected to optimize the efficiency at light loads.

### 7.12 Bus timing

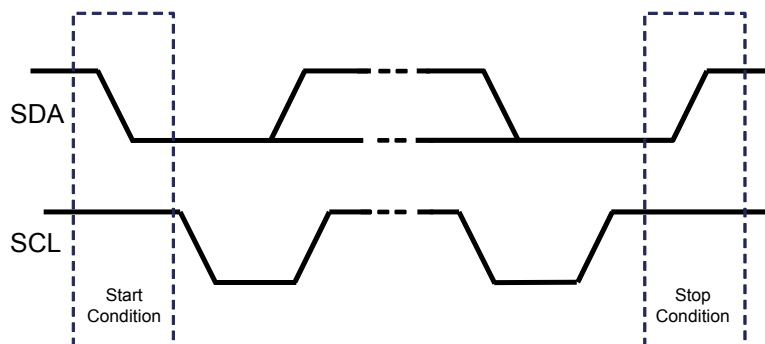
As shown in the figure below, the data on the SDA line must be stable during the high semi-period of the clock. The high and low-state of the data line can only change when the clock signal on the SCL line is low.

**Figure 37. Data transfer validity**



Each bus transaction begins with a “START” command which is defined as SDA transition from 1 to 0 with SCL high, and it is finished with a “STOP” command, which is defined as SDA transition from 0 to 1 with SCL high, as shown in Figure 38. [START and STOP commands](#).

**Figure 38. START and STOP commands**



The master generates the start command and transmits the 7-bit address and the read/write bit on SDA line. All slave devices compare the address sent by the master to their internal fixed addresses. Only the slave device, with a matching address, generates an ACK by pulling the SDA line low during the entire high period of the ninth SCL clock. The acknowledge bit is used to indicate a successful byte transfer.

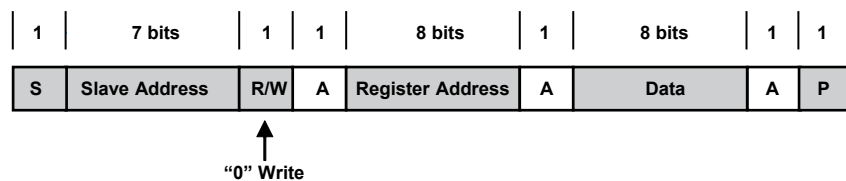
The master then generates further SCL cycles to either transmit data to the slave or receive data from the slave. At the end of the data transfer, the master generates the stop command and the bus is released and all devices wait for a new start command.

### 7.12.1 Read and write commands

The format of I<sup>2</sup>C commands is described below. All figures use common format and symbols. Every data word consists of eight bits with most significant bit first and least significant bit last.

**Write command** to the transceiver device is described by the following figure. It is possible to write to several consecutive registers during one write command.

**Figure 39. Write command**



- From Master to Slave
  - From Slave to Master
- A = acknowledge (SDA LOW)  
S = START condition  
P = STOP condition

**Read command** consists of dummy write to set the proper address of a register followed by a real read sequence.

**Figure 40. Read command**



- From Master to Slave
  - From Slave to Master
- A = acknowledge (SDA LOW)  
S = START condition  
P = STOP condition  
Sr = Repeated Start

The master sends a “Repeated Start” after sending the register address and before resending the slave address. The “Repeated Start” is defined as SDA transition from 1 to 0 with SCL high.

### 7.12.2 I<sup>2</sup>C address selection

The I<sup>2</sup>C address can be selected using the ADD pin to allow multiple devices to be connected on the same bus. The address is composed as below:

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|------|------|------|------|------|------|------|------|
| 0    | 0    | 0    | 0    | 1    | ADD1 | ADD0 | R/W  |

There are four possible configurations as reported below:

**Table 9. I<sup>2</sup>C address configuration**

| ADD connection   | Bit ADD1 and ADD0 |
|------------------|-------------------|
| VAUX (max 5.5 V) | 00                |
| GND              | 01                |
| SDA              | 10                |
| SCL              | 11                |



## 8 Control register description

### 8.1 Register map

**Table 10. Configuration bits**

| Content             | # of configurations | Comments  |
|---------------------|---------------------|---|
| Vout                | 240 (8 bit)         | 3 V to 5.9 V with 20 mV step, 5.9 V to 11 V with 100 mV step, 11 V to 20 V with 200 mV step |
| Ilim                | 25 (5 bit)          | From 0.1 A to 3 A with 100 mA steps (flag_50 mA can be used to obtain 50 mA steps)          |
| Interrupt mask      | 7 (7 bit)           | OVP, CC, SCP, Pon, WD, OTP, OTW, IPK  |
| Interrupt status    | 7 (7 bit)           | Interrupt status  |
| Interrupt latch     | 7 (7 bit)           | Interrupt latch   |
| Auto-discharge      | 2 (1 bit)           | Auto-discharge enable/disable   |
| Dithering           | 2 (1 bit)           | Dithering enable/disable  |
| Switching frequency | 2 (1 bit)           | 500 kHz, 750 kHz  |
| Cable drop comp.    | 3 (2 bit)           | OFF, full   |
| Enable watchdog     | 2 (1 bit)           | Enable/disable  |
| Watchdog            | 4 (2 bit)           | 100 ms, 500 ms, 1 s, 5 s  |
| Enable              | 2 (1 bit)           | ON/OFF (see Section 7 Operation description)  |

**Table 11. Register map summary**

| ADDR | R/W | Bit7        | Bit6        | Bit5        | Bit4        | Bit3        | Bit2        | Bit1        | Bit0        |
|------|-----|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 0x00 | R/W | Vout(7)     | Vout(6)     | Vout(5)     | Vout(4)     | Vout(3)     | Vout(2)     | Vout(1)     | Vout(0)     |
| 0x01 | R/W | Flag_50ma   | Not used    | Not used    | ILIM(4)     | ILIM(3)     | ILIM(2)     | ILIM(1)     | ILIM(0)     |
| 0x02 | R   | INT_STAT(7) | INT_STAT(6) | INT_STAT(5) | INT_STAT(4) | INT_STAT(3) | INT_STAT(2) | INT_STAT(1) | INT_STAT(0) |
| 0x03 | R/C | INT_LTC(7)  | INT_LTC(6)  | INT_LTC(5)  | INT_LTC(4)  | INT_LTC(3)  | INT_LTC(2)  | INT_LTC(1)  | INT_LTC(0)  |
| 0x04 | R/W | INT_MASK(7) | INT_MASK(6) | INT_MASK(5) | INT_MASK(4) | INT_MASK(3) | INT_MASK(2) | INT_MASK(1) | INT_MASK(0) |
| 0x05 | R/W | WTCHDG(1)   | WTCHDG(0)   | Not used    | CDC(1)      | CDC(0)      | SW_FREQ     | DITH        | AUTO_DIS    |
| 0x06 | R/W | Not used    | Not used    | Not used    | Not used    | Not used    | Not used    | WD_EN       | DIG_EN      |

R: read; R/W: read and write; R/C: cleared when read.

## 8.2 Register description

### 8.2.1 Register 0x00

The register 0x00 is used to set the output voltage configuration. Its default value (reset) is 0x64.

**Table 12. 0x00 register description**

| Hex value | Voltage value (V) | Hex value | Voltage value (V) | Hex value | Voltage value (V) | Hex value | Voltage value (V) | Hex value | Voltage value (V) |
|-----------|-------------------|-----------|-------------------|-----------|-------------------|-----------|-------------------|-----------|-------------------|
| 0x00      | 3                 | 0x30      | 3.96              | 0x66      | 5.04              | 0x9C      | 7                 | 0xD2      | 13.8              |
| 0x01      | 3.02              | 0x31      | 3.98              | 0x67      | 5.06              | 0x9D      | 7.1               | 0xD3      | 14                |
| 0x02      | 3.04              | 0x32      | 4                 | 0x68      | 5.08              | 0x9E      | 7.2               | 0xD4      | 14.2              |
| 0x03      | 3.06              | 0x33      | 4.02              | 0x69      | 5.1               | 0x9F      | 7.3               | 0xD5      | 14.4              |
| 0x04      | 3.08              | 0x34      | 4.04              | 0x6A      | 5.12              | 0xA0      | 7.4               | 0xD6      | 14.6              |
| 0x05      | 3.1               | 0x35      | 4.06              | 0x6B      | 5.14              | 0xA1      | 7.5               | 0xD7      | 14.8              |
| 0x06      | 3.12              | 0x36      | 4.08              | 0x6C      | 5.16              | 0xA2      | 7.6               | 0xD8      | 15                |
| 0x07      | 3.14              | 0x37      | 4.1               | 0x6D      | 5.18              | 0xA3      | 7.7               | 0xD9      | 15.2              |
| 0x08      | 3.16              | 0x38      | 4.12              | 0x6E      | 5.2               | 0xA4      | 7.8               | 0xDA      | 15.4              |
| 0x09      | 3.18              | 0x39      | 4.14              | 0x6F      | 5.22              | 0xA5      | 7.9               | 0xDB      | 15.6              |
| 0x0A      | 3.2               | 0x3A      | 4.16              | 0x70      | 5.24              | 0xA6      | 8                 | 0xDC      | 15.8              |
| 0x0B      | 3.22              | 0x3B      | 4.18              | 0x71      | 5.26              | 0xA7      | 8.1               | 0xDD      | 16                |
| 0x0C      | 3.24              | 0x3C      | 4.2               | 0x72      | 5.28              | 0xA8      | 8.2               | 0xDE      | 16.2              |
| 0x0D      | 3.26              | 0x3D      | 4.22              | 0x73      | 5.3               | 0xA9      | 8.3               | 0xDF      | 16.4              |
| 0x0E      | 3.28              | 0x3E      | 4.24              | 0x74      | 5.32              | 0xAA      | 8.4               | 0xE0      | 16.6              |
| 0x0F      | 3.3               | 0x3F      | 4.26              | 0x75      | 5.34              | 0xAB      | 8.5               | 0xE1      | 16.8              |
| 0x10      | 3.32              | 0x40      | 4.28              | 0x76      | 5.36              | 0xAC      | 8.6               | 0xE2      | 17                |
| 0x11      | 3.34              | 0x41      | 4.3               | 0x77      | 5.38              | 0xAD      | 8.7               | 0xE3      | 17.2              |
| 0x12      | 3.36              | 0x42      | 4.32              | 0x78      | 5.4               | 0xAE      | 8.8               | 0xE4      | 17.4              |
| 0x13      | 3.38              | 0x43      | 4.34              | 0x79      | 5.42              | 0xAF      | 8.9               | 0xE5      | 17.6              |
| 0x14      | 3.4               | 0x44      | 4.36              | 0x7A      | 5.44              | 0xB0      | 9                 | 0xE6      | 17.8              |
| 0x15      | 3.42              | 0x45      | 4.38              | 0x7B      | 5.46              | 0xB1      | 9.1               | 0xE7      | 18                |
| 0x16      | 3.44              | 0x46      | 4.4               | 0x7C      | 5.48              | 0xB2      | 9.2               | 0xE8      | 18.2              |
| 0x17      | 3.46              | 0x47      | 4.42              | 0x7D      | 5.5               | 0xB3      | 9.3               | 0xE9      | 18.4              |
| 0x18      | 3.48              | 0x48      | 4.44              | 0x7E      | 5.52              | 0xB4      | 9.4               | 0xEA      | 18.6              |
| 0x19      | 3.5               | 0x49      | 4.46              | 0x7F      | 5.54              | 0xB5      | 9.5               | 0xEB      | 18.8              |
| 0x1A      | 3.52              | 0x4A      | 4.48              | 0x80      | 5.56              | 0xB6      | 9.6               | 0xEC      | 19                |
| 0x1B      | 3.54              | 0x4B      | 4.5               | 0x81      | 5.58              | 0xB7      | 9.7               | 0xED      | 19.2              |
| 0x1C      | 3.56              | 0x4C      | 4.52              | 0x82      | 5.6               | 0xB8      | 9.8               | 0xEE      | 19.4              |
| 0x1D      | 3.58              | 0x4D      | 4.54              | 0x83      | 5.62              | 0xB9      | 9.9               | 0xEF      | 19.6              |
| 0x1E      | 3.6               | 0x4E      | 4.56              | 0x84      | 5.64              | 0xBA      | 10                | 0xF0      | 19.8              |
| 0x1F      | 3.62              | 0x4F      | 4.58              | 0x85      | 5.66              | 0xBB      | 10.1              | 0xF1      | 20                |
| 0x20      | 3.64              | 0x50      | 4.6               | 0x86      | 5.68              | 0xBC      | 10.2              |           |                   |
| 0x21      | 3.66              | 0x51      | 4.62              | 0x87      | 5.7               | 0xBD      | 10.3              |           |                   |

| Hex value | Voltage value (V) | Hex value | Voltage value (V) | Hex value | Voltage value (V) | Hex value | Voltage value (V) | Hex value | Voltage value (V) |
|-----------|-------------------|-----------|-------------------|-----------|-------------------|-----------|-------------------|-----------|-------------------|
| 0x22      | 3.68              | 0x52      | 4.64              | 0x88      | 5.72              | 0xBE      | 10.4              |           |                   |
| 0x23      | 3.7               | 0x53      | 4.66              | 0x89      | 5.74              | 0xBF      | 10.5              |           |                   |
| 0x24      | 3.72              | 0x54      | 4.68              | 0x8A      | 5.76              | 0xC0      | 10.6              |           |                   |
| 0x25      | 3.74              | 0x55      | 4.7               | 0x8B      | 5.78              | 0xC1      | 10.7              |           |                   |
| 0x26      | 3.76              | 0x56      | 4.72              | 0x8C      | 5.8               | 0xC2      | 10.8              |           |                   |
| 0x27      | 3.78              | 0x57      | 4.74              | 0x8D      | 5.82              | 0xC3      | 10.9              |           |                   |
| 0x28      | 3.8               | 0x58      | 4.76              | 0x8E      | 5.84              | 0xC4      | 11                |           |                   |
| 0x29      | 3.82              | 0x59      | 4.78              | 0x8F      | 5.86              | 0xC5      | 11.2              |           |                   |
| 0x2A      | 3.84              | 0x5A      | 4.8               | 0x90      | 5.88              | 0xC6      | 11.4              |           |                   |
| 0x2B      | 3.86              | 0x5B      | 4.82              | 0x91      | 5.9               | 0xC7      | 11.6              |           |                   |
| 0x2C      | 3.88              | 0x5C      | 4.84              | 0x92      | 6                 | 0xC8      | 11.8              |           |                   |
| 0x2D      | 3.9               | 0x5D      | 4.86              | 0x93      | 6.1               | 0xC9      | 12                |           |                   |
| 0x2E      | 3.92              | 0x5E      | 4.88              | 0x94      | 6.2               | 0xCA      | 12.2              |           |                   |
| 0x2F      | 3.94              | 0x5F      | 4.9               | 0x95      | 6.3               | 0xCB      | 12.4              |           |                   |
| 0x30      | 3.96              | 0x60      | 4.92              | 0x96      | 6.4               | 0xCC      | 12.6              |           |                   |
| 0x31      | 3.98              | 0x61      | 4.94              | 0x97      | 6.5               | 0xCD      | 12.8              |           |                   |
| 0x32      | 4                 | 0x62      | 4.96              | 0x98      | 6.6               | 0xCE      | 13                |           |                   |
| 0x33      | 4.02              | 0x63      | 4.98              | 0x99      | 6.7               | 0xCF      | 13.2              |           |                   |
| 0x34      | 4.04              | 0x64      | 5                 | 0x9A      | 6.8               | 0xD0      | 13.4              |           |                   |
| 0x35      | 4.06              | 0x65      | 5.02              | 0x9B      | 6.9               | 0xD1      | 13.6              |           |                   |

### 8.2.2 Register 0x01

The register 0x01 is used to set the output current limitation configuration. Its default value (reset) is 0x04, which is 500 mA.

**Table 13. 0x01 register description**

| Hex value | I <sub>LIM</sub> (mA) | Hex value | I <sub>LIM</sub> (mA) |
|-----------|-----------------------|-----------|-----------------------|
| 0x00      | 100                   | 0x0F      | 1600                  |
| 0x01      | 200                   | 0x10      | 1700                  |
| 0x02      | 300                   | 0x11      | 1800                  |
| 0x03      | 400                   | 0x12      | 1900                  |
| 0x04      | 500                   | 0x13      | 2000                  |
| 0x05      | 600                   | 0x14      | 2100                  |
| 0x06      | 700                   | 0x15      | 2200                  |
| 0x07      | 800                   | 0x16      | 2300                  |
| 0x08      | 900                   | 0x17      | 2400                  |
| 0x09      | 1000                  | 0x18      | 2500                  |
| 0x0A      | 1100                  | 0x19      | 2600                  |
| 0x0B      | 1200                  | 0x1A      | 2700                  |
| 0x0C      | 1300                  | 0x1B      | 2800                  |
| 0x0D      | 1400                  | 0x1C      | 2900                  |
| 0x0E      | 1500                  | 0x1D      | 3000                  |

### 8.2.3 Interrupt registers: 0x02, 0x03, 0x04

The registers 0x02, 0x03 and 0x04 are used for the interrupt management and in particular:

0x02: interrupt status (reset value 0x00), bit at 0 means “no interrupt”

0x03: interrupt latch (reset value 0x00), bit at 0 means “not latched”

0x04: interrupt mask (reset value 0x0E), bit at 0 means “not masked”

The single bits are organized as follows:

**Table 14. Interrupt register description**

| Bit | Function                         | Notes                       |
|-----|----------------------------------|-----------------------------|
| 0   | Overvoltage protection           |                             |
| 1   | Constant current function        |                             |
| 2   | Short-circuit protection         |                             |
| 3   | Power-on                         |                             |
| 4   | Watchdog                         |                             |
| 5   | Overtemperature protection       | Junction temperature 165 °C |
| 6   | Overtemperature warning          | Junction temperature 145 °C |
| 7   | Inductor peak current protection |                             |

### 8.2.4 Register 0x05

The register 0x05 is used for services and in particular:

| Bit | Function                | Notes  |
|-----|-------------------------|--|
| 0   | Discharge               | 0: OFF<br>1: ON (default)                                |
| 1   | Dithering               | 0: OFF (default)<br>1: ON                                |
| 2   | Switching frequency     | 0: 500 kHz (default)<br>1: 750 kHz                       |
| 4:3 | Cable drop compensation | 00: OFF (default)<br>10: Full<br>01: N/A<br>11: N/A      |
| 5   | Not used                | -  |
| 7:6 | Watchdog timer          | 00: 100 ms (default)<br>01: 500 ms<br>10: 1 s<br>11: 5 s |

Default value (reset) is 0x01.

### 8.2.5 Register 0x06

The register 0x06 is only used for digital enable.

| Bit | Function        | Notes                     |
|-----|-----------------|---------------------------|
| 0   | Digital enable  | 0: OFF<br>1: ON (default) |
| 1   | Watchdog enable | 0: OFF (default)<br>1: ON |
| 7:2 | To be defined   | To be defined             |

Default value (reset) is 0x01.

## 9 Application notes

### 9.1 Board layout guidelines

#### Guidelines

The DC-DC converter area is very sensitive, and it is necessary to pay attention to the layout of this part. The DC-DC converter generates GND noise that can get coupled on surrounding ground reducing the sensitivity, and high-frequency components can be coupled onto RF part. So, to ensure a correct layout it is necessary to:

- Provide efficient filtering by placing capacitors as close as possible
- Reduce parasitic ensuring wide and short connections.

#### Four-layer boards

A four-layer board is strongly recommended. Put the ground layer very close to the top layer to obtain a good ground plane reference. A thickness between the top layer and ground layer of 0.2 mm or 0.3 mm is suggested. Put a ground plane internally to reduce the coupling between the traces

If it is not possible to use a four-layer board, it is necessary to fill the area under the phase node of the board with ground metal to reduce or eliminate radiation emissions. Board routing and wiring should not be placed in this region to prevent coupling effects and to ensure a good ground reference plane to the RF parts.

#### Ground plane

Any switch mode power supply requires a good PCB layout in order to achieve the maximum performance. Component placement, and GND trace routing and width are the major issues. Basic rules commonly used for DC-DC converters for good PCB layout should be followed. All traces carrying current should be drawn on the PCB as short and as thick as possible. This should be done to minimize resistive and inductive parasitic effects, and increase system efficiency. Suggested PCB (ring) ground plane to avoid spikes on the output voltage. Good soldering of the exposed pad helps on this issue.

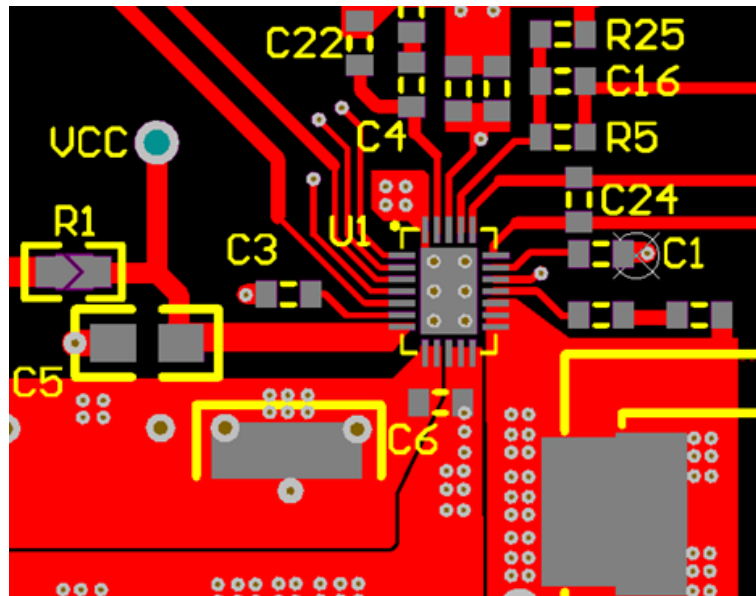
Connect all the ground metallization and/or layers with as many vias as possible. Ground vias between layers should be added liberally throughout the RF portion of the PCB. This helps prevent accrual of parasitic ground inductance due to ground-current return paths. The vias also help to prevent cross-coupling from RF and other signal lines across the PCB.

The layers assigned to system bias (DC supply) and ground must be considered in terms of the return current for the components. The general guidance is not to have signals routed on layers between the bias layer and the ground layer.

#### Capacitors placing

Particular care has to be taken in the placement of the supply voltage filtering capacitors. It is, in fact, important to ensure efficient filtering placing these capacitors as close as possible from their dedicated pins on the VIN (C6), VCC (C5), VREG (C1), VHDRIVE (C3), VBOOT (C14) and VSNS (C16).

Figure 41. Capacitor placing

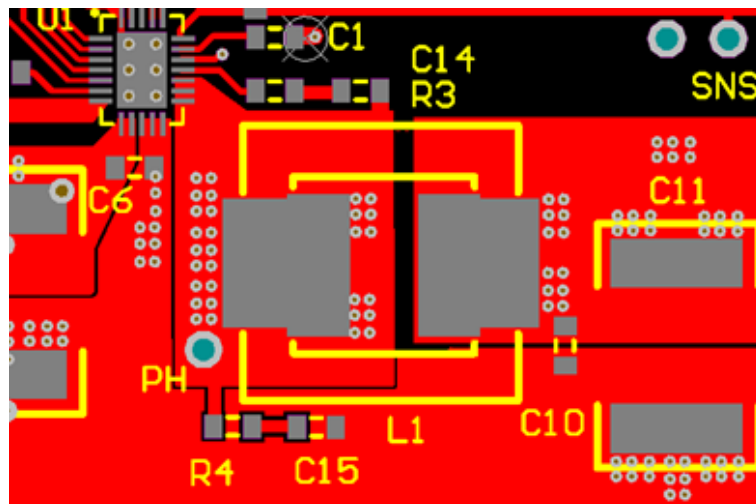


The layout of decoupling capacitors is extremely important to minimize the induction loop formed between the capacitor and the IC power and ground. The vias should be placed on the side of the capacitor lands, not the ends. The vias should be located at minimum keepout distance and connected to the capacitor lands with a wide trace - at least as wide as the via pad. Vias of opposite polarity should be placed as close together as possible (minimum keepout distance) and vias of the same polarity should be kept separated as much as possible. If space allows, a second pair of vias on the opposite side of the capacitor may be added to reduce the inductance further.

#### Inductor placing

The DC-DC converter inductor has to be placed as close as possible with traces as short and as thick as possible. This should be done to minimize resistive parasitic effects, and increase system efficiency.

Figure 42. Inductor placing



#### Vias placing

It is crucial to connect very well the ground of the exposed pad of the QFN24L to the ground on the application board. Therefore many vias are necessary to be sure that the parasitic inductor introduced from each via is negligible.

Connect all the ground metallization and/or layers with as many vias as possible. The vias should be located at minimum keepout distance; this should be done to minimize resistive and inductive parasitic effects.

**Reference voltage**

V<sub>ref</sub> is generated by an internal LDO. Place a decoupling capacitor very close. Use good capacitor layout techniques. Do not route the V<sub>ref</sub> trace near noisy traces or planes.

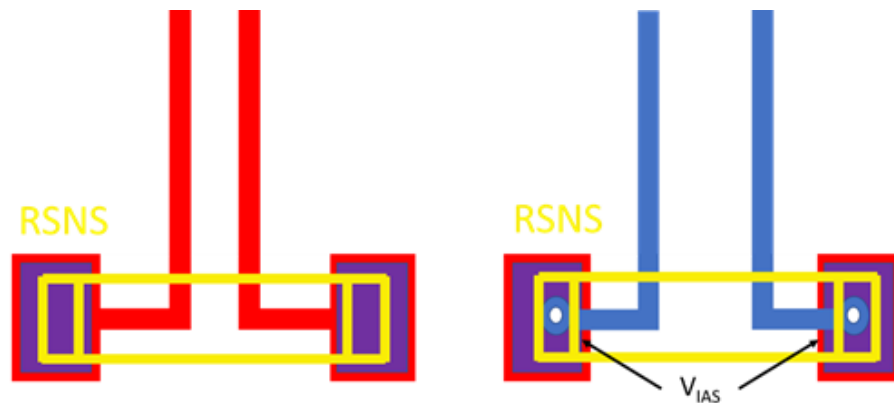
**High-side driver supply**

V<sub>DRIVEH</sub> is generated by an internal LDO. Place a decoupling capacitor very close. Use good capacitor layout techniques. Do not route the V<sub>ref</sub> trace near noisy traces or planes.

**Current sensing**

With small value sense resistors, trace resistance shared with the load can cause significant errors. It is recommended to connect the sense resistor pads directly to the ISNS+ and ISNS- pins using “Kelvin” or “4-wire” connection techniques as shown in Figure 43. RSNS Kelvin connection (sx sense in the same layer, at dx with vias top to bottom). Run two dedicated traces with decent width in parallel (close to each other to minimize the loop area) from the two terminals of the current-sensing resistor to the IC. Place in the differential mode and avoid sense lines pass through noisy areas, such as switch nodes.

**Figure 43. RSNS Kelvin connection (sx sense in the same layer, at dx with vias top to bottom)**

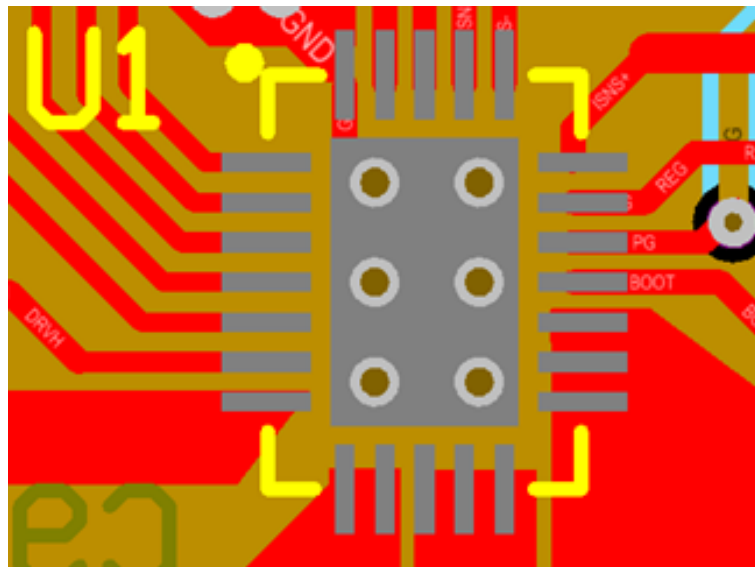


The ISNS+ and ISNS- pins tolerate a DC voltage of -0.3 V with respect to GND. If VISNS+ and VISNS- pins are forecasted to go below the DC value for short AC pulses, the source current must be limited to a max. of 10 mA.

**Thermal aspects**

The STPD01 power dissipation inside the IC is mainly due to the DC-DC integrated MOSFET power loss. The heat generated due to this power dissipation level requires a suitable heatsink to keep the junction temperature below the overtemperature protection threshold at the rated ambient temperature. Try, where possible, to increase the number of power planes connected, at least below the IC position, to improve the heat dissipation. However, different layouts are also possible. Basic principles suggest keeping the IC and its ground exposed pad approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.



**Figure 44. Thermal aspects**


## 9.2 Selecting components for the application

This section provides information to assist in the selection of the most appropriate components for the intended application.

### Output capacitor

The output capacitor is very important to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the coil, but this increases the current ripple. Therefore, to reduce the output voltage ripple a low ESR capacitor is required.

The output voltage ripple ( $V_{OUT\_RIPPLE}$ ), in continuous mode, is:

$$V_{OUT\_RIPPLE} = \Delta I \times \left( C_{OUT\_ESR} + \frac{1}{8 \times C_{OUT} \times F_{SW}} \right) \quad (3)$$

where  $\Delta I$  is the ripple current and  $F_{SW}$  is the switching frequency.

### Inductor

The inductor value is very important because it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20-40% of  $I_{OUT\_MAX}$ , which is 0.6-1.2 A with  $I_{OUT\_MAX} = 3$  A. The approximate inductor value is obtained using the following formula:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \times T_{ON} \quad (4)$$

where  $T_{ON}$  is the ON time of the internal switch, given by  $D \cdot T$ .

For example, with  $V_{OUT} = 5$  V,  $V_{IN} = 24$  V,  $F_{SW} = 500$  kHz and  $\Delta I_{OUT} = 0.8$  A, the inductor value is around 10  $\mu$ H.

The peak current through the inductor is given by:

$$I_{PK} = I_{OUT} + \frac{\Delta I}{2} \quad (5)$$

It can be observed that if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. So, for fixed peak current protection, a higher value of the inductor allows a higher value for the output current.

### Thermal considerations

The dissipated power of the device is given by three separate factors:

- Switching losses due to the  $R_{DS(on)}$ . These are equal to:

$$P_{HS} = R_{DS(on)} I_{OUT}^2 D \quad (6)$$

and

$$P_{LS} = R_{DS(on)} I_{OUT}^2 (1 - D) \quad (7)$$

where D is the duty cycle of the application.

**Note:** *The duty cycle is theoretically given by the ratio between V<sub>OUT</sub> and V<sub>IN</sub>, but in practice it is significantly higher than this value to compensate for the losses of the whole application. For this reason, the switching losses related to the R<sub>DS(on)</sub> increase compared to an ideal case.*

- On and OFF switching losses. These are given by the following relation:

$$P_{SW} = V_{IN} I_{OUT} \frac{(T_{rise} + T_{fall})}{2} F_{SW} \quad (8)$$

where T<sub>rise</sub> and T<sub>fall</sub> are the overlap times of the voltage across the power switch and the current flowing into it during the turn-on and turn-off phases.

- Quiescent current losses:

$$P_Q = V_{IN} \times I_{IN} \quad (9)$$

where I<sub>N</sub> is the supply current.

$$P_{TOT} = P_Q + P_{SW} + P_{HS} + P_{LS} \quad (10)$$

The junction temperature of the device is:

$$T_J = T_A + R_{thJ-A} \cdot P_{TOT} \quad (11)$$

where T<sub>A</sub> is the ambient temperature and R<sub>thJ-A</sub> is the junction to ambient thermal resistance.

Considering that the device, mounted on the board with a good ground plane, has a thermal resistance junction to ambient (R<sub>thJ-A</sub>) of about 31 °C/W.

It is also possible to estimate the junction temperature directly from the efficiency measures acquired on a stationary application condition.

Considering that the power losses are given by:

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (12)$$

Neglecting the AC losses of the selected inductor, the power losses are given by:

$$P_{LOSS} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT} - DCR1 \cdot I_{OUT} \quad (13)$$

Therefore, the junction temperature T<sub>J</sub> can be calculated as:

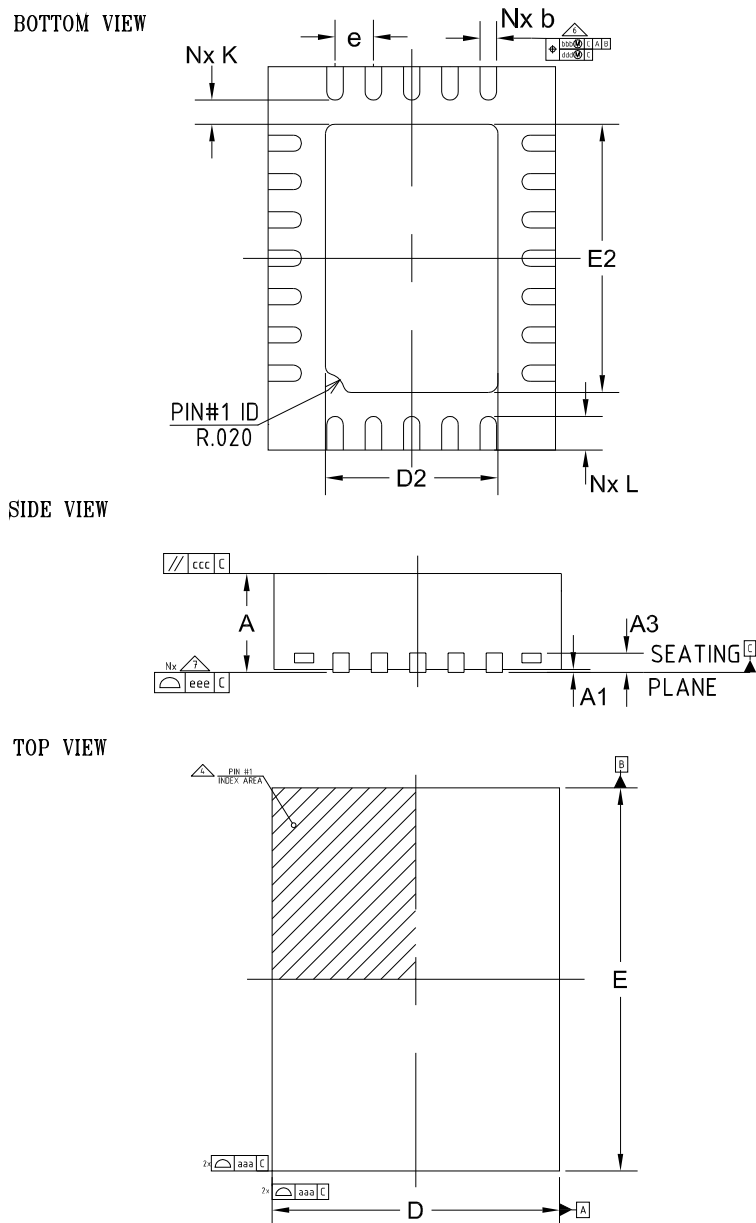
$$T_J = T_A + R_{thJA} \cdot P_{LOSS} \quad (14)$$

## 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 10.1 QFN24L (3 x 4 x 1.0 mm) package information

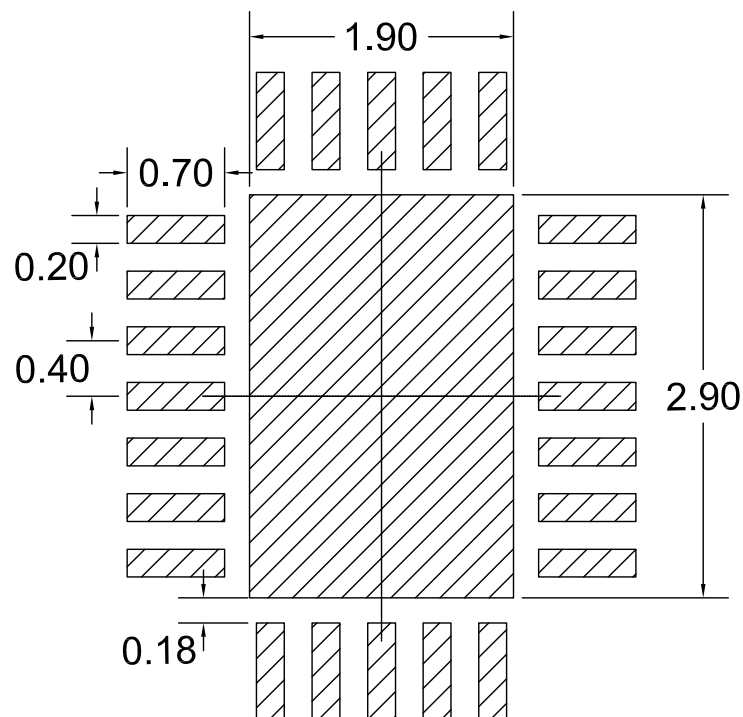
Figure 45. QFN24L (3 x 4 x 1.0 mm) package outline



**Table 15. QFN24L (3 x 4 x 1.0 mm) mechanical data**

| Symbol | mm        |      |      |
|--------|-----------|------|------|
|        | Min.      | Typ. | Max. |
| A      | 0.80      | 0.90 | 1.00 |
| A1     | 0.00      | 0.02 | 0.05 |
| A3     | 0.20 REF. |      |      |
| b      | 0.15      | 0.20 | 0.25 |
| D      | 3.00 BSC  |      |      |
| E      | 4.00 BSC  |      |      |
| e      | 0.40 BSC  |      |      |
| D2     | 1.65      | 1.80 | 1.90 |
| E2     | 2.65      | 2.80 | 2.90 |
| K      | 0.15      |      |      |
| L      | 0.25      | 0.35 | 0.45 |
| N      | 24        |      |      |

**Note:** *N* is the total number of terminals. Dimension *b* applies to metallized terminal. If the terminal has a radius on its end dimension *b* should not be measured in that radius area.

**Figure 46. QFN24L (3 x 4 x 1.0 mm) recommended footprint**


## Revision history

**Table 16. Document revision history**

| Date        | Version | Changes   |
|-------------|---------|---|
| 02-Oct-2020 | 1       | Initial release.  |
| 07-Apr-2021 | 2       | Updated: DC and Cable drop values in Table 6, VAUX in Table 9 and Figure 45.  |
| 06-May-2021 | 3       | Updated Table 6. Electrical characteristics and Figure 7. System P <sub>LOSS</sub> (V <sub>in</sub> = V <sub>CC</sub> = 24 V, CC = 0x1F, F <sub>sw</sub> = 750 kHz) |

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