

# HEF40175B

## Quad D-type flip-flop

Rev. 10 — 29 November 2021

Product data sheet

## 1. General description

The HEF40175B is a quad positive edge triggered D-type flip-flop with four data ( $D_n$ ) inputs, common clock (CP) and asynchronous master reset ( $\overline{MR}$ ) inputs, and complementary  $Q_n$  and  $\overline{Q}_n$  outputs. When  $\overline{MR}$  is HIGH data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. When LOW,  $\overline{MR}$  resets all flip-flops ( $Q_n = \text{LOW}$ ,  $\overline{Q}_n = \text{HIGH}$ ), independent of CP and  $D_n$ . Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

## 2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
- Specified from -40 °C to +85°C and from -40 °C to +125 °C

## 3. Applications

- Shift registers
- Buffer/storage register
- Pattern generator

## 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF40175BT	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF40175BTT	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

### 5. Functional diagram

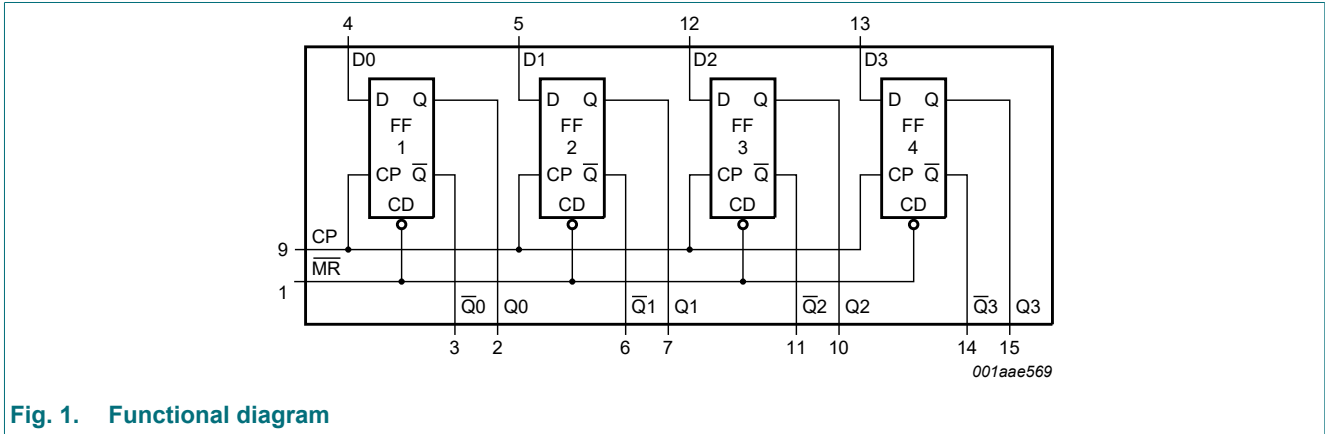


Fig. 1. Functional diagram

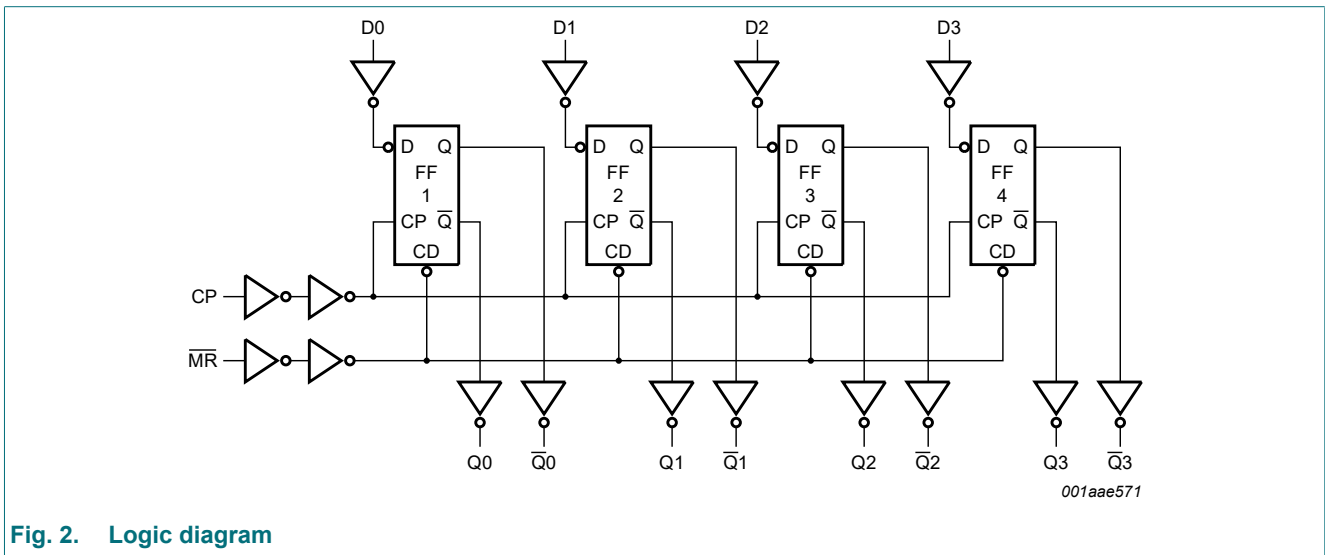


Fig. 2. Logic diagram

## 6. Pinning information

### 6.1. Pinning

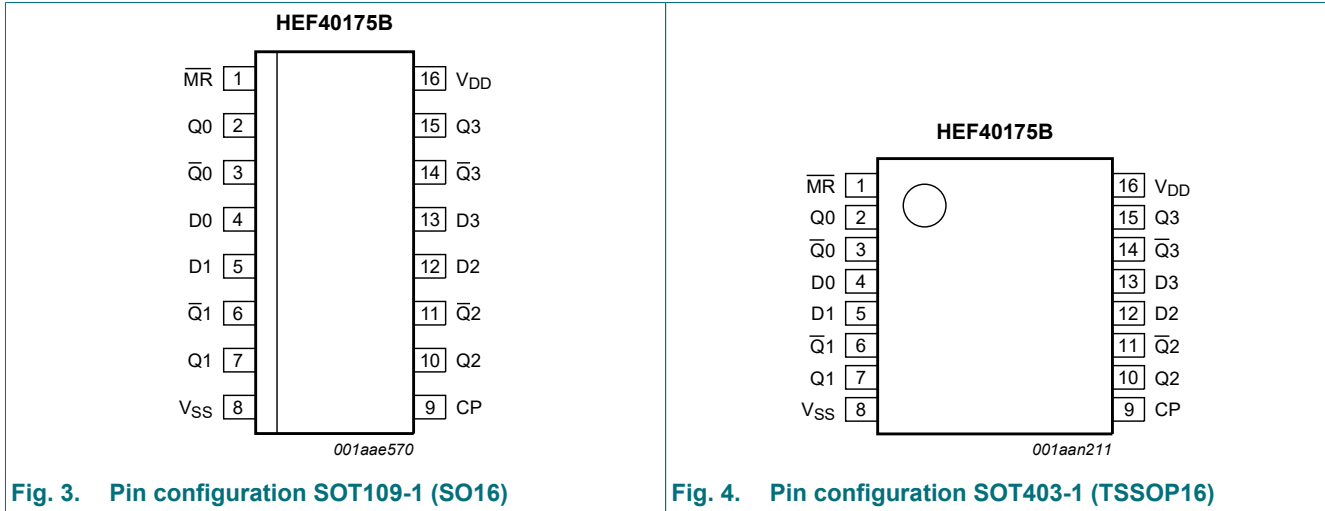


Fig. 3. Pin configuration SOT109-1 (SO16)

Fig. 4. Pin configuration SOT403-1 (TSSOP16)

### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
MR	1	master reset input (active LOW)
Q0, Q1, Q2, Q3	2, 7, 10, 15	buffered output
Q0, Q1, Q2, Q3	3, 6, 11, 14	complementary buffered output
D0, D1, D2, D3	4, 5, 12, 13	data input
V <sub>SS</sub>	8	ground supply voltage
CP	9	clock input (LOW-to-HIGH edge-triggered)
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = positive-going transition; ↓ = negative-going transition.

Input			Output	
CP	Dn	MR	Qn	Qn
↑	H	H	H	L
↑	L	H	L	H
↓	X	H	no change	no change
X	X	L	L	H

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

- [1] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		T <sub>amb</sub> = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>O</sub>   < 1 μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>O</sub>   < 1 μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub>   < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level output current	V <sub>O</sub> = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V <sub>O</sub> = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V <sub>O</sub> = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V <sub>O</sub> = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I <sub>OL</sub>	LOW-level output current	V <sub>O</sub> = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V <sub>O</sub> = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I <sub>I</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>DD</sub>	supply current	all valid input combinations;  I <sub>O</sub>   = 0 A	5 V	-	1.0	-	1.0	-	30	-	30	μA
			10 V	-	2.0	-	2.0	-	60	-	60	μA
			15 V	-	4.0	-	4.0	-	120	-	120	μA
C <sub>I</sub>	input capacitance		-	-	-	-	7.5	-	-	-	pF	

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$  unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula[1]	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	CP to Qn or $\bar{Q}n$ ; see Fig. 5	5 V	53 ns + (0.55 ns/pF) C <sub>L</sub>	-	80	160	ns
			10 V	24 ns + (0.23 ns/pF) C <sub>L</sub>	-	35	70	ns
			15 V	17 ns + (0.16 ns/pF) C <sub>L</sub>	-	25	50	ns
		$\bar{M}R$ to Qn; see Fig. 5	5 V	48 ns + (0.55 ns/pF) C <sub>L</sub>	-	75	155	ns
			10 V	19 ns + (0.23 ns/pF) C <sub>L</sub>	-	30	65	ns
			15 V	17 ns + (0.16 ns/pF) C <sub>L</sub>	-	25	50	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	CP to Qn or $\bar{Q}n$ ; see Fig. 5	5 V	43 ns + (0.55 ns/pF) C <sub>L</sub>	-	70	140	ns
			10 V	19 ns + (0.23 ns/pF) C <sub>L</sub>	-	30	65	ns
			15 V	17 ns + (0.16 ns/pF) C <sub>L</sub>	-	25	45	ns
		$\bar{M}R$ to $\bar{Q}n$ ; see Fig. 5	5 V	43 ns + (0.55 ns/pF) C <sub>L</sub>	-	70	140	ns
			10 V	19 ns + (0.23 ns/pF) C <sub>L</sub>	-	30	65	ns
			15 V	17 ns + (0.16 ns/pF) C <sub>L</sub>	-	25	50	ns
t <sub>t</sub>	transition time	see Fig. 5	5 V	10 ns + (1.00 ns/pF) C <sub>L</sub>	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF) C <sub>L</sub>	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF) C <sub>L</sub>	-	20	40	ns
t <sub>su</sub>	set-up time	Dn to CP; see Fig. 5	5 V		60	30	-	ns
			10 V		20	10	-	ns
			15 V		15	5	-	ns
t <sub>h</sub>	hold time	Dn to CP; see Fig. 5	5 V		+25	-5	-	ns
			10 V		10	0	-	ns
			15 V		10	0	-	ns
t <sub>w</sub>	pulse width	CP input LOW; minimum pulse width; see Fig. 5	5 V		90	45	-	ns
			10 V		35	15	-	ns
			15 V		25	10	-	ns
		$\bar{M}R$ input LOW; minimum pulse width; see Fig. 5	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t <sub>rec</sub>	recovery time	$\bar{M}R$ input; see Fig. 5	5 V		0	-30	-	ns
			10 V		0	-20	-	ns
			15 V		0	-15	-	ns
f <sub>max</sub>	maximum frequency		5 V		5	11	-	MHz
			10 V		15	30	-	MHz
			15 V		20	45	-	MHz

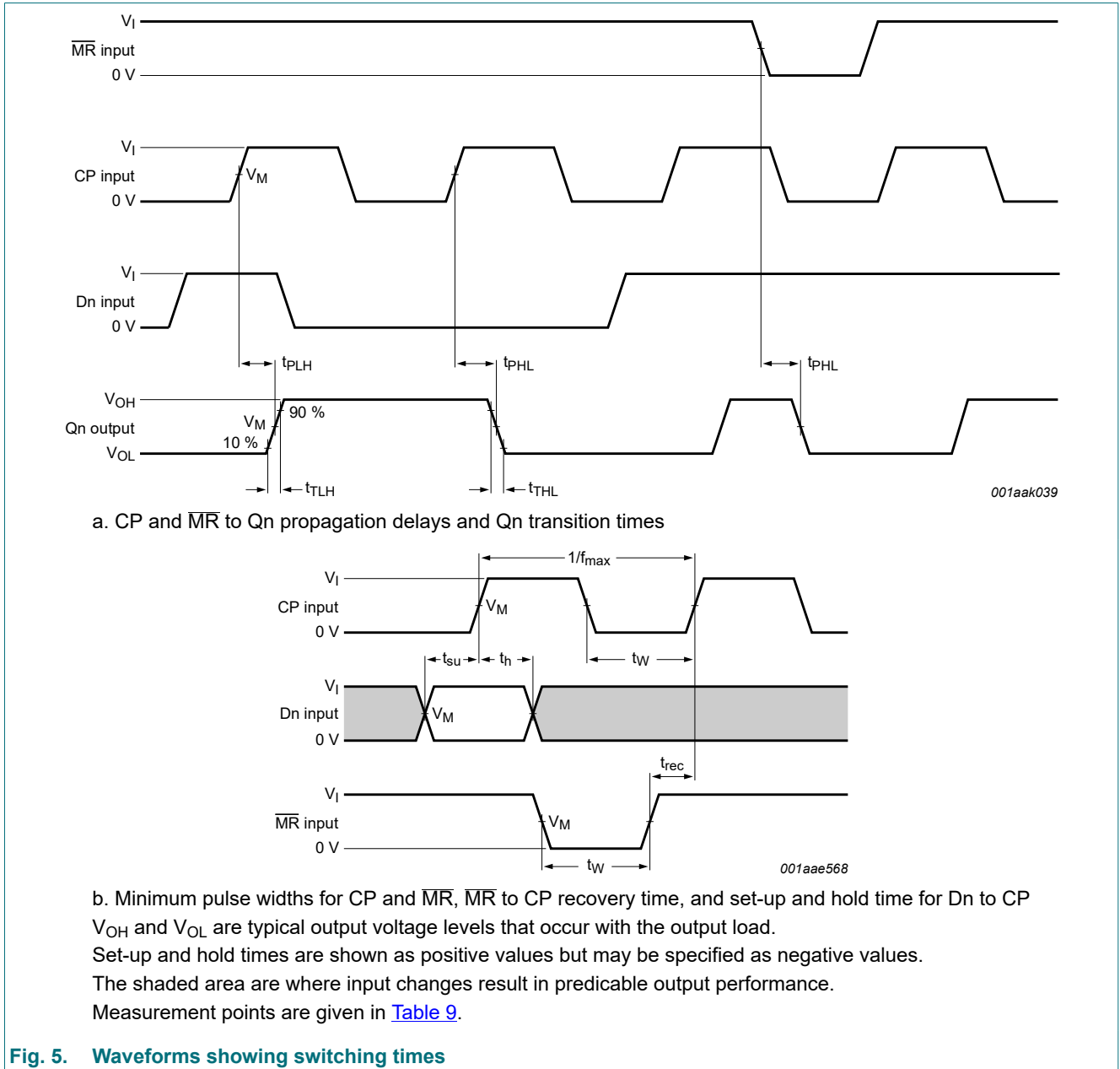
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formula shown (C<sub>L</sub> in pF).

**Table 8. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 2000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 8400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 22500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

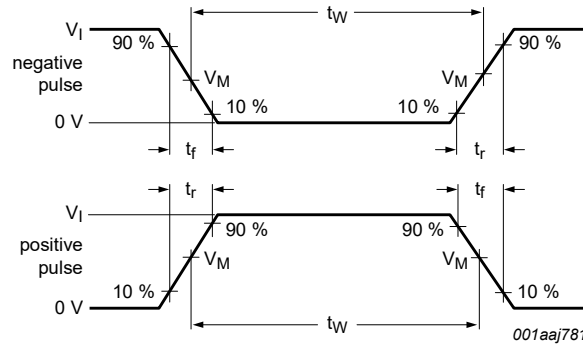
**11.1. Waveforms and test circuit**



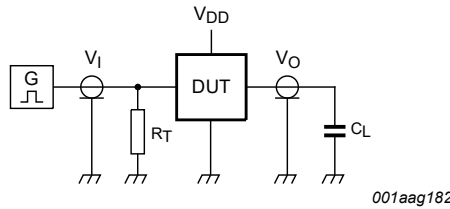
**Fig. 5. Waveforms showing switching times**

Table 9. Measurement points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



a. Input waveforms



b. Test circuit

Test and measurement data is given in [Table 10](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$C_L$  = Load capacitance including jig and probe capacitance.

Fig. 6. Test circuit for measuring switching times

Table 10. Measurement points and test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	50 pF



## 12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

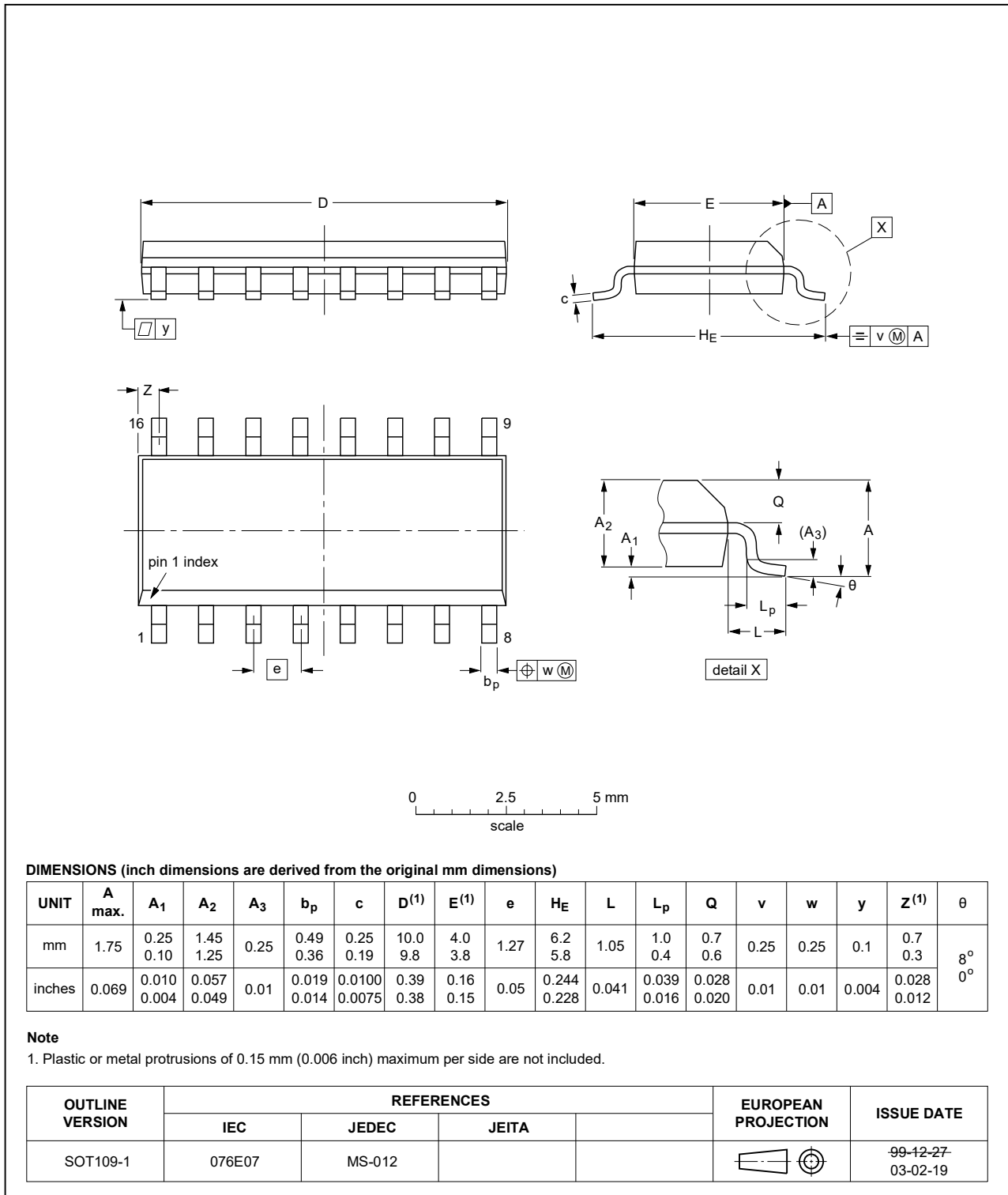


Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

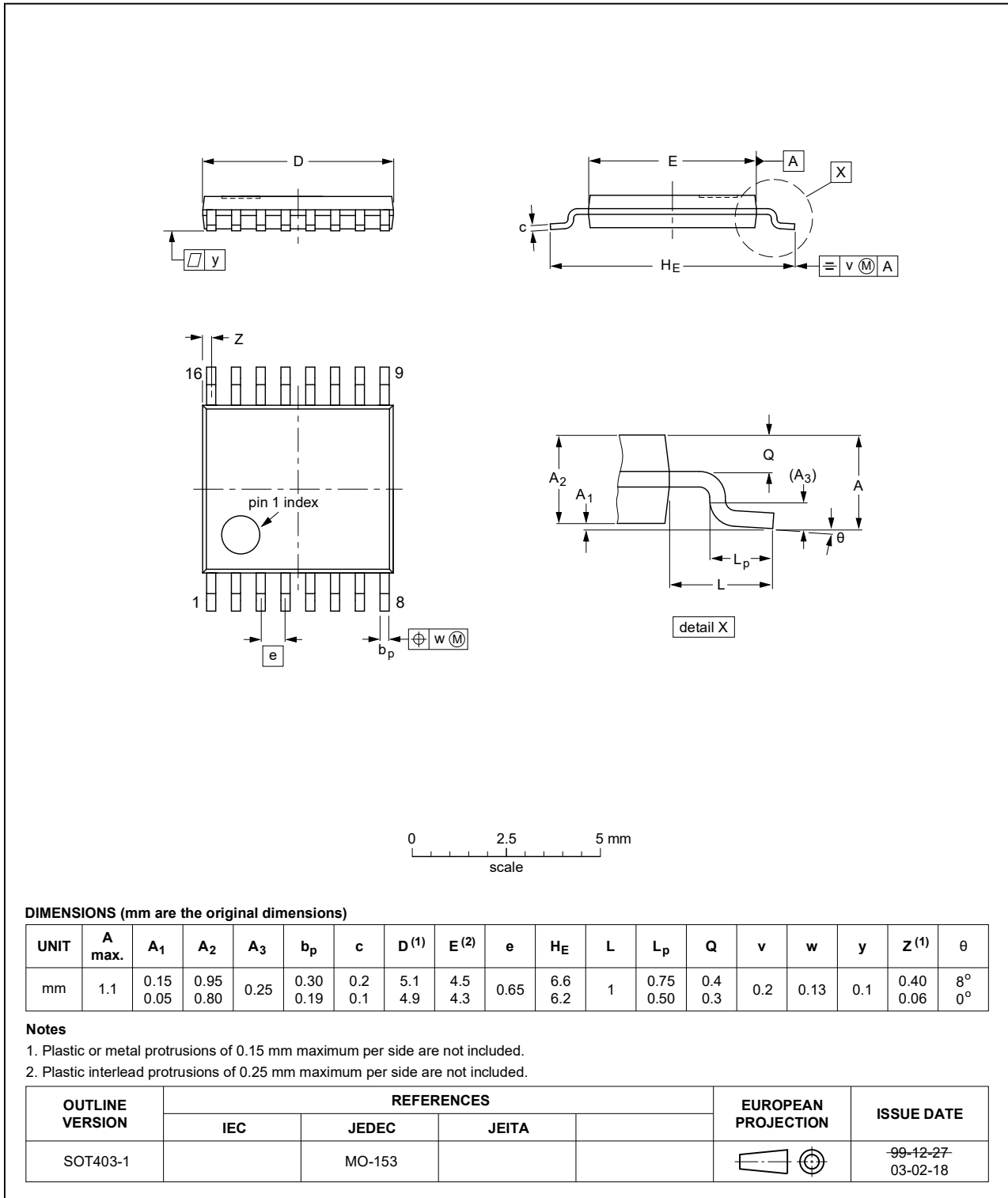


Fig. 8. Package outline SOT403-1 (TSSOP16)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40175B v.10	20211129	Product data sheet	-	HEF40175B v.9
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
HEF40175B v.9	20160321	Product data sheet	-	HEF40175B v.8
Modifications:	<ul style="list-style-type: none"> <li>Type number HEF40175BP (SOT38-4) removed.</li> </ul>			
HEF40175B v.8	20111121	Product data sheet	-	HEF40175B v.7
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> <li>Changes in "General description", "Features and benefits" and "Applications".</li> </ul>			
HEF40175B v.7	20110503	Product data sheet	-	HEF40175B v.6
HEF40175B v.6	20101214	Product data sheet	-	HEF40175B v.5
HEF40175B v.5	20100105	Product data sheet	-	HEF40175B v.4
HEF40175B v.4	20090813	Product data sheet	-	HEF40175B_CNV v.3
HEF40175B_CNV v.3	19950101	Product specification	-	HEF40175B_CNV v.2
HEF40175B_CNV v.2	19950101	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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