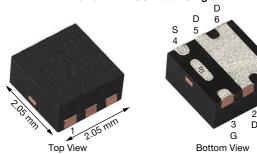
www.vishay.com

Vishay Siliconix

# N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY									
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ ) MAX.	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (TYP.)						
20	0.0095 at V <sub>GS</sub> = 10 V	25							
	0.0111 at V <sub>GS</sub> = 6 V	25	6.3 nC						
	0.0130 at V <sub>GS</sub> = 4.5 V	25							

#### PowerPAK® SC-70-6L Single



Marking Code: AW Ordering Information:

SiA466EDJ-T1-GE3 (lead (Pb)-free and halogen-free)

#### **FEATURES**

TrenchFET® power MOSFET



• Thermally enhanced PowerPAK® SC-70 package

- Small footprint area

- Low on-resistance

COMPLIANT HALOGEN FREE

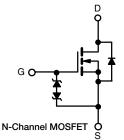
• Typical ESD protection: 2500 V (HBM)

• 100 % R<sub>q</sub> Tested

 Material categorization: For definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>

#### **APPLICATIONS**

- For smart phones and mobile computing
  - DC/DC converters
  - Power management
  - Load switches



PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V <sub>DS</sub>	20	V		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V		
	T <sub>C</sub> = 25 °C		25 <sup>a</sup>			
Onetic Dunin O	T <sub>C</sub> = 70 °C		25 a			
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	15.1 <sup>b, c</sup>			
	T <sub>A</sub> = 70 °C		12.1 <sup>b, c</sup>	А		
Pulsed Drain Current (t = 300 μs)	•	I <sub>DM</sub>	I <sub>DM</sub> 50			
Osalis a a Osasa Bais Bisda Osasa	T <sub>C</sub> = 25 °C		16			
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	l <sub>s</sub> —	2.9 b, c			
	T <sub>C</sub> = 25 °C		19.2			
Marrian and Danier District	T <sub>C</sub> = 70 °C		12.3	14/		
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.5 b, c	W		
	T <sub>A</sub> = 70 °C		2.2 b, c			
Operating Junction and Storage Temperature Ra	ange	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C		
Soldering Recommendations (Peak Temperature	e) <sup>d, e</sup>	-	260	-0		

THERMAL RESISTANCE RATINGS									
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT					
Maximum Junction-to-Ambient b, f	t ≤ 5 s	R <sub>thJA</sub>	28	36	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	5.3	6.5	] 0/1				

#### Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s
- d. See solder profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 80 °C/W.



# Vishay Siliconix

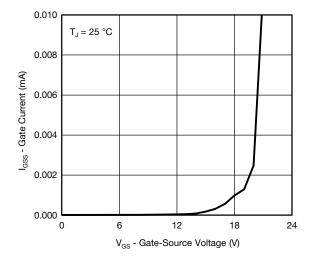
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	17	-	mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-4.7	-	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	-	2.5	V
Onto Course Londone		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 30	μΑ
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$	-	-	± 1	
Zana Oata Waltana Busin Commant		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	-	-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	20	-	-	Α
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9 A	-	0.0079	0.0095	
Drain-Source On-State Resistance a	R <sub>DS(on)</sub>	$V_{GS} = 6 \text{ V}, I_D = 5 \text{ A}$	-	0.0095	0.0111	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	0.0104	0.0130	
Forward Transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A	-	38	-	S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>		-	620	-	pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 1 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	230	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	135	-	
Total Cata Charge		V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	-	13	20	nC
Total Gate Charge	Q <sub>g</sub> Q <sub>gs</sub>		-	6.3	10	
Gate-Source Charge		$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 15 \text{ A}$	-	1.6	-	
Gate-Drain Charge	$Q_{gd}$		-	2.1	-	
Gate Resistance	$R_g$	f = 1 MHz	0.2	0.9	1.8	Ω
Turn-On Delay Time	t <sub>d(on)</sub>		-	5	10	ns
Rise Time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_L = 1 \Omega$	-	22	33	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	12	20	
Fall Time	t <sub>f</sub>		-	6	12	
Turn-On Delay Time	t <sub>d(on)</sub>		-	15	23	
Rise Time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_L = 1 \Omega$	-	73	110	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	12	20	
Fall Time	t <sub>f</sub>		-	20	30	
<b>Drain-Source Body Diode Characterist</b>	ics					
Continuous Source-Drain Diode Current	Is	T <sub>C</sub> = 25 °C	-	-	16	۸
Pulse Diode Forward Current	I <sub>SM</sub>		-	-	50	Α
Body Diode Voltage			-	0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	-	22	33	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	10 A dl/dt 100 A / T 05 00	-	10	15	nC
Reverse Recovery Fall Time	ta	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	11	-	ns
Reverse Recovery Rise Time	t <sub>b</sub>		-	11	-	

#### Notes

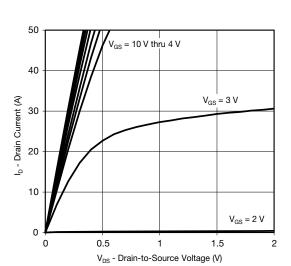
- a. Pulse test; pulse width  $\leq 300~\mu s,\,duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Package limited

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

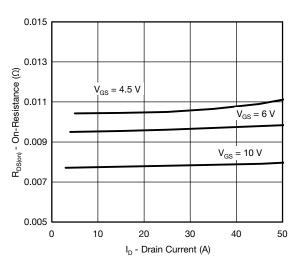




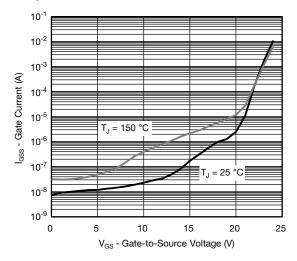
Gate Source Voltage vs. Gate Current



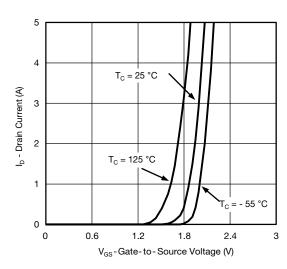
**Output Characteristics** 



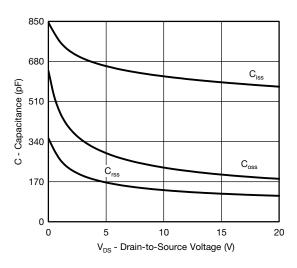
On-Resistance vs. Drain Current and Gate Voltage



Gate Source Voltage vs. Gate Current

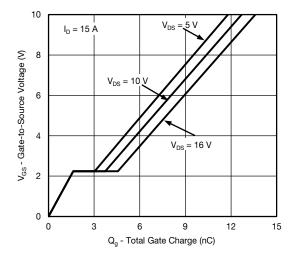


**Transfer Characteristics** 

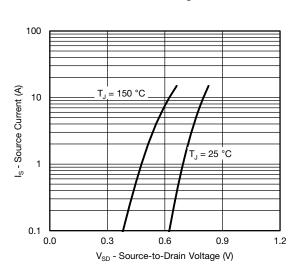


Capacitance

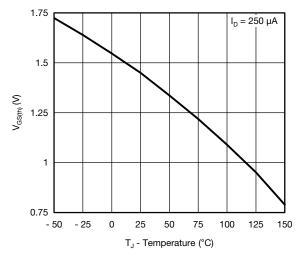




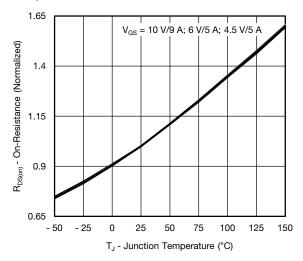
**Gate Charge** 



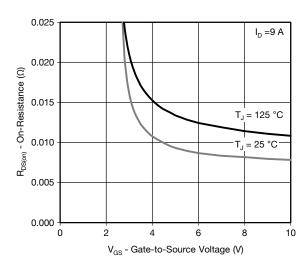
Source-Drain Diode Forward Voltage



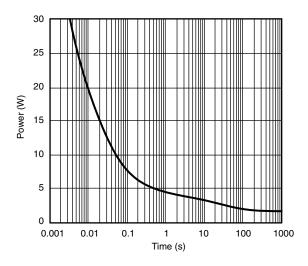
**Threshold Voltage** 



On-Resistance vs. Junction Temperature

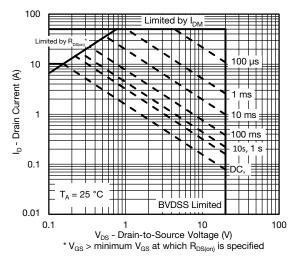


On-Resistance vs. Gate-to-Source Voltage

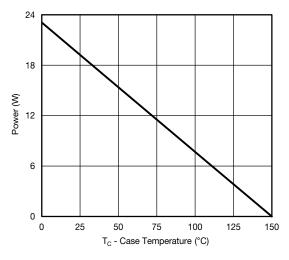


Single Pulse Power, Junction-to-Ambient

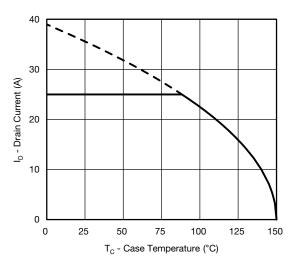




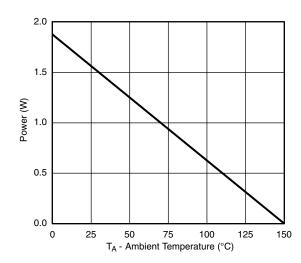
#### Safe Operating Area, Junction-to-Ambient



Power, Junction-to-Case



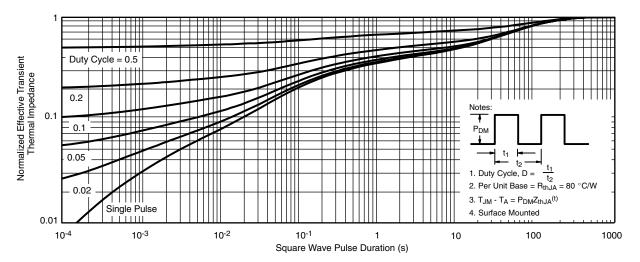
#### **Current Derating\***



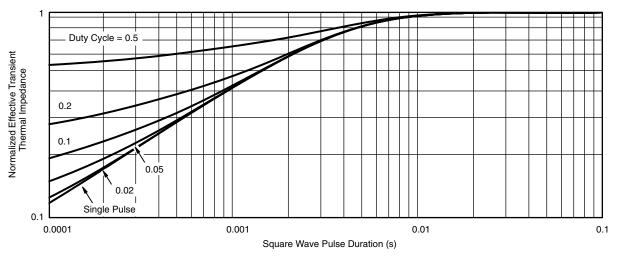
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J (max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?62955">www.vishay.com/ppg?62955</a>.





Vishay Siliconix

# PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
  Package outline exclusive of mold flash and metal burr
  Package outline inclusive of plating

	SINGLE PAD						DUAL PAD					
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC		
K		0.275 TYP			0.011 TYP		0.275 TYP		0.011 TYP			
K1		0.400 TYP		0.016 TYP		0.320 TYP			0.013 TYP			
K2		0.240 TYP		0.009 TYP		0.252 TYP			0.010 TYP			
К3		0.225 TYP		0.009 TYP					•	•		
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



# RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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Vishay

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