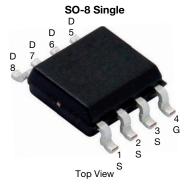


Vishay Siliconix

# N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) MAX.	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (TYP.)			
30	0.0140 at V <sub>GS</sub> = 10 V	14	7.3 nC			
30	0.0175 at V <sub>GS</sub> = 4.5 V	12.5	7.5110			



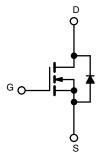
#### **FEATURES**

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



#### **APPLICATIONS**

- DC/DC conversion
  - Notebook system power



N-Channel MOSFET

### **Ordering Information:**

Si4134DY-T1-E3 (lead (Pb)-free) Si4134DY-T1-GE3 (lead (Pb)-free and halogen-free)

PARAMETER	SYMBOL V <sub>DS</sub>	LIMIT	UNIT	
Drain-Source Voltage Gate-Source Voltage		30 ± 20	V	
				V <sub>GS</sub>
	T <sub>C</sub> = 25 °C		14	
Ossilia as a Davis Ossia (F. 150.00)	T <sub>C</sub> = 70 °C	1 .	11.2	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	9.9 b, c	
	T <sub>A</sub> = 70 °C		7.9 <sup>b, c</sup>	
Pulsed Drain Current (t = 300 μs)		I <sub>DM</sub>	50	A
Osadia as a Osaga a Basis Bisada Osaga	T <sub>C</sub> = 25 °C		4.1	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2 <sup>b, c</sup>	
Single Pulse Avalanche Current		I <sub>AS</sub>	15	
Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	11.25	mJ
	T <sub>C</sub> = 25 °C		5	
Martin or Brown Black of the	T <sub>C</sub> = 70 °C		3.2	144
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>b, c</sup>	W
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>sta</sub>	-55 to +150	°C

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT			
Maximum Junction-to-Ambient b, d	t ≤ 10 s	R <sub>thJA</sub>	38	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	20	25	C/VV		

#### Notes

- a. Based on  $T_C = 25$  °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under steady state conditions is 85 °C/W.



# Vishay Siliconix

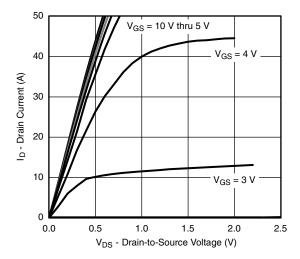
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	-	-	V	
V <sub>DS</sub> Temperature Coefficient	AVpe/Tu		-	33	-	mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu\text{A}$		-5	-		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \ \mu A$	1.2	1.8	2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zana Onto Welliam Busin On and		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	_	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	μA	
On-State Drain Current a	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20	-	-	Α	
D : 0	, ,	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	0.0115 0.0140		-	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 7 \text{ A}$	-	0.0145	0.0175	Ω	
Forward Transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A	-	24	-	S	
Dynamic <sup>b</sup>		-		L			
Input Capacitance	C <sub>iss</sub>		-	846	-	pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	187	-		
Reverse Transfer Capacitance	C <sub>rss</sub>		-	72	-		
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	15.4	23	nC	
Total Gate Charge			-	7.3	11		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$	-	2.3	-		
Gate-Drain Charge	Q <sub>ad</sub>		-	2.2	-		
Gate Resistance	$R_g$	f = 1 MHz	0.2	0.8	1.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>		-	15	30		
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V, R}_{I} = 1.5 \Omega$	-	12	24		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	13	26		
Fall Time	t <sub>f</sub>	1	-	10	20		
Turn-On Delay Time	t <sub>d(on)</sub>		-	9	18	ns -	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V, R}_{I} = 1.5 \Omega$	-	9	18		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	14	28		
Fall Time	t <sub>f</sub>	1	-	8	16		
<b>Drain-Source Body Diode Characterist</b>	ics			L			
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	4.2		
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	-	-	-	50	Α	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 3 A	-	0.78	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	_	-	17	34	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 <u>.</u>	-	9.5	19	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$	-	10	-	ns	

#### Notes

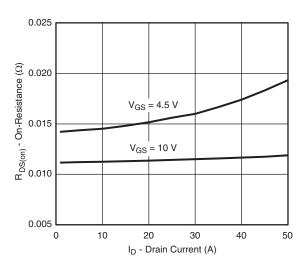
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

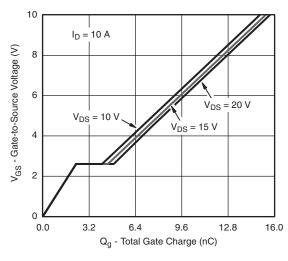




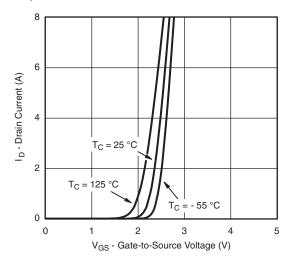
#### **Output Characteristics**



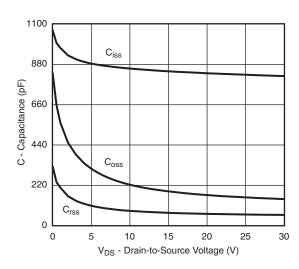
On-Resistance vs. Drain Current and Gate Voltage



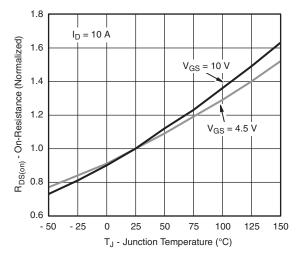
**Gate Charge** 



**Transfer Characteristics** 

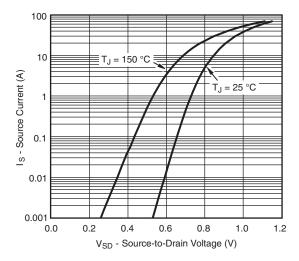


Capacitance

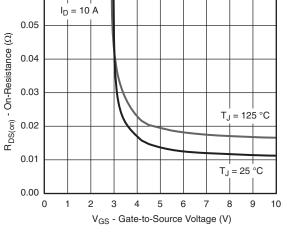


On-Resistance vs. Junction Temperature



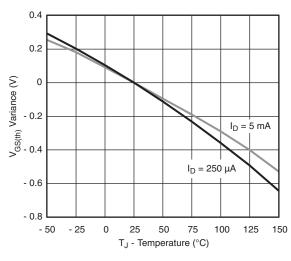


#### Source-Drain Diode Forward Voltage

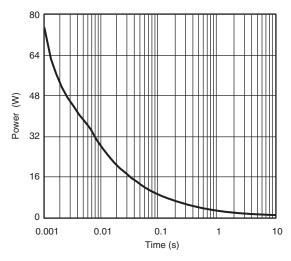


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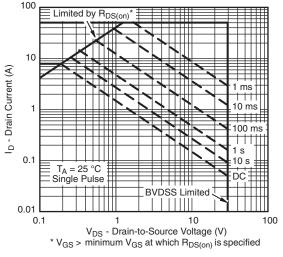
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 

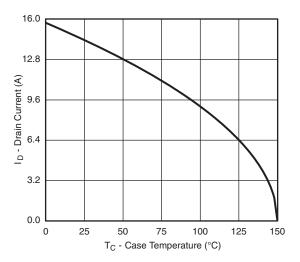


Single Pulse Power, Junction-to-Ambient

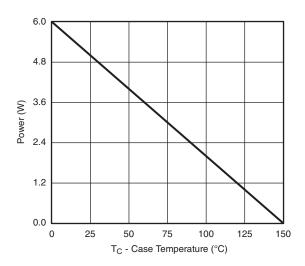


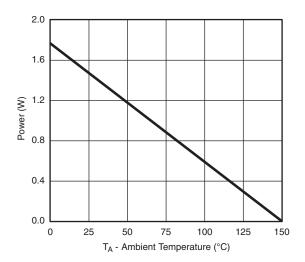
Safe Operating Area, Junction-to-Ambient





#### Current Derating a





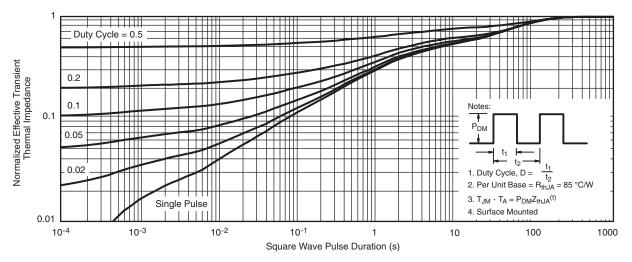
Power, Junction-to-Foot

Power Derating, Junction-to-Ambient

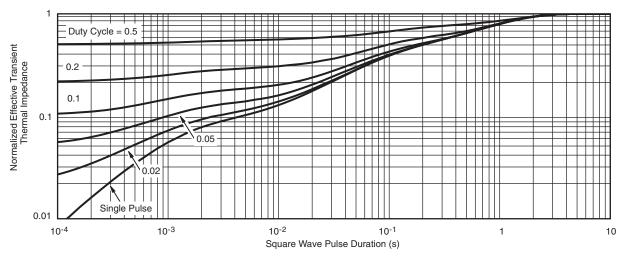
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg268999">www.vishay.com/ppg268999</a>.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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