

# NTB6410AN, NTP6410AN, NVB6410AN

## MOSFET – Power, N-Channel

100 V, 76 A, 13 mΩ



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- NVB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DS}$	100	V
Gate-to-Source Voltage – Continuous			$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	76	A
		$T_C = 100^\circ\text{C}$		54	
Power Dissipation $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	$P_D$	188	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		$I_{DM}$	305	A
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)			$I_S$	76	A
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 50 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_{L(pk)} = 57.7 \text{ A}$ , $L = 0.3 \text{ mH}$ , $R_G = 25 \Omega$ )			$E_{AS}$	500	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds			$T_L$	260	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

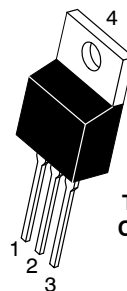
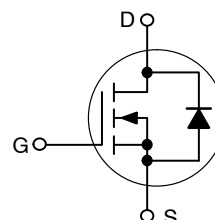
Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	0.8	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	32	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

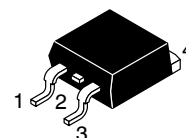
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$ (Note 1)
100 V	13 mΩ @ 10 V	76 A

### N-Channel

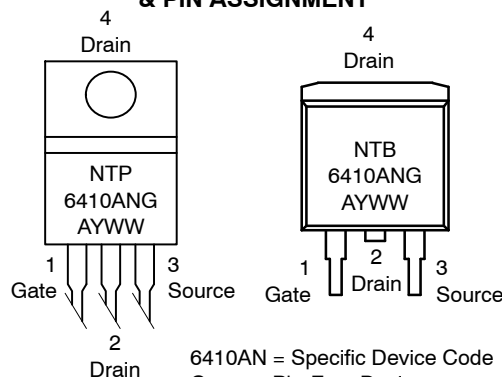


TO-220AB  
CASE 221A  
STYLE 5



D<sup>2</sup>PAK  
CASE 418B  
STYLE 2

### MARKING DIAGRAM & PIN ASSIGNMENT



6410AN = Specific Device Code  
G = Pb-Free Device  
A = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTB6410AN, NTP6410AN, NVB6410AN

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			94		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 150°C		100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

## ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0		4.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(th)</sub> /T <sub>J</sub>			9.0		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 76 A		11	13	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		10	12	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 20 A		40		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4500		pF
Output Capacitance	C <sub>oss</sub>			650		
Reverse Transfer Capacitance	C <sub>rss</sub>			250		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 80 V, I <sub>D</sub> = 76 A		120		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			5.2		
Gate-to-Source Charge	Q <sub>GS</sub>			20		
Gate-to-Drain Charge	Q <sub>GD</sub>			57		
Plateau Voltage	V <sub>GP</sub>			5.1		
Gate Resistance	R <sub>G</sub>			2.4		Ω

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 10 V (Note 3)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 80 V, I <sub>D</sub> = 76 A, R <sub>G</sub> = 6.2 Ω		17		ns
Rise Time	t <sub>r</sub>			170		
Turn-Off Delay Time	t <sub>d(off)</sub>			120		
Fall Time	t <sub>f</sub>			190		

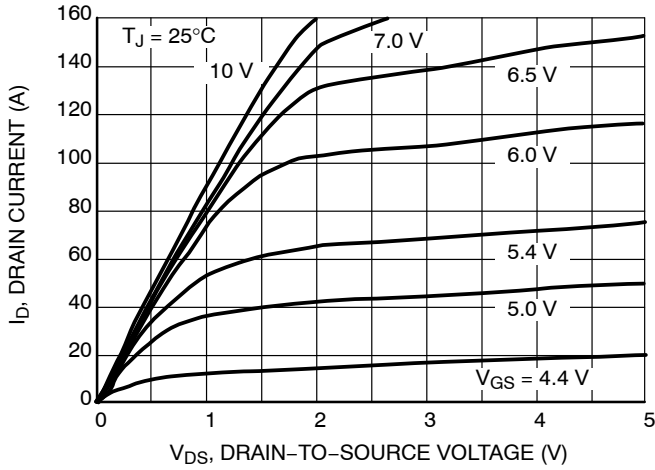
## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 76 A	T <sub>J</sub> = 25°C		1.0	1.3	V
			T <sub>J</sub> = 125°C		0.9		
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 76 A, di <sub>SD</sub> /dt = 100 A/μs		93		ns	
Charge Time	t <sub>a</sub>			69			
Discharge Time	t <sub>b</sub>			24			
Reverse Recovery Charge	Q <sub>RR</sub>			300			nC

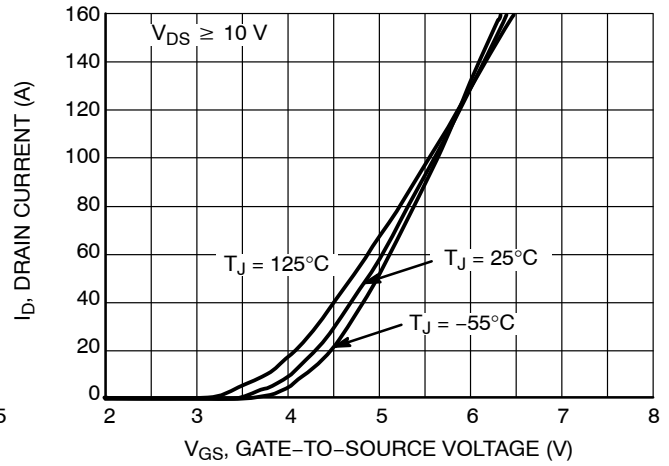
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

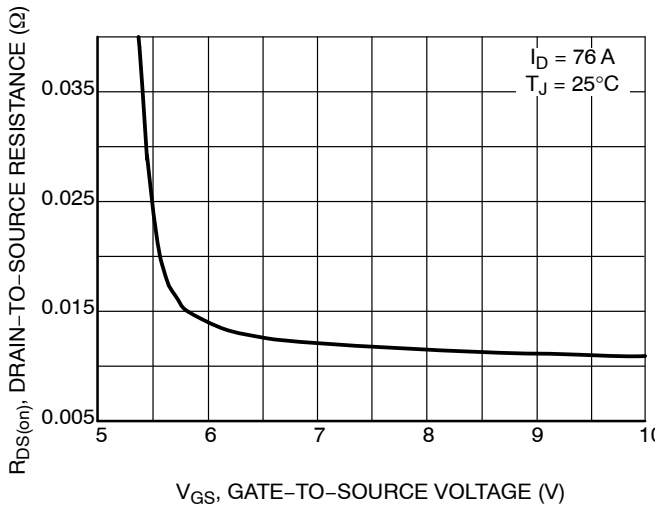
# NTB6410AN, NTP6410AN, NVB6410AN



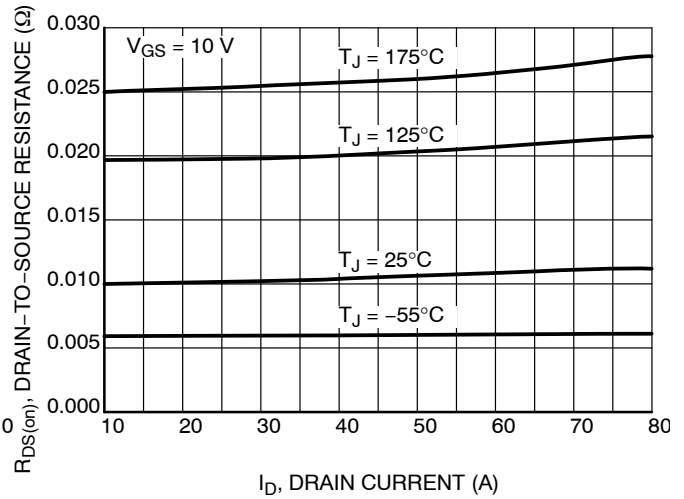
**Figure 1. On-Region Characteristics**



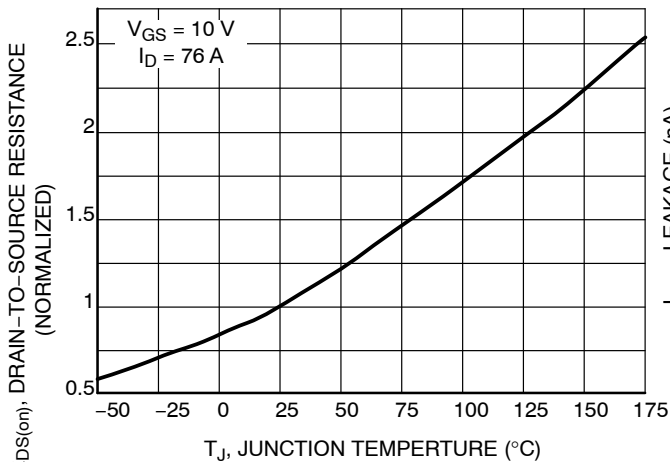
**Figure 2. Transfer Characteristics**



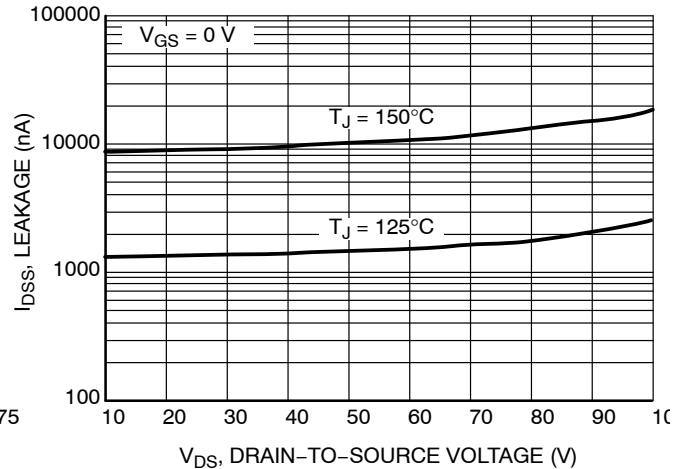
**Figure 3. On-Region versus Gate Voltage**



**Figure 4. On-Region versus Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current versus Voltage**

# NTB6410AN, NTP6410AN, NVB6410AN

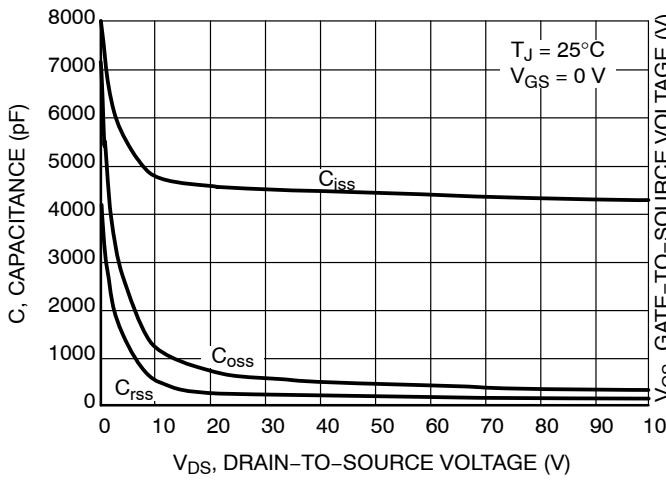


Figure 7. Capacitance Variation

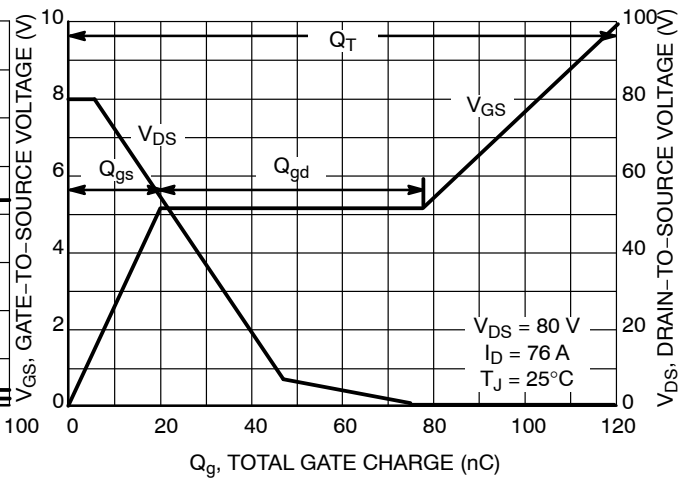


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

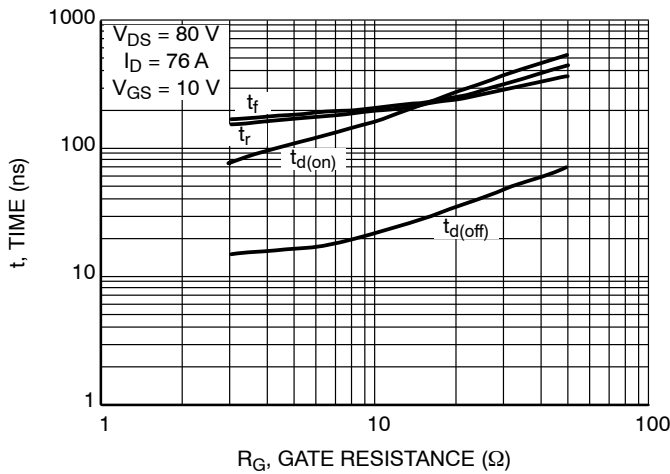


Figure 9. Resistive Switching Time Variation versus Gate Resistance

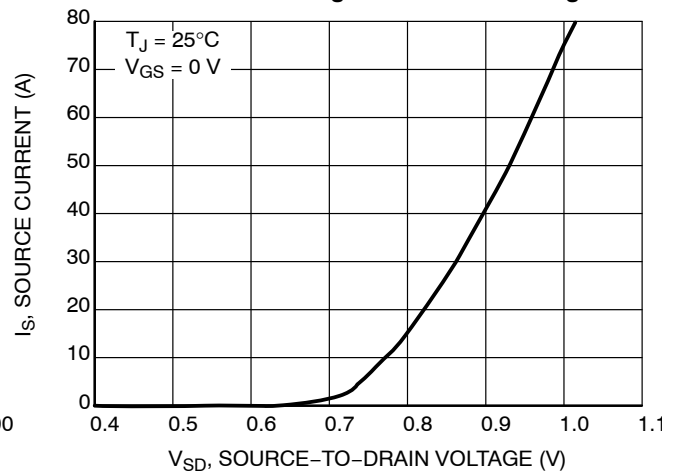


Figure 10. Diode Forward Voltage versus Current

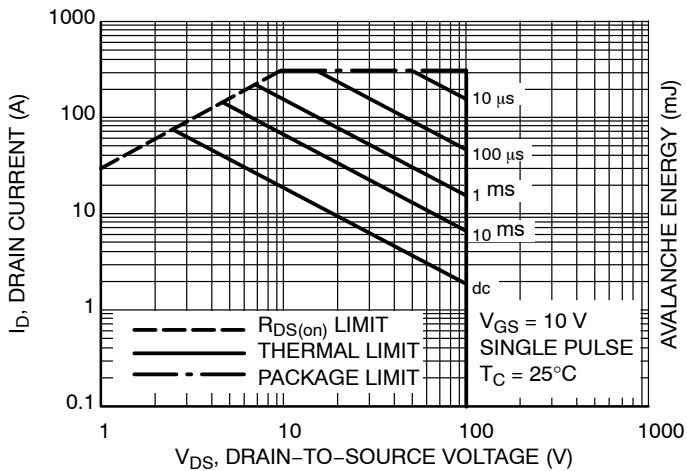


Figure 11. Maximum Rated Forward Biased Safe Operating Area

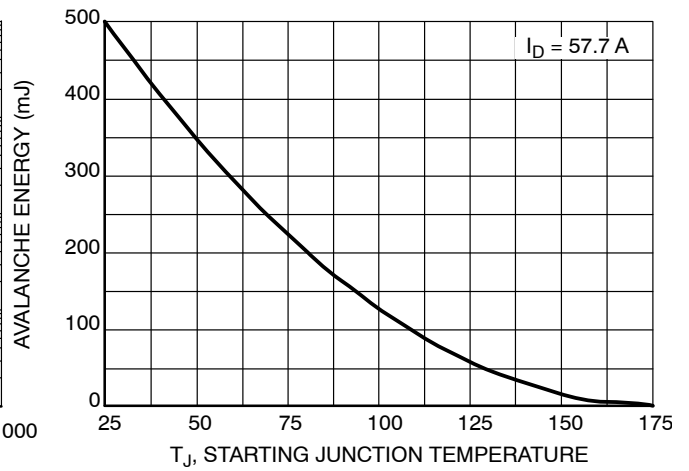


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

# NTB6410AN, NTP6410AN, NVB6410AN

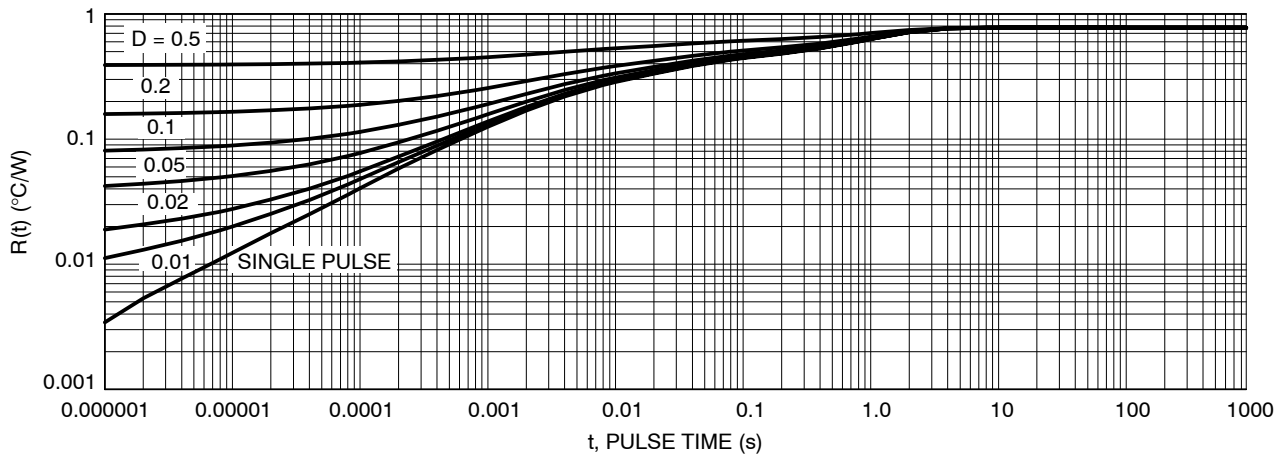


Figure 13. Thermal Response

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTB6410ANG	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
NTB6410ANT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NTP6410ANG	TO-220 (Pb-Free)	50 Units / Rail
NVB6410ANT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1



TO-220  
CASE 221A  
ISSUE AK

DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

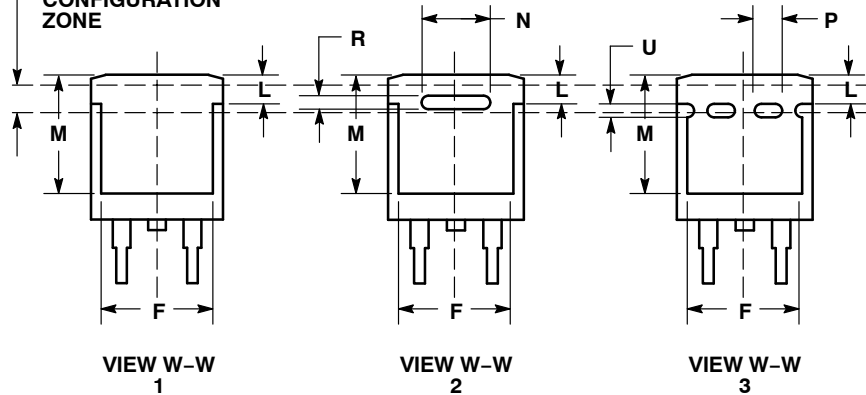


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

**VARIABLE CONFIGURATION ZONE**



- |  |   |   |  |   |  |
|--|---|---|--|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE | <b>STYLE 6:</b><br>PIN 1. NO CONNECT<br>2. CATHODE<br>3. ANODE<br>4. CATHODE |
|--|---|---|--|---|--|

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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

**GENERIC  
MARKING DIAGRAM\***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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