

MOSFET – Single N-Channel

150 V, 4.4 mΩ, 187 A

NTBLS4D0N15MC

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			150	V
V_{GS}	Gate-to-Source Voltage			± 20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^\circ\text{C}$	187	A
P_D				Power Dissipation $R_{\theta JC}$ (Note 2)	316
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	19	A
P_D				Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	3.4
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	2255	A	
T_J, T_{stg}	Operating Junction and Storage Temperature Range			-55 to 175	$^\circ\text{C}$
I_S	Source Current (Body Diode)			263	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_L = 81.5 \text{ A}_{pk}, L = 0.1 \text{ mH}$)			332	mJ
T_L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

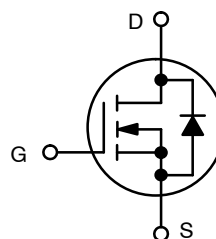
1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



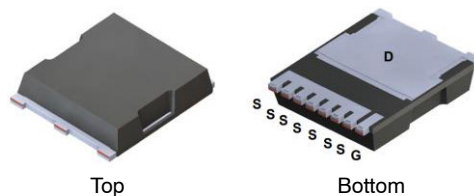
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	4.4 mΩ @ 10 V	187 A
	4.9 mΩ @ 8 V	



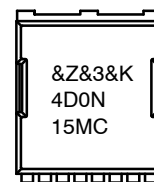
N-CHANNEL MOSFET



Top Bottom

H-PSOF8L 11.68x9.80
MO-299A
CASE 100CU

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
4D0N15MC = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTBLS4D0N15MC	MO-299A (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 2)	0.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	43	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150	–	–	V	
$V_{(BR)DSS} / T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, ref to 25°C	–	30.23	–	mV/°C	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$	$T_J = 25^\circ\text{C}$	–	–	1	μA
			$T_J = 125^\circ\text{C}$	–	–	10	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	–	–	± 100	nA	

ON CHARACTERISTICS

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 584\ \mu\text{A}$	2.5	3.7	4.5	V
$V_{GS(TH)} / T_J$	Negative Threshold Temperature Coefficient	$I_D = 250\ \mu\text{A}$, ref to 25°C	–	–10.12	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}$	–	3.1	4.4	m Ω
		$V_{GS} = 8\text{ V}, I_D = 53\text{ A}$	–	3.5	4.9	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 80\text{ A}$	–	174	–	S
R_G	Gate-Resistance	$T_A = 25^\circ\text{C}$	–	1.3	–	Ω

CHARGES & CAPACITANCES

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$	–	7490	–	pF
C_{OSS}	Output Capacitance		–	2055	–	
C_{RSS}	Reverse Transfer Capacitance		–	27.2	–	
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 80\text{ A}$	–	90.4	–	nC
$Q_{G(TH)}$	Threshold Gate Charge		–	24.7	–	
Q_{GS}	Gate-to-Source Charge		–	40.2	–	
Q_{GD}	Gate-to-Drain Charge		–	12.6	–	
V_{GP}	Plateau Voltage		–	5.7	–	
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$	–	251	–	nC

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 80\text{ A}, R_G = 6\ \Omega$	–	47	–	ns
t_r	Rise Time		–	115	–	
$t_{d(OFF)}$	Turn-Off Delay Time		–	58	–	
t_f	Fall Time		–	11	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 80\text{ A}$	$T_J = 25^\circ\text{C}$	–	0.86	1.2	V
			$T_J = 125^\circ\text{C}$	–	0.75	–	

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $di_S/dt = 100\text{ A}/\mu\text{s}$, $I_S = 80\text{ A}$	–	84	–	ns
t_a	Charge Time		–	55	–	
t_b	Discharge Time		–	29	–	
Q_{RR}	Reverse Recovery Charge		–	180	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

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TYPICAL CHARACTERISTICS

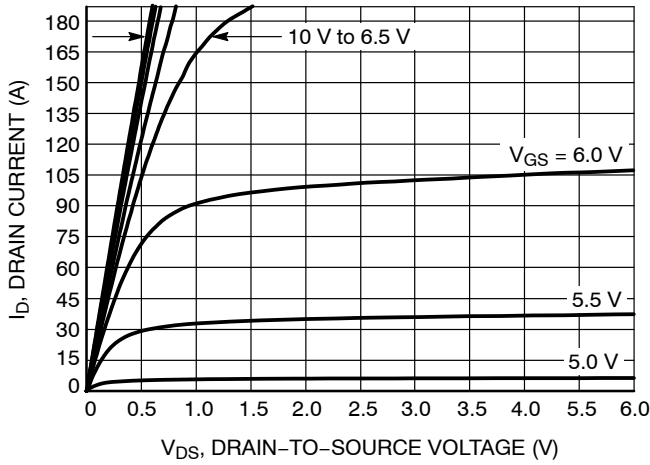


Figure 1. On-Region Characteristics

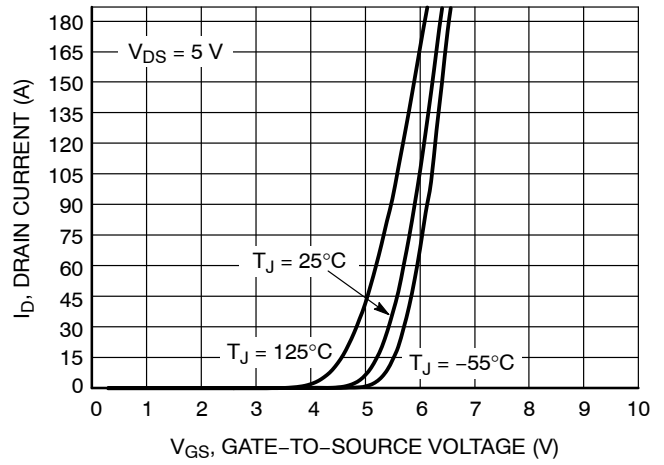


Figure 2. Transfer Characteristics

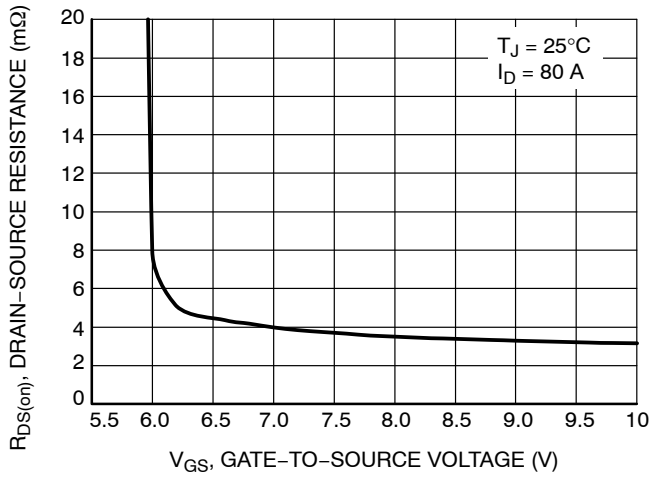


Figure 3. On-Resistance vs. V_{GS}

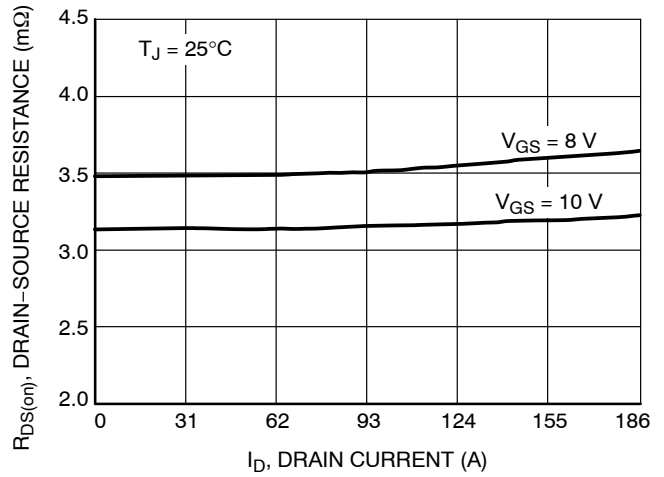


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

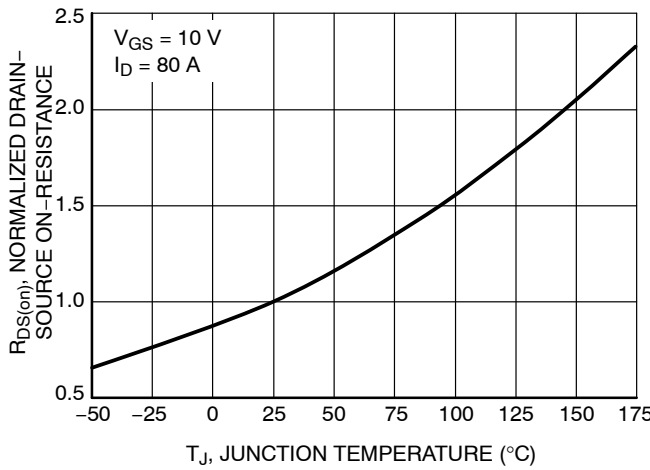


Figure 5. On-Resistance Variation with Temperature

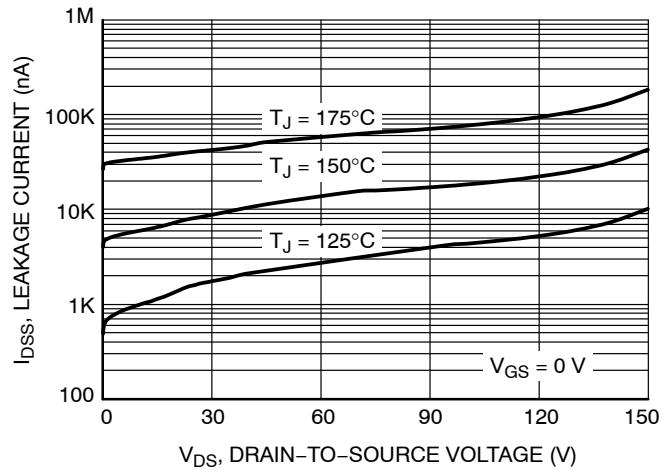


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

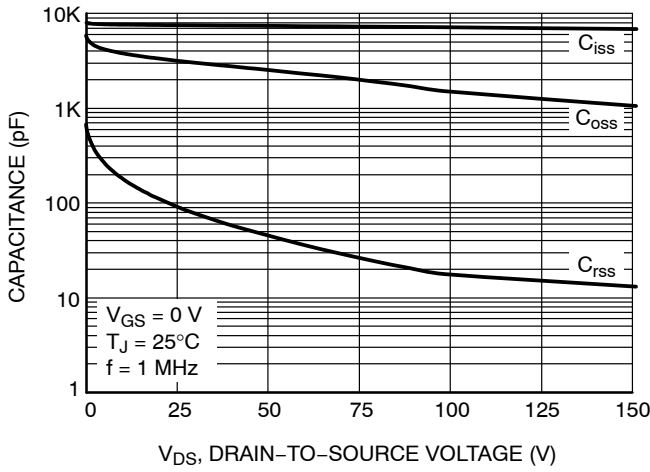


Figure 7. Capacitance Variation

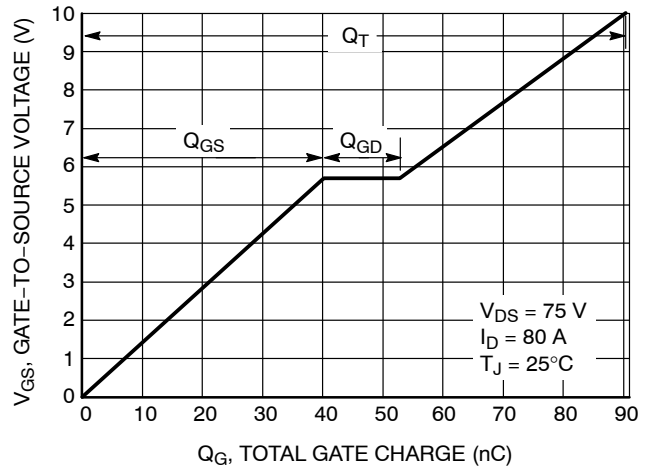


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

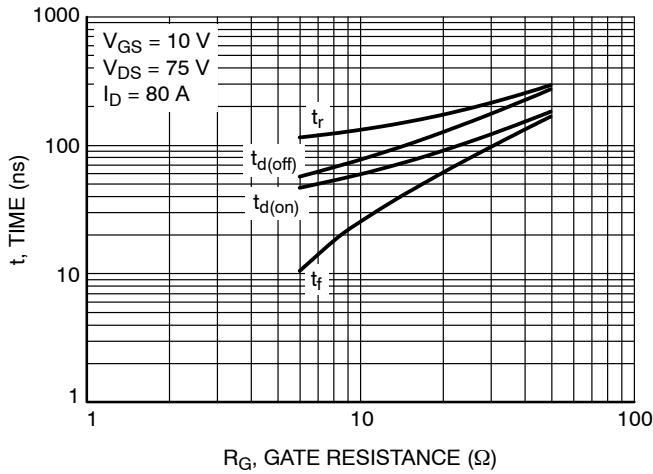


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

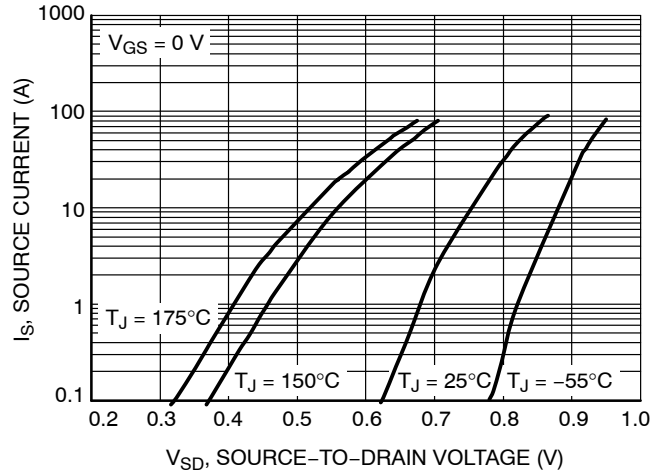


Figure 10. Diode Forward Voltage vs. Current

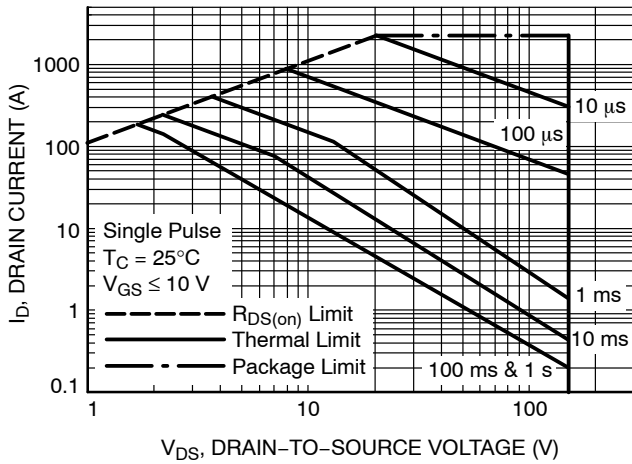


Figure 11. Maximum Rated Forward Biased Safe Operating Area

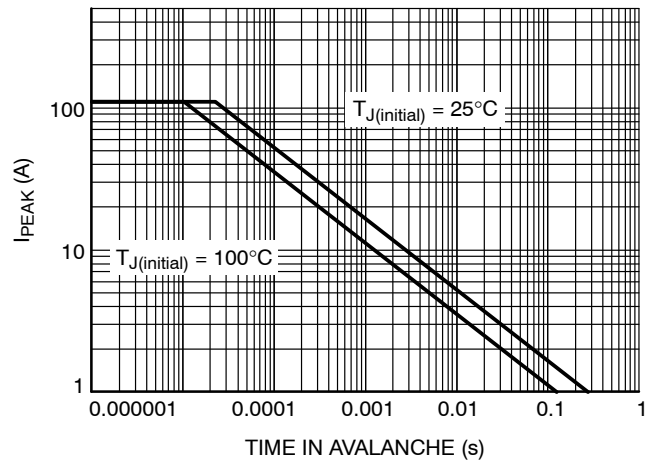


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

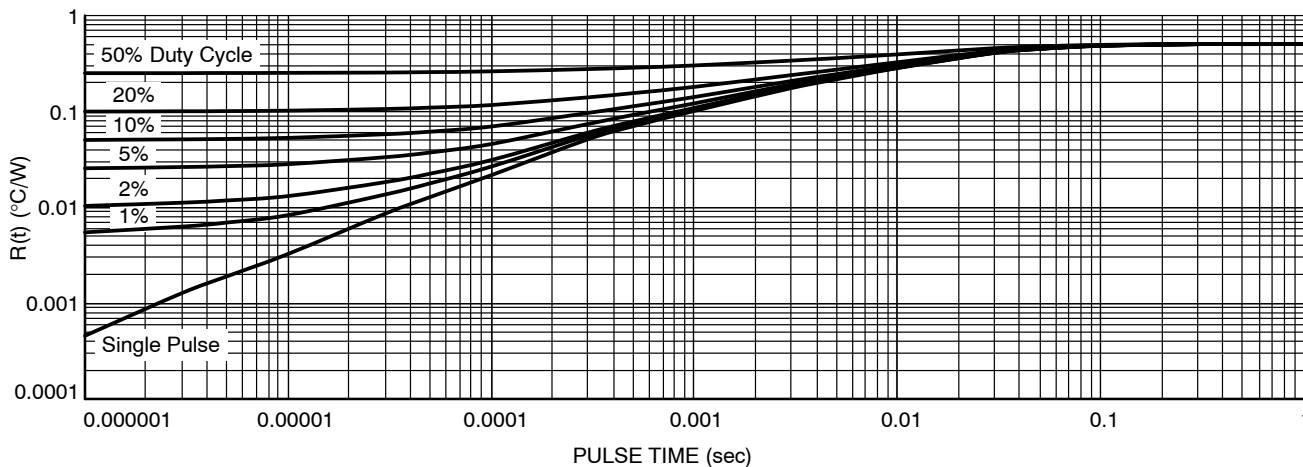


Figure 13. Thermal Characteristics (Junction-to-Ambient)

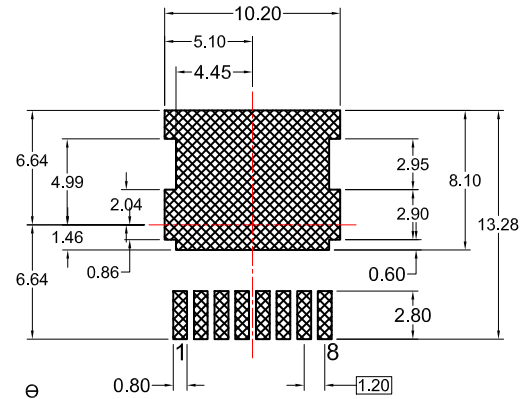
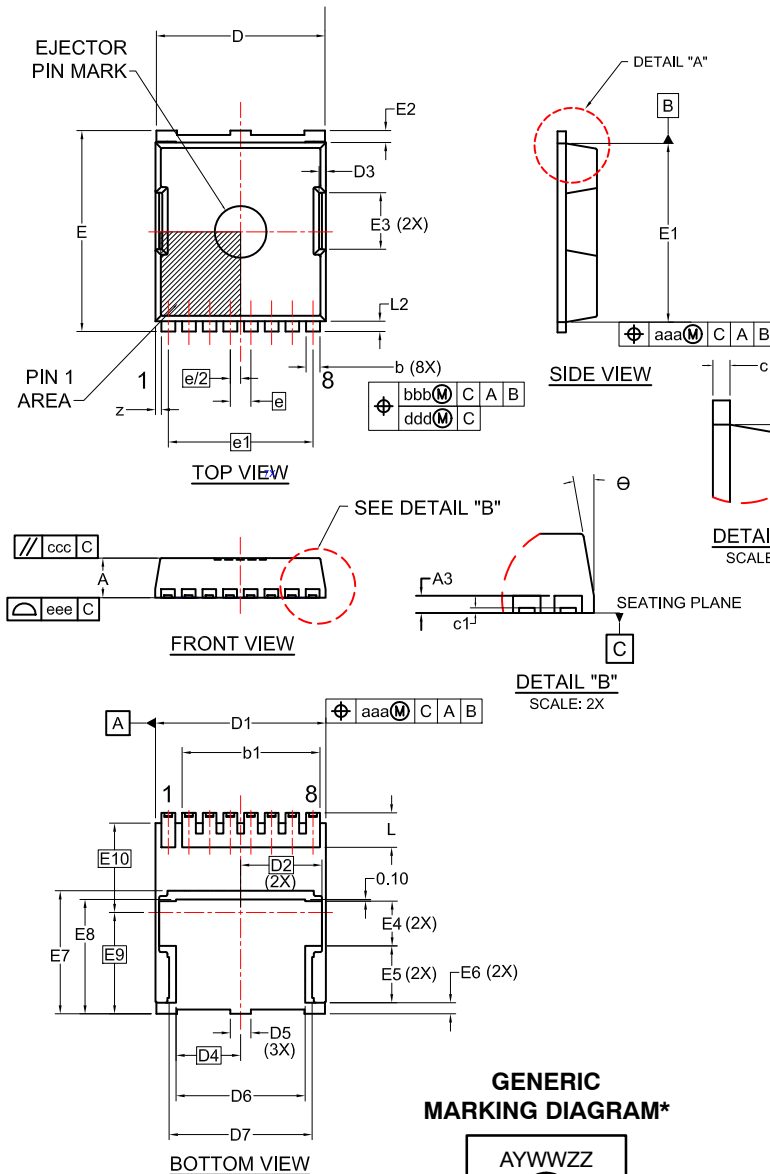
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



H-PSOF8L 11.68x9.80 CASE 100CU ISSUE A

DATE 06 JAN 2020



LAND PATTERN RECOMMENDATION

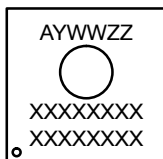
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

- NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 3. CONTROLLING DIMENSION: MILLIMETERS.
 4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
 5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A3	0.40	0.50	0.60
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	--	--
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	--	1.20	--
D6	7.40	7.50	7.60
D7	(8.30)		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	--	2.60	--

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	1.50	1.57	1.70
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	--	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		
E5	--	3.30	--
E6	--	0.65	--
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		

GENERIC MARKING DIAGRAM*



- A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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