[MOSFET](#) - P-Channel, PowerTrench®, Logic Level
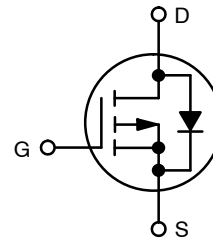## -40 V, -25 A, 21 mΩ

FDD9511L-F085

Features

- Typ $r_{DS(on)}$ = 17 mΩ at V_{GS} = −10 V; I_D = −25 A
- Typ $Q_{g(tot)}$ = 17 nC at V_{GS} = −10 V; I_D = −25 A
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

ON Semiconductor®

www.onsemi.com

DPAK
TO−252
CASE 369AS

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain to Source Voltage	V_{DSS}	−40	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current – Continuous (V_{GS} = −10 V) (T_C = 25°C) (Note 1)	I_D	−25	A
Pulsed Drain Current (T_C = 25°C)	I_D	See Figure 4	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	25	mJ
Power Dissipation	P_D	48.4	W
Derate above 25°C	P_D	0.32	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	−55 to +175	°C
Thermal Resistance (Junction to Case)	$R_{θJC}$	3.1	°C/W
Maximum Thermal Resistance (Junction to Ambient) (Note 3)	$R_{θJA}$	52	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by wirebond configuration
2. Starting Tj = 25°C, L = 0.08 mH, I_{AS} = −25 A, V_{DD} = −40 V during inductor charging and V_{DD} = 0 V during time in avalanche
3. $R_{θJA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{θJC}$ is guaranteed by design while $R_{θJA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDD9511L–F085	FDD9511L	D–PAK (TO–252)	13″	12 mm	2500 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA		–40	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = –40 V, V_{GS} = 0 V	T_J = 25°C	–	–	–1	μA
			T_J = 175°C (Note 4)	–	–	–1	mA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±16 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		–1	–1.8	–3	V
$R_{DS(on)}$	Drain to Source On–Resistance	V_{GS} = –4.5 V, I_D = –12.5 A, T_J = 25°C		–	24	32	mΩ
		V_{GS} = –10 V, I_D = –25 A	T_J = 25°C	–	17	21	mΩ
			T_J = 175°C (Note 4)	–	28	36	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = –20 V, V_{GS} = 0 V, f = 100 KHz		–	1200	–	pF
C_{oss}	Output Capacitance			–	480	–	pF
C_{rss}	Reverse Transfer Capacitance			–	27	–	pF
R_g	Gate Resistance	V_{GS} = –0.5 V, f = 1 MHz		–	38	–	Ω
$Q_{g(tot)}$	Total Gate Charge	V_{DD} = –20 V, I_D = –25 A	V_{GS} = 0 V to –10 V	–	17	23	nC
$Q_{g(-4.5)}$	Total Gate Charge		V_{GS} = 0 V to –4.5 V	–	8	–	nC
$Q_{g(th)}$	Threshold Gate Charge		V_{GS} = 0 V to –1 V	–	1	–	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = –20 V, I_D = –25 A		–	4	–	nC
Q_{gd}	Gate to Drain "Miller" Charge			–	2.5	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn-On Time	V_{DD} = –20 V, I_D = –25 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		–	–	45	ns
$t_{d(on)}$	Turn-On Delay Time			–	7	–	ns
t_r	Turn-On Rise Time			–	24	–	ns
$t_{d(off)}$	Turn-Off Delay Time			–	120	–	ns
t_f	Turn-Off Fall Time			–	40	–	ns
t_{off}	Turn-Off Time			–	–	235	ns
DRAIN–SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Voltage	V_{GS} = 0 V, I_{SD} = –25 A		–	–0.95	–1.25	V
		V_{GS} = 0 V, I_{SD} = –12.5 A		–	–0.9	–1.2	V
T_{rr}	Reverse Recovery Time	I_F = –25 A, dI_{SD}/dt = 100 A/μs		–	36	54	ns
Q_{rr}	Reverse Recovery Charge			–	22	33	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production
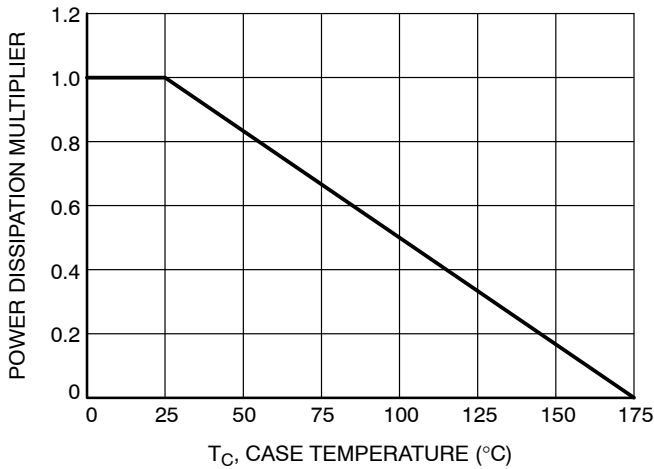
TYPICAL CHARACTERISTICS

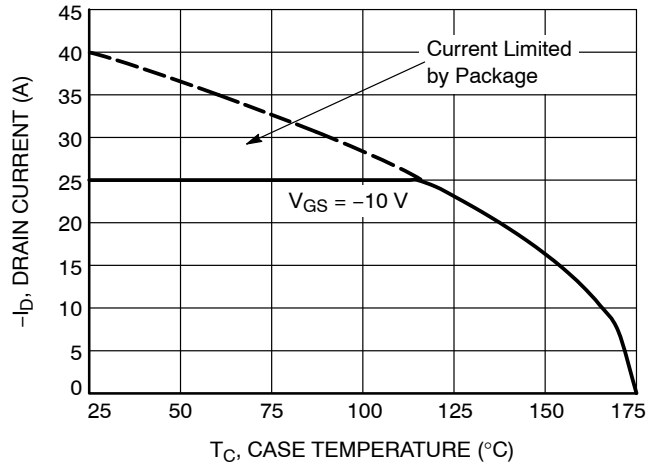**Figure 1. Normalized Power Dissipation vs. Case Temperature**

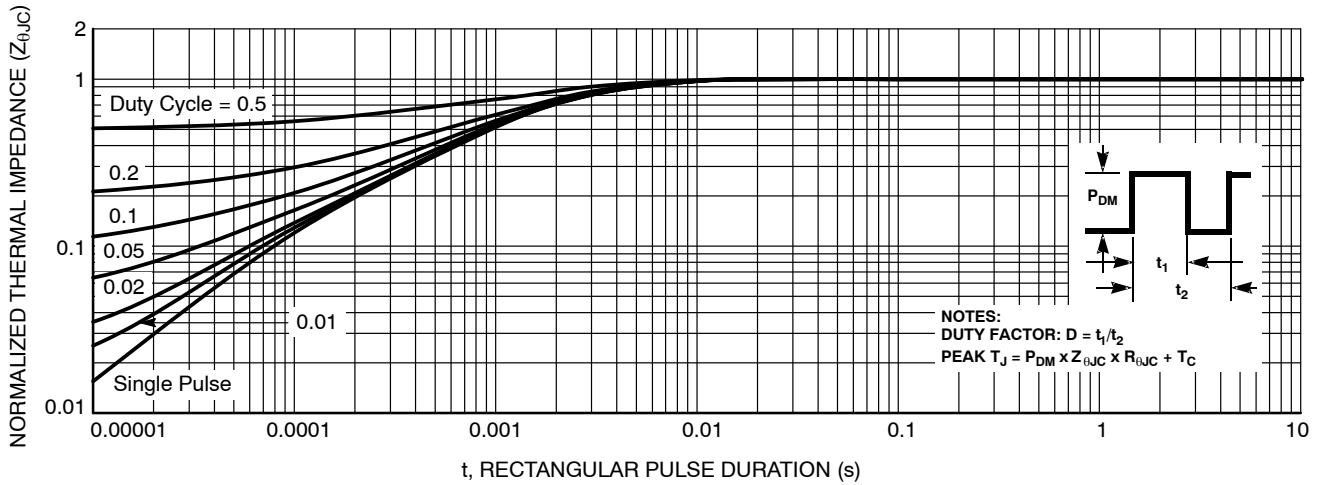**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 3. Normalized Maximum Transient Thermal Impedance

$T_C = 25\ ^oC$
FOR TEMPERATURES
ABOVE 25°C DERATE PEAK
CURRENT AS FOLLOWS:

$$I = I_{25} \left[\sqrt{\frac{175 - T_C}{150}} \right]$$
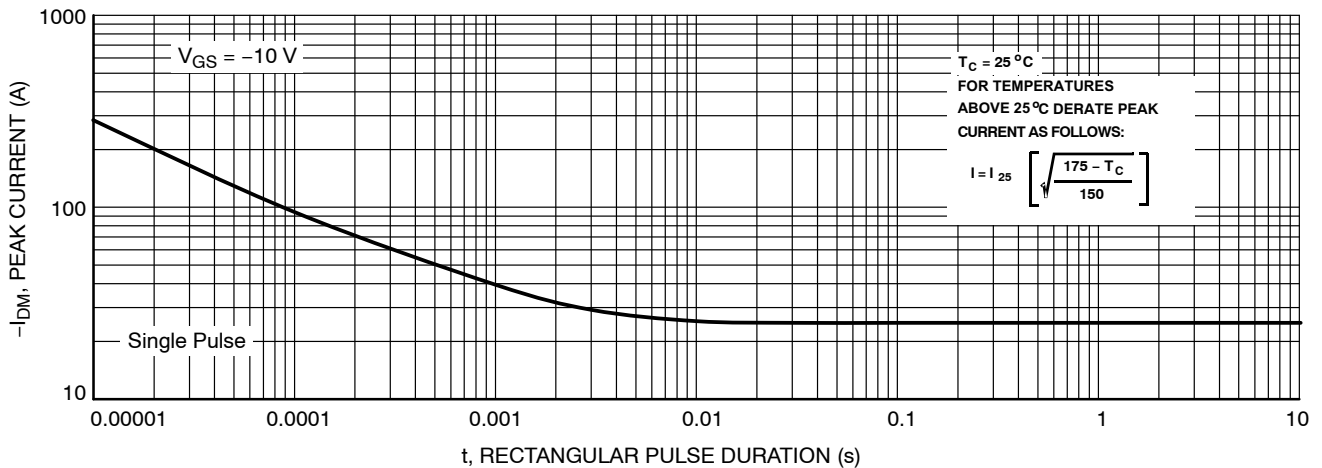
Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS
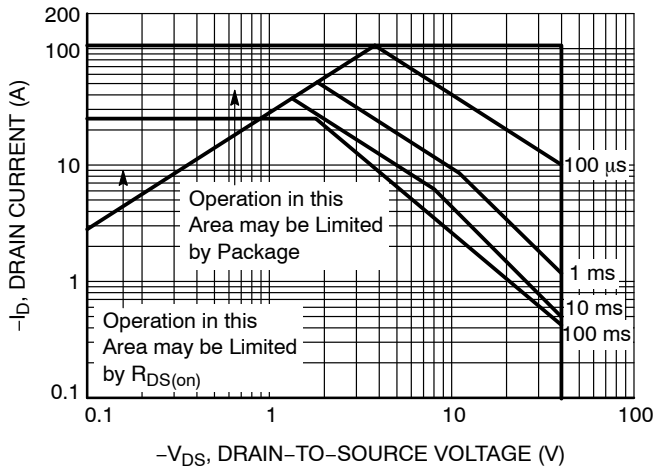
Figure 5. Forward Bias Safe Operating Area
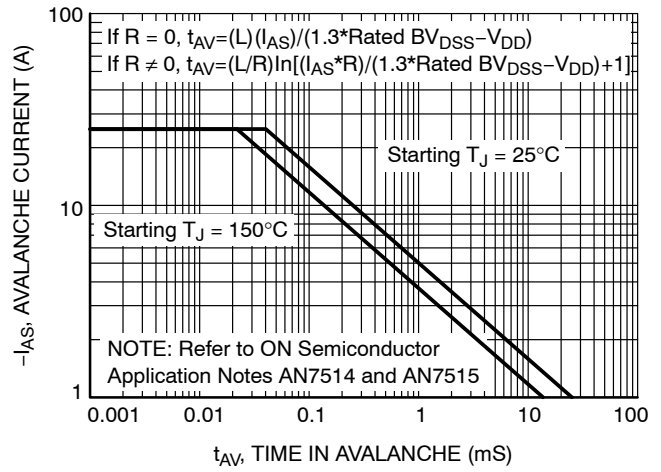
Figure 6. Unclamped Inductive Switching Capability
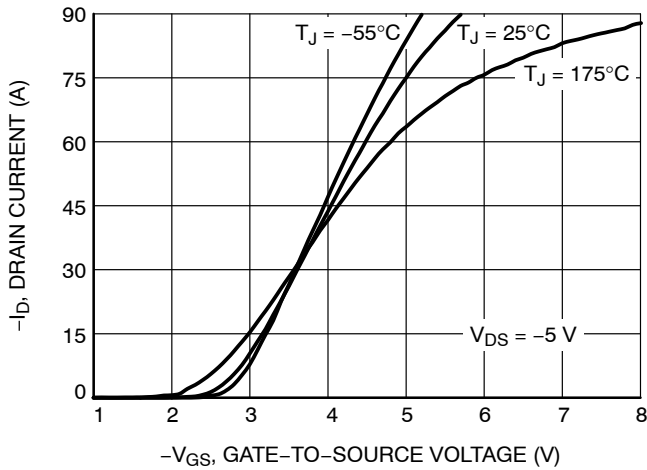
Figure 7. Transfer Characteristics
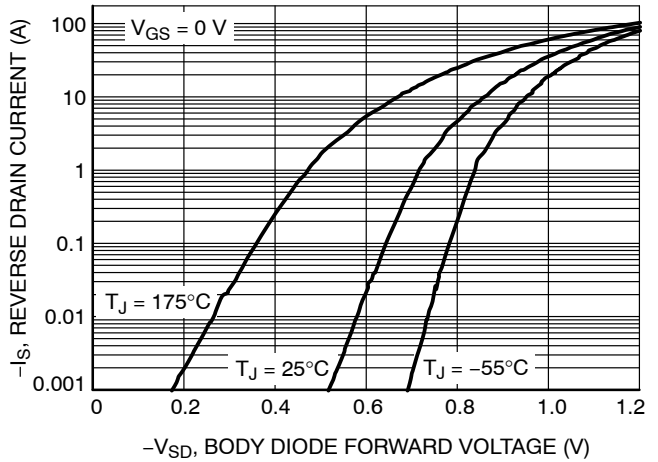
Figure 8. Forward Diode Characteristics
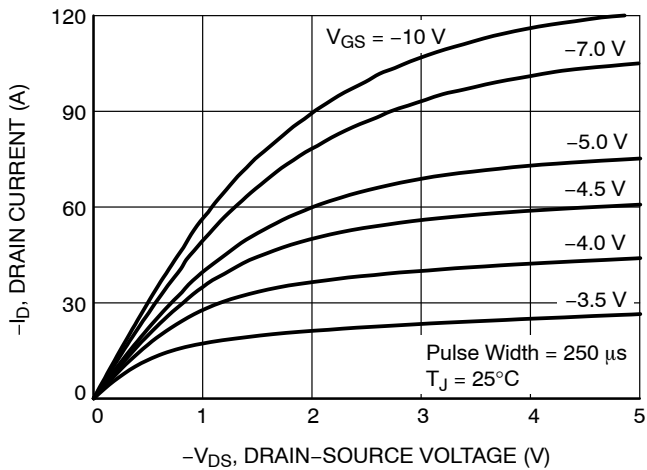
Figure 9. Saturation Characteristics
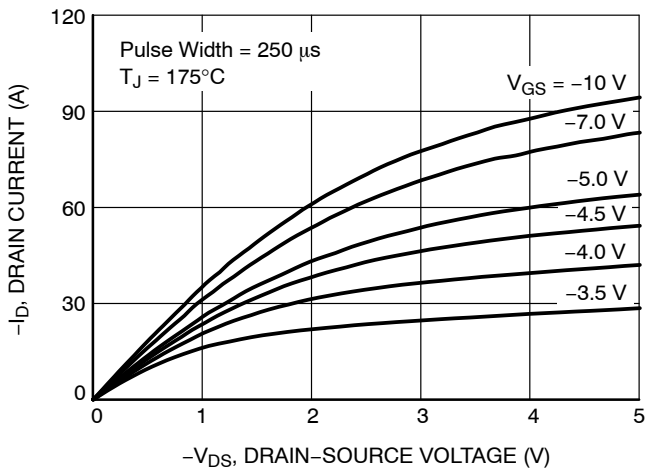
Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS
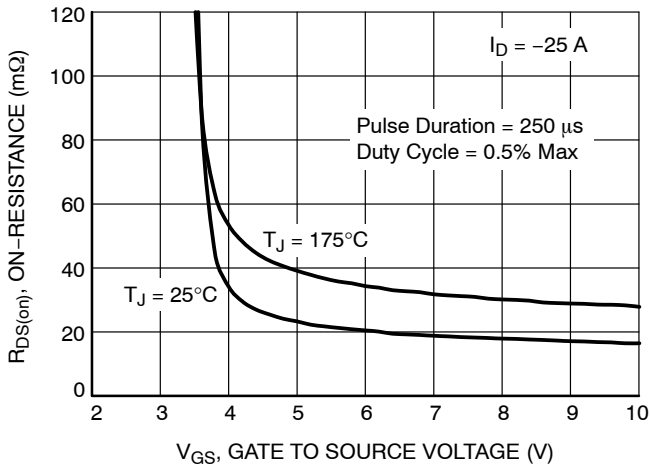
Figure 11. R$_{DS(on)}$ vs. Gate Voltage
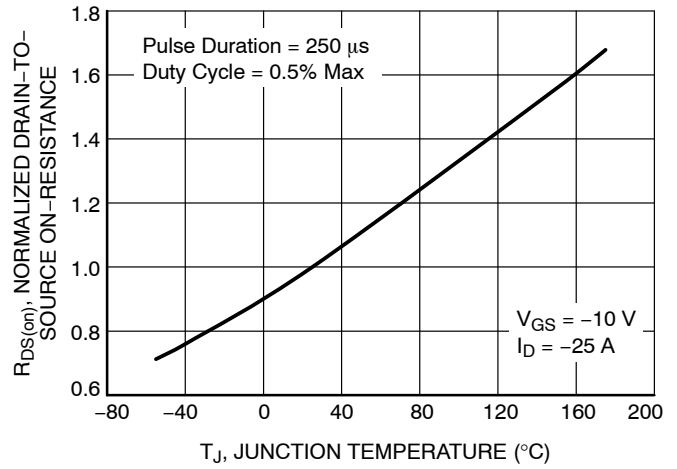
Figure 12. Normalized R$_{DS(on)}$ vs. Junction Temperature
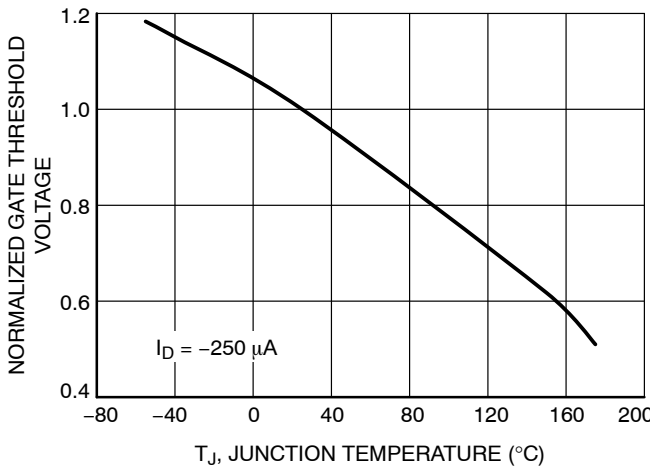
Figure 13. Normalized Gate Threshold Voltage vs. Temperature
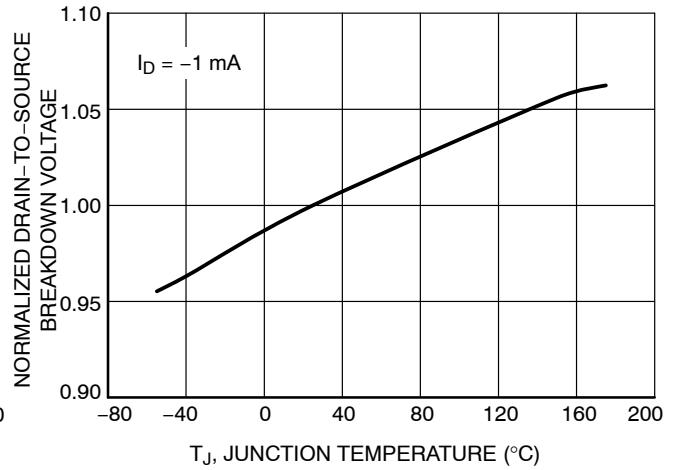
Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature
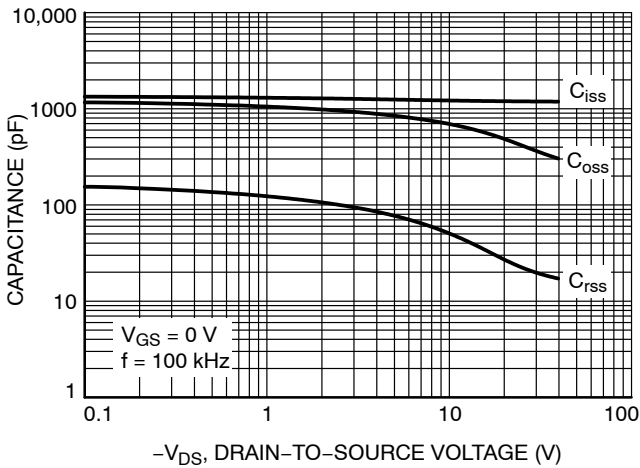
Figure 15. Capacitance vs. Drain−to−Source Voltage
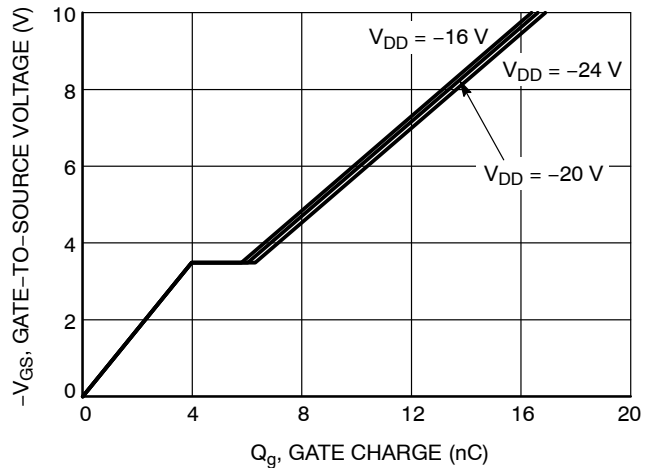
Figure 16. Gate Charge vs. Gate−to−Source Voltage

DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE O

DATE 30 SEP 2016

6.73
6.35

5.46
5.21

A

1.27
0.89

6.22
5.97

E
1.02 MAX

C

1   2   3

0.25 MAX
PLASTIC BODY
STUB

1   2   3

DIODE PRODUCTS VERSION

(0.59)

1.14
0.76

0.89
0.64

2.29

⊕ 0.25 Ⓜ A Ⓜ C

4.57

NON-DIODE PRODUCTS VERSION

5.55 MIN

4

6.50 MIN

6.40

1   3   2.85 MIN

1.25 MIN

2.28

4.56

LAND PATTERN RECOMMENDATION

SEE
NOTE D

4.32 MIN   4

5.21 MIN

3   2   1
E

NON-DIODE PRODUCTS VERSION

3   2   1

DIODE PRODUCTS VERSION

B

2.39
2.18

0.58
0.45

10.41
9.40

SEE DETAIL A

⌒ 0.10 B

GAGE PLANE

0.51

0.61
0.45

10°
0°

(1.54)

1.78
1.40

0.127 MAX

(2.90)

SEATING PLANE

DETAIL A
(ROTATED -90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252,
   ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER
   ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED
   CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURSS,
   MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD
   TO228P991X239-3N.
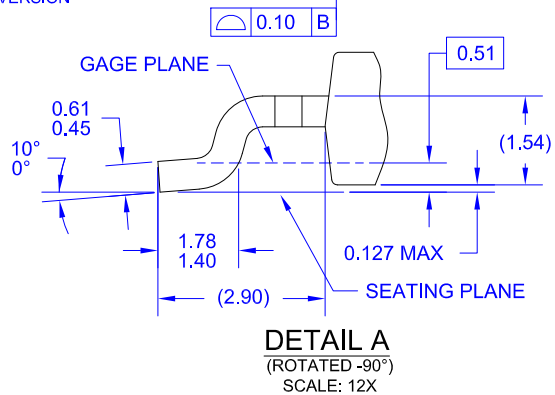
DOCUMENT NUMBER:	98AON13810G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	DPAK3 (TO−252 3 LD)		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

◊