

FDMA8051L

MOSFET, Single N-Channel, POWERTRENCH[®]

40 V, 10 A, 14 mΩ

General Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $r_{DS(on)}$ and gate charge provide excellent switching performance.

Features

- Max $r_{DS(on)}$ = 14 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$
- Max $r_{DS(on)}$ = 18 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 8.5\text{ A}$
- Low Profile – 0.8 mm maximum in the new package MicroFET 2 x 2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

Application

- DC-DC Buck Converters

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	10	A
	– Pulsed (Note 3)	80	
P_D	Power dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.4	W
	Power dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	0.9	
T_J , T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping [†]
051	FDMA8051L	MicroFET 2x2	3000 Units/ Tape & Reel

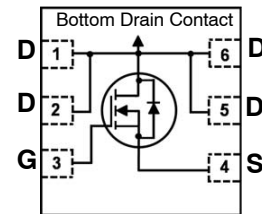
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



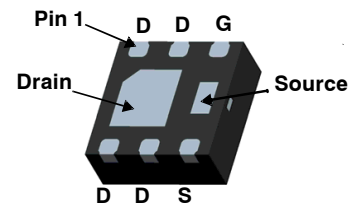
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ELECTRICAL CONNECTION

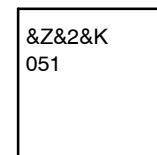


Single N-Channel MOSFET



MicroFET 2x2
(WDFN6 2x2, 0.65P)
CASE 511DB

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = Numeric Date Code
&K = Lot Code
051 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 1 of this data sheet.

FDMA8051L

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		22		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V			100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		-5		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 10 A		11	14	mΩ
		V _{GS} = 4.5 V, I _D = 8.5 A		14	18	
		V _{GS} = 10 V, I _D = 10 A, T _J = 125°C		15	19	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 10 A		35		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 20 V, V _{GS} = 0 V, f = 1MHz		901	1260	pF
C _{oss}	Output Capacitance			251	350	
C _{rss}	Reverse Transfer Capacitance			16	25	
R _g	Gate Resistance		0.1	0.6	1.8	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn – On Delay Time	V _{DD} = 20 V, I _D = 10 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		6.4	13	ns
t _r	Rise Time			1.8	10	
t _{D(off)}	Turn – Off Delay Time			17	31	
t _f	Fall Time			1.8	10	
Q _g	Total Gate Charge	V _{GS} = 0V to 10 V V _{GS} = 0V to 4.5 V V _{DD} = 20 V, I _D = 10 A		14	20	nC
Q _g	Total Gate Charge			6.4	9.0	
Q _{gs}	Total Gate Charge			2.4	3.7	
Q _{gd}	Gate to Source Charge			1.8	2.5	

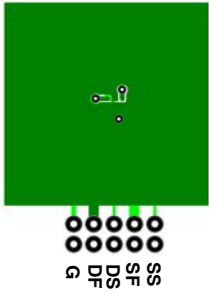
DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2 A (Note 2)		0.7	1.2	V
		V _{GS} = 0 V, I _S = 10 A (Note 2)		0.8	1.2	
t _{rr}	Reverse Recovery Time	I _F = 10 A, di/dt = 100 A/μs		23	37	ns
Q _{rr}	Reverse Recovery Charge			6.7	14	nC

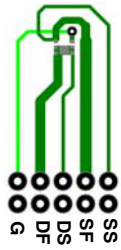
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 52°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 145°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Pulsed I_D limited by junction temperature, $t_{d} \leq 100 \mu s$, please refer to SOA curve for more details.

TYPICAL CHARACTERISTICS $T_J = 25^\circ C$ unless otherwise noted

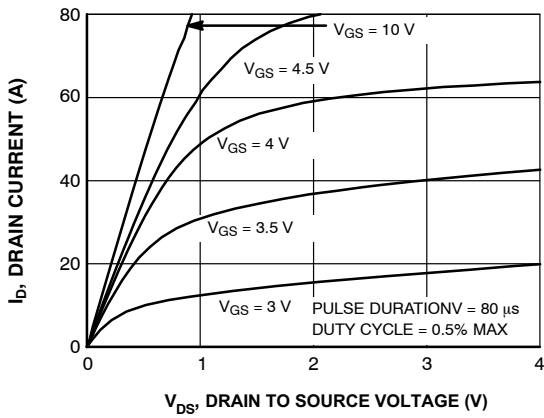


Figure 1. On Region Characteristics

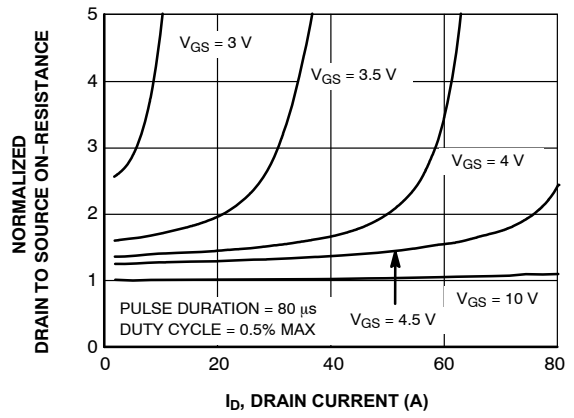


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

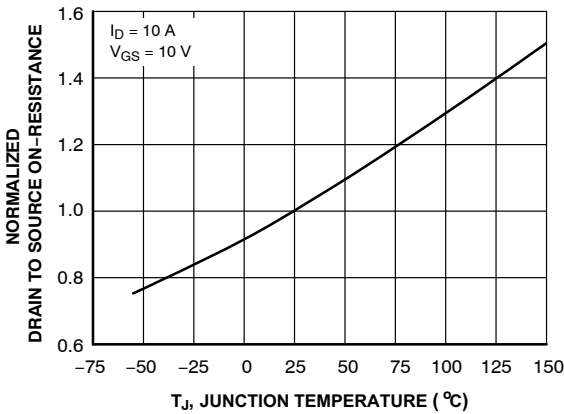


Figure 3. Normalized On Resistance vs. Junction Temperature

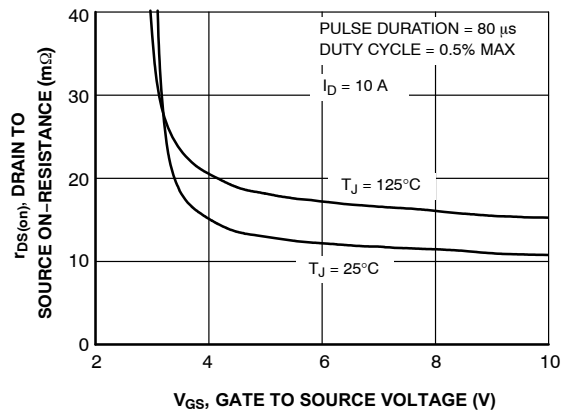


Figure 4. On-Resistance vs. Gate to Source Voltage

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted (continued)

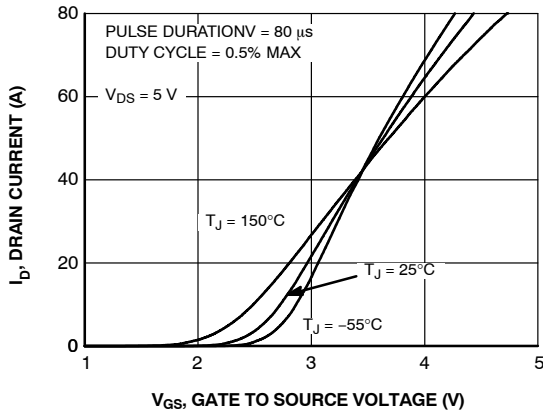


Figure 5. Transfer Characteristics

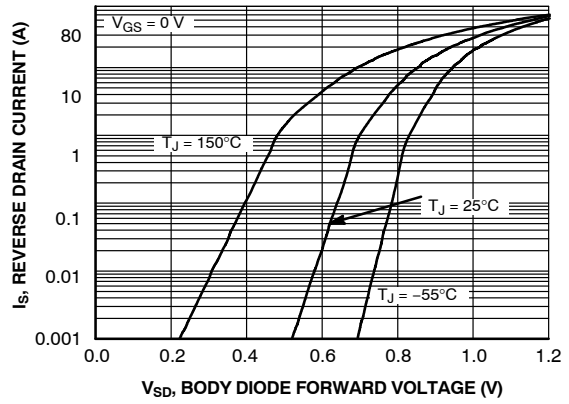


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

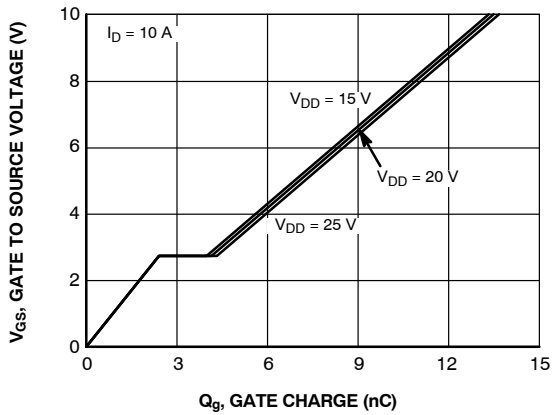


Figure 7. Gate Charge Characteristics

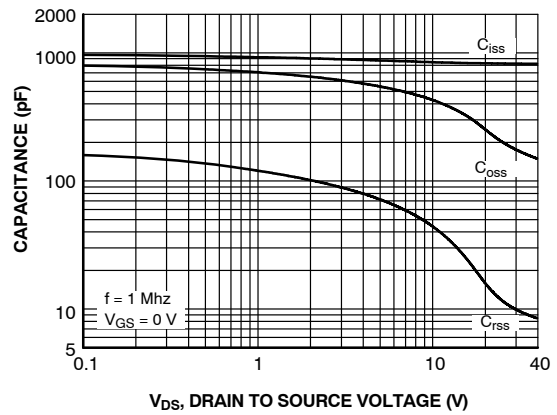


Figure 8. Capacitance vs. Drain to Source Voltage

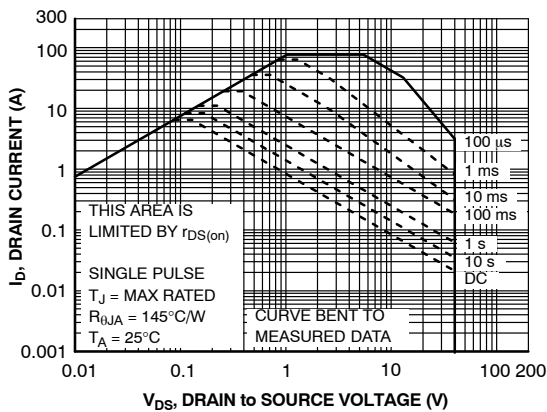


Figure 9. Forward Bias Safe Operating Area

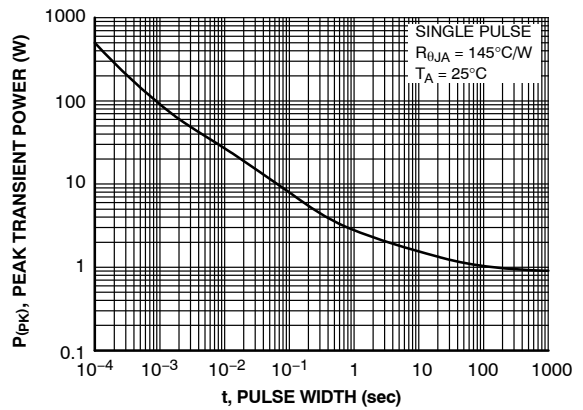


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted (continued)

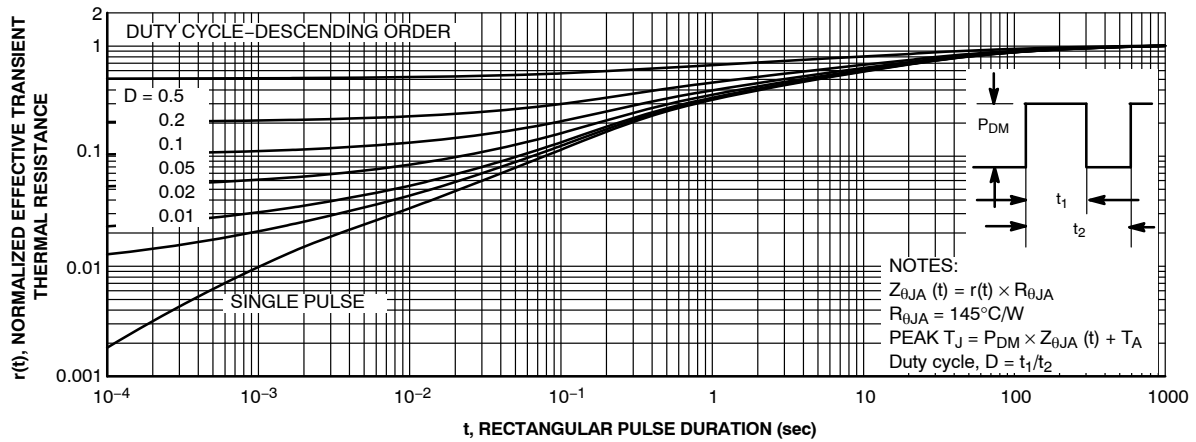


Figure 11. Single Pulse Junction-to-Ambient Transient Thermal Response Curve

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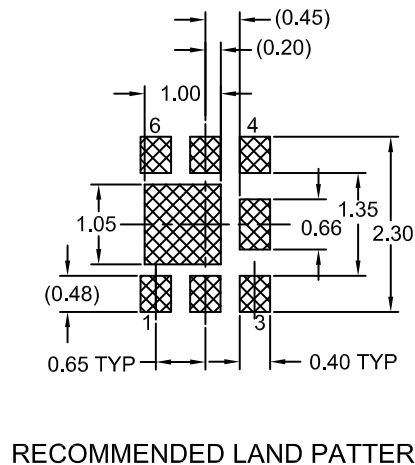
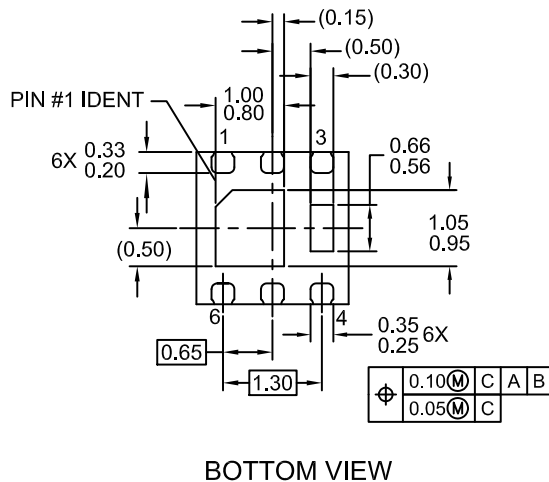
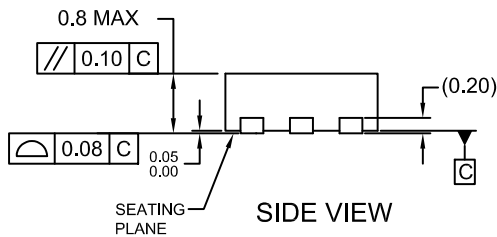
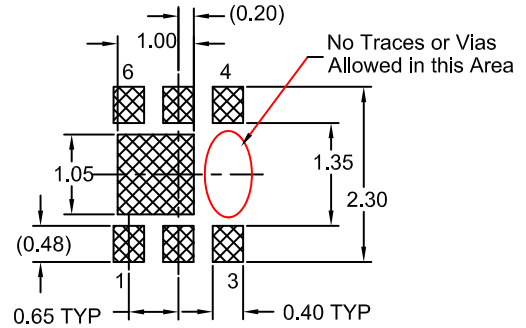
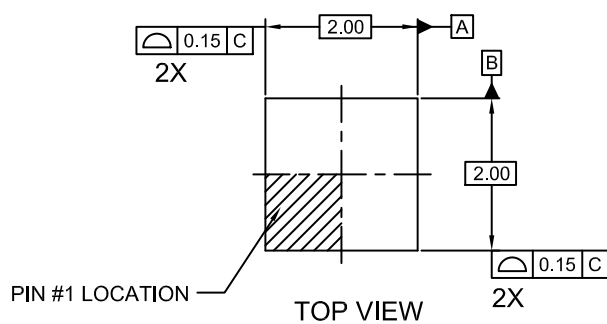
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



WDFN6 2x2, 0.65P
CASE 511DB
ISSUE O

DATE 31 AUG 2016



NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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