

# LSF0204-Q100

4-bit bidirectional multi-voltage level translator; open-drain; push-pull

Rev. 2 — 28 October 2020

Product data sheet

## 1. General description

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The LSF0204-Q100 is an 4 channel bidirectional multi-voltage level translator for open-drain and push-pull applications. It supports up to 100 MHz up translation and  $\geq 100$  MHz down translation at  $\leq 30$  pF capacitive load. There is no need for a direction pin which minimizes system effort.

The LSF0204-Q100 supports 5 V tolerant I/O pins for compatibility with TTL levels in a variety of applications. The ability to set up different voltage translation levels on each channel makes the device very flexible and suitable for a lot of different applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from  $-40$  °C to  $+125$  °C
- Bidirectional voltage translation with no direction pin
- Up translation
  - $\geq 100$  MHz;  $C_L = 15$  pF, 30 pF
  - $\geq 80$  MHz;  $C_L = 50$  pF
- Down translation
  - $\geq 120$  MHz;  $C_L = 15$  pF, 30 pF
  - $\geq 100$  MHz;  $C_L = 50$  pF
- Hot insertion
- Bidirectional voltage level translation between:
  - 0.8 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.2 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
  - 1.8 V and 2.5 V, 3.3 V and 5.0 V
  - 2.5 V and 3.3 V and 5.0 V
  - 3.3 V and 5.0 V
- Low standby current
- 5 V tolerant I/O pins to support TTL
- Low  $R_{ON}$  provides less signal distortion
- Latch-up performance exceeds 100 mA per JESD78 class II level A
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM ANSI/ESDA/JEDEC JS-002 exceeds 1000 V

## 3. Applications

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- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I<sup>2</sup>C, and other interfaces in Telecom infrastructure
- Industrial
- Personal computing

## 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
LSF0204PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

## 5. Functional diagram

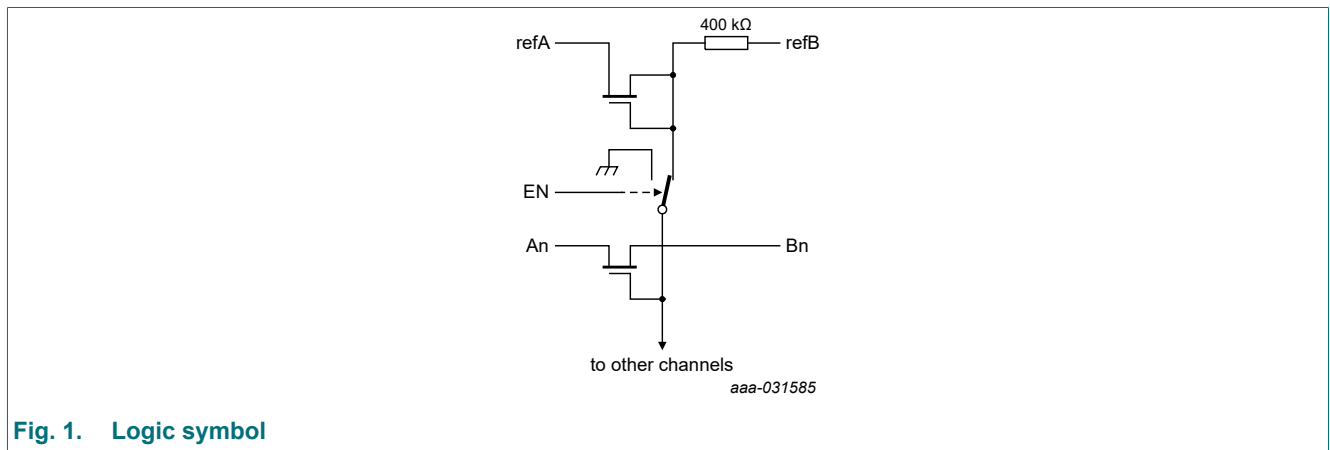


Fig. 1. Logic symbol

## 6. Pinning information

### 6.1. Pinning

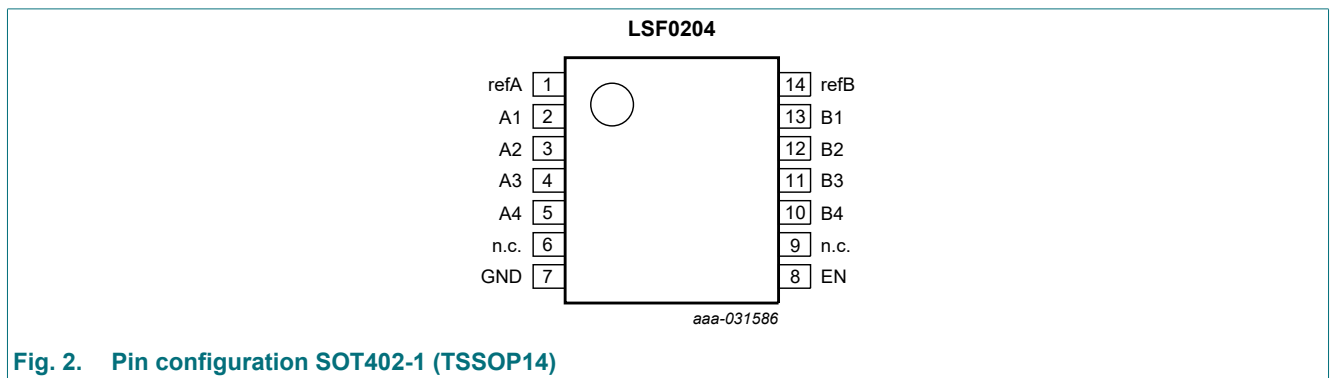


Fig. 2. Pin configuration SOT402-1 (TSSOP14)

## 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
refA	1	reference voltage A (EN input circuit is referenced to refA)
A1, A2, A3, A4	2, 3, 4, 5	data input/output A
n.c.	6, 9	not connected
GND	7	ground (0 V)
EN	8	enable input (active HIGH)
B1, B2, B3, B4	13, 12, 11, 10	data input/output B
refB	14	reference voltage B

## 7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	input/output
EN <sup>[1]</sup>	An, Bn channel
H	An = Bn
L	Z

[1] EN input circuit is referenced to refA

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage	pins refA, refB, An, Bn and EN <sup>[1]</sup>	-0.5	+7.0	V
$I_{I/O}$	input/output current	pins refA, refB, An and Bn; continuous channel current	-	+128	mA
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	<sup>[2]</sup>	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage	pins refA, refB, An, Bn and EN	0.0	5.0	V
$I_{I/O}$	input/output current	pins refA, refB, An and Bn; continuous channel current	-	+64	mA
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	EN input	-	10	ns/V

## 10. Static characteristics

**Table 6. Static characteristics**

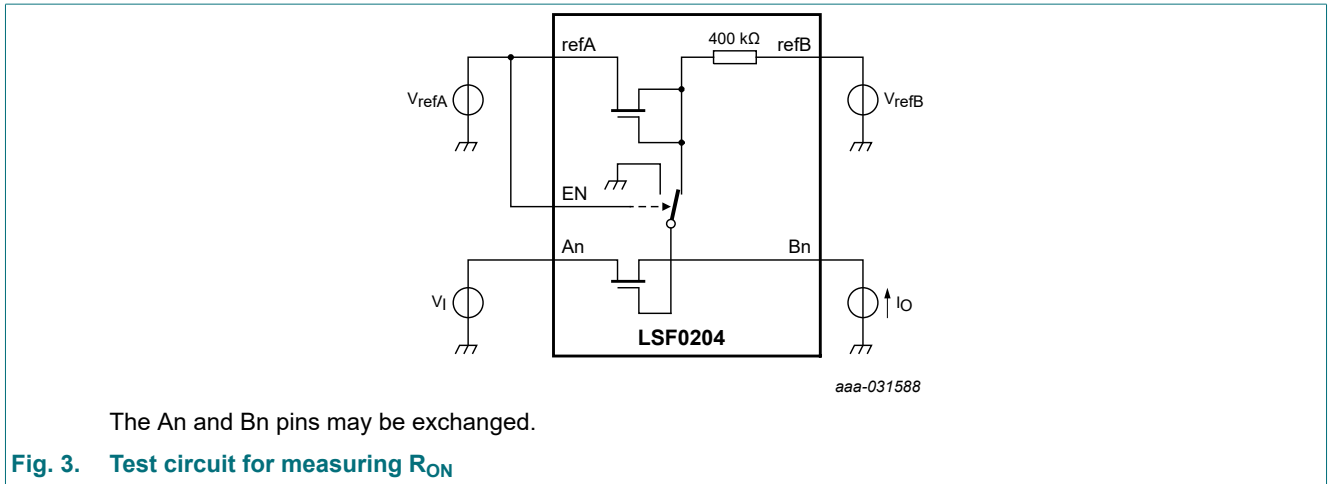
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +125 °C			Unit
			Min	Typ [1]	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>I(EN)</sub> = 0 V; I <sub>I</sub> = -18 mA	-1.2	-	-	V
I <sub>IH</sub>	HIGH-level input current	V <sub>I</sub> = 5 V; V <sub>I(EN)</sub> = 0 V	-	-	5	μA
I <sub>I</sub>	input current	EN input; V <sub>refA</sub> = 4.5 V; V <sub>refB</sub> = 5.5 V; V <sub>I(EN)</sub> = 0 V to V <sub>refA</sub> ; I <sub>O</sub> = 0 A	-	-	±1	μA
V <sub>IH</sub>	HIGH-level input voltage	EN input				
		V <sub>refA</sub> = 1.5 V to 4.5 V	0.7V <sub>refA</sub>	-	-	V
		V <sub>refA</sub> = 1.0 V to 1.5 V	0.8V <sub>refA</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	EN input				
		V <sub>refA</sub> = 1.5 V to 4.5 V	-	-	0.3V <sub>refA</sub>	V
		V <sub>refA</sub> = 1.0 V to 1.5 V	-	-	0.3V <sub>refA</sub>	V
I <sub>refB-A</sub>	leakage current refB to refA	V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V; I <sub>O</sub> = 0 A; V <sub>I</sub> = 3.3 V or GND	-	-	3.5	μA
I <sub>GND</sub>	ground current	V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V; I <sub>O</sub> = 0 A; V <sub>I</sub> = 3.3 V or GND	-	0.2	-	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>refA</sub> = V <sub>refB</sub> = V <sub>I(EN)</sub> = 0 V; I <sub>O</sub> = 0 A; V <sub>I</sub> = 5 V or GND	-	-	±1	μA
C <sub>I</sub>	input capacitance	pins refA, refB and EN; V <sub>I</sub> = 3 V or 0 V	-	7	-	pF
C <sub>io(off)</sub>	OFF-state input/output capacitance	pins An, Bn; V <sub>O</sub> = 0 V or 3 V; V <sub>I(EN)</sub> = 0 V	-	3	6	pF
C <sub>io(on)</sub>	ON-state input/output capacitance	pins An, Bn; V <sub>O</sub> = 0 V or 3 V; V <sub>I(EN)</sub> = 3.0 V	-	8	13	pF
R <sub>ON</sub>	ON resistance	see <a href="#">Fig. 3</a> [2]				
		V <sub>I</sub> = 0 V; I <sub>O</sub> = 64 mA;				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 3.3 V; V <sub>refB</sub> = 5 V	-	3	-	Ω
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 5 V	-	4	-	Ω
		V <sub>I</sub> = 0 V; I <sub>O</sub> = 32 mA;				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.0 V; V <sub>refB</sub> = 5 V	-	7	-	Ω
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 5 V	-	4	-	Ω
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 2.5 V; V <sub>refB</sub> = 5 V	-	3.5	-	Ω
		V <sub>I</sub> = 1.8 V; I <sub>O</sub> = 15 mA; V <sub>refA</sub> = V <sub>I(EN)</sub> = 3.3 V; V <sub>refB</sub> = 5 V	-	5	-	Ω
		V <sub>I</sub> = 1 V; I <sub>O</sub> = 10 mA; V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V	-	8	-	Ω
		V <sub>I</sub> = 0 V; I <sub>O</sub> = 10 mA; V <sub>refA</sub> = V <sub>I(EN)</sub> = 1 V; V <sub>refB</sub> = 3.3 V	-	6	-	Ω
		V <sub>I</sub> = 0 V; I <sub>O</sub> = 10 mA; V <sub>refA</sub> = V <sub>I(EN)</sub> = 1 V; V <sub>refB</sub> = 1.8 V	-	6	-	Ω

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

[2] Measured by the voltage drop between the An and Bn pins at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) pins.

4-bit bidirectional multi-voltage level translator; open-drain; push-pull



## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ; for waveforms see Fig. 4 and Fig. 5; for test circuit see Fig. 6

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+125\text{ °C}$			Unit
			Min	Typ[1]	Max	
<b>Translating down (3.3 V to 1.8 V)</b>						
$t_{PLH}$	LOW to HIGH propagation delay	An to Bn or Bn to An				
		$V_{refA} = V_{I(EN)} = 1.8\text{ V}$ ; $V_{refB} = 3.3\text{ V}$ ; $V_I = 3.3\text{ V}$ ; $V_M = 1.15\text{ V}$				
		$C_L = 15\text{ pF}$	-	0.3	5.19	ns
		$C_L = 30\text{ pF}$	-	0.5	5.29	ns
$t_{PHL}$	HIGH to LOW propagation delay	An to Bn or Bn to An				
		$V_{refA} = V_{I(EN)} = 1.8\text{ V}$ ; $V_{refB} = 3.3\text{ V}$ ; $V_I = 3.3\text{ V}$ ; $V_M = 1.15\text{ V}$				
		$C_L = 15\text{ pF}$	-	0.5	4.5	ns
		$C_L = 30\text{ pF}$	-	0.7	4.7	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	EN to An or Bn				
		$V_{refA} = V_{I(EN)} = 1.8\text{ V}$ ; $V_{refB} = 3.3\text{ V}$ ; $V_M = 1.15\text{ V}$				
		$C_L = 15\text{ pF}$	-	11	15	ns
		$C_L = 30\text{ pF}$	-	12	16.5	ns
$t_{PZL}$	OFF-state to LOW propagation delay	EN to An or Bn				
		$V_{refA} = V_{I(EN)} = 1.8\text{ V}$ ; $V_{refB} = 3.3\text{ V}$ ; $V_M = 1.15\text{ V}$				
		$C_L = 15\text{ pF}$	-	23	37	ns
		$C_L = 30\text{ pF}$	-	30	40	ns
		$C_L = 50\text{ pF}$	-	33	45	ns

## 4-bit bidirectional multi-voltage level translator; open-drain; push-pull

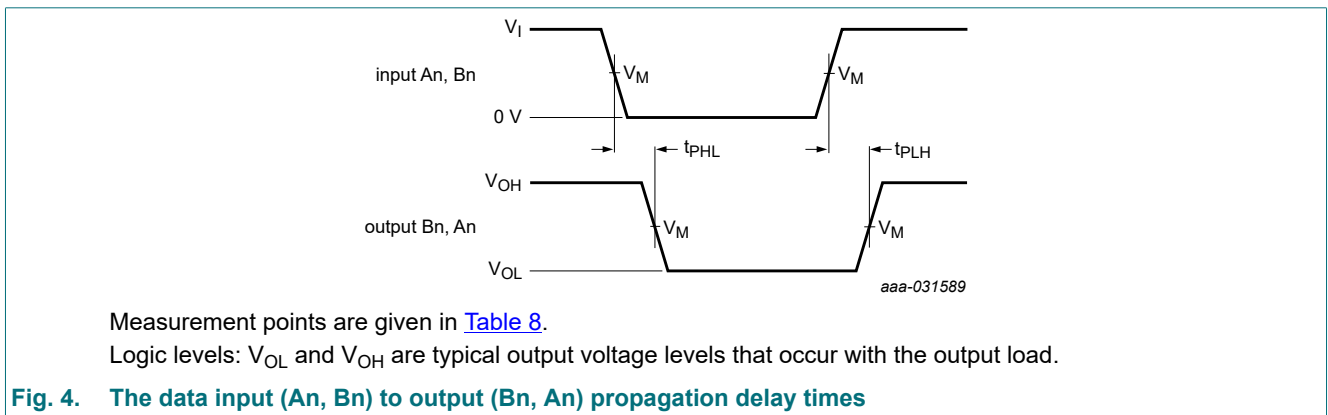
Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
f <sub>max</sub>	maximum frequency	V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V; V <sub>I</sub> = 3.3 V; V <sub>M</sub> = 1.15 V				
		C <sub>L</sub> = 15 pF	-	120	-	MHz
		C <sub>L</sub> = 30 pF	-	120	-	MHz
		C <sub>L</sub> = 50 pF	-	100	-	MHz
<b>Translating down (3.3 V to 1.2 V)</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay	An to Bn or Bn to An				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.2 V; V <sub>refB</sub> = 3.3 V; V <sub>I</sub> = 3.3 V; V <sub>M</sub> = 0.85 V				
		C <sub>L</sub> = 15 pF	-	0.3	3.8	ns
		C <sub>L</sub> = 30 pF	-	0.5	3.9	ns
		C <sub>L</sub> = 50 pF	-	0.8	4.1	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	An to Bn or Bn to An				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.2 V; V <sub>refB</sub> = 3.3 V; V <sub>I</sub> = 3.3 V; V <sub>M</sub> = 0.85 V				
		C <sub>L</sub> = 15 pF	-	0.6	4.3	ns
		C <sub>L</sub> = 30 pF	-	0.7	4.5	ns
		C <sub>L</sub> = 50 pF	-	0.9	4.7	ns
f <sub>max</sub>	maximum frequency	V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.2 V; V <sub>refB</sub> = 3.3 V; V <sub>I</sub> = 3.3 V; V <sub>M</sub> = 0.85 V				
		C <sub>L</sub> = 15 pF	-	120	-	MHz
		C <sub>L</sub> = 30 pF	-	120	-	MHz
		C <sub>L</sub> = 50 pF	-	100	-	MHz
<b>Translating up (1.8 V to 3.3 V)</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay	An to Bn or Bn to An				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V; V <sub>I</sub> = 1.8 V; V <sub>M</sub> = 0.9 V				
		C <sub>L</sub> = 15 pF	-	0.2	5.1	ns
		C <sub>L</sub> = 30 pF	-	0.4	5.3	ns
		C <sub>L</sub> = 50 pF	-	0.6	5.7	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	An to Bn or Bn to An				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V; V <sub>I</sub> = 1.8 V; V <sub>M</sub> = 0.9 V				
		C <sub>L</sub> = 15 pF	-	0.7	5.3	ns
		C <sub>L</sub> = 30 pF	-	1	6.4	ns
		C <sub>L</sub> = 50 pF	-	1.3	6.7	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	EN to An or Bn				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V; V <sub>M</sub> = 0.9 V				
		C <sub>L</sub> = 15 pF	-	11	15	ns
		C <sub>L</sub> = 30 pF	-	12	16.5	ns
		C <sub>L</sub> = 50 pF	-	13	18	ns

4-bit bidirectional multi-voltage level translator; open-drain; push-pull

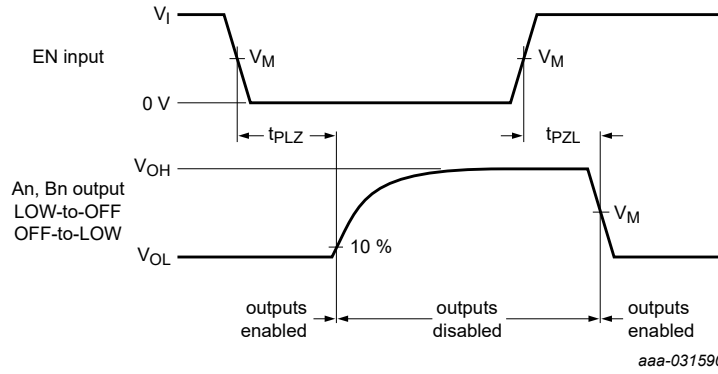
Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
t <sub>PZL</sub>	OFF-state to LOW propagation delay	EN to An or Bn				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V; V <sub>M</sub> = 0.9 V				
		C <sub>L</sub> = 15 pF	-	23	37	ns
		C <sub>L</sub> = 30 pF	-	30	40	ns
f <sub>max</sub>	maximum frequency	V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.8 V; V <sub>refB</sub> = 3.3 V; V <sub>I</sub> = 1.8 V; V <sub>M</sub> = 0.9 V; R <sub>L</sub> = 100 Ω				
		C <sub>L</sub> = 15 pF	-	100	-	MHz
		C <sub>L</sub> = 30 pF	-	100	-	MHz
		C <sub>L</sub> = 50 pF	-	80	-	MHz
<b>Translating up (1.2 V to 1.8 V)</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay	An to Bn or Bn to An				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.2 V; V <sub>refB</sub> = 1.8 V; V <sub>I</sub> = 1.2 V; V <sub>M</sub> = 0.6 V				
		C <sub>L</sub> = 15 pF	-	0.2	6.85	ns
		C <sub>L</sub> = 30 pF	-	0.4	7.05	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	An to Bn or Bn to An				
		V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.2 V; V <sub>refB</sub> = 1.8 V; V <sub>I</sub> = 1.2 V; V <sub>M</sub> = 0.6 V				
		C <sub>L</sub> = 15 pF	-	1	5.4	ns
		C <sub>L</sub> = 30 pF	-	1.3	6.5	ns
f <sub>max</sub>	maximum frequency	V <sub>refA</sub> = V <sub>I(EN)</sub> = 1.2 V; V <sub>refB</sub> = 1.8 V; V <sub>I</sub> = 1.2 V; V <sub>M</sub> = 0.6 V; R <sub>L</sub> = 100 Ω				
		C <sub>L</sub> = 15 pF	-	100	-	MHz
		C <sub>L</sub> = 30 pF	-	100	-	MHz
		C <sub>L</sub> = 50 pF	-	80	-	MHz

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

11.1. Waveforms and test circuit



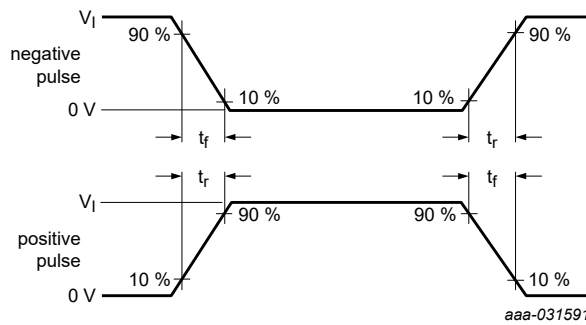
4-bit bidirectional multi-voltage level translator; open-drain; push-pull



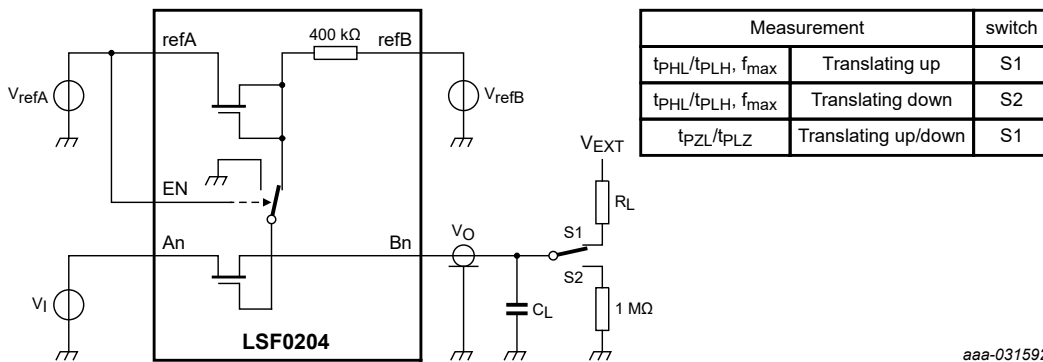
Measurement points are given in Table 8.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 5. The enable (EN) to output (An, Bn) propagation delay times



a.  $V_I$  source waveform



b. Test circuit

Test data is given in Table 8; The An and Bn pins may be exchanged.

All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz;  $Z_O = 50 \Omega$ .

Definitions test circuit:  $C_L$  = Load capacitance including jig and probe capacitance;  $R_L$  = Load resistance; S1/S2 = Test selection switch.

Fig. 6. Test circuit for measuring switching times

Table 8. Test data

Input	Load		$V_{EXT}$		
	$C_L$	$R_L$			
$t_r, t_f$		$t_{PLH}, t_{PHL}, t_{PLZ}, t_{PZL}$	$f_{max}$	$t_{PLH}, t_{PHL}, f_{max}$	$t_{PLZ}, t_{PZL}$ [1]
$\leq 2$ ns	15 pF, 30 pF, 50 pF	500 $\Omega$	100 $\Omega$	$V_{refB}$	$V_{refA}, V_{refB}$

[1] For measuring  $t_{PLZ}, t_{PZL}$  (translating up)  $V_{EXT} = V_{refB}$ .  
 For measuring  $t_{PLZ}, t_{PZL}$  (translating down)  $V_{EXT} = V_{refA}$ .



## 12. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

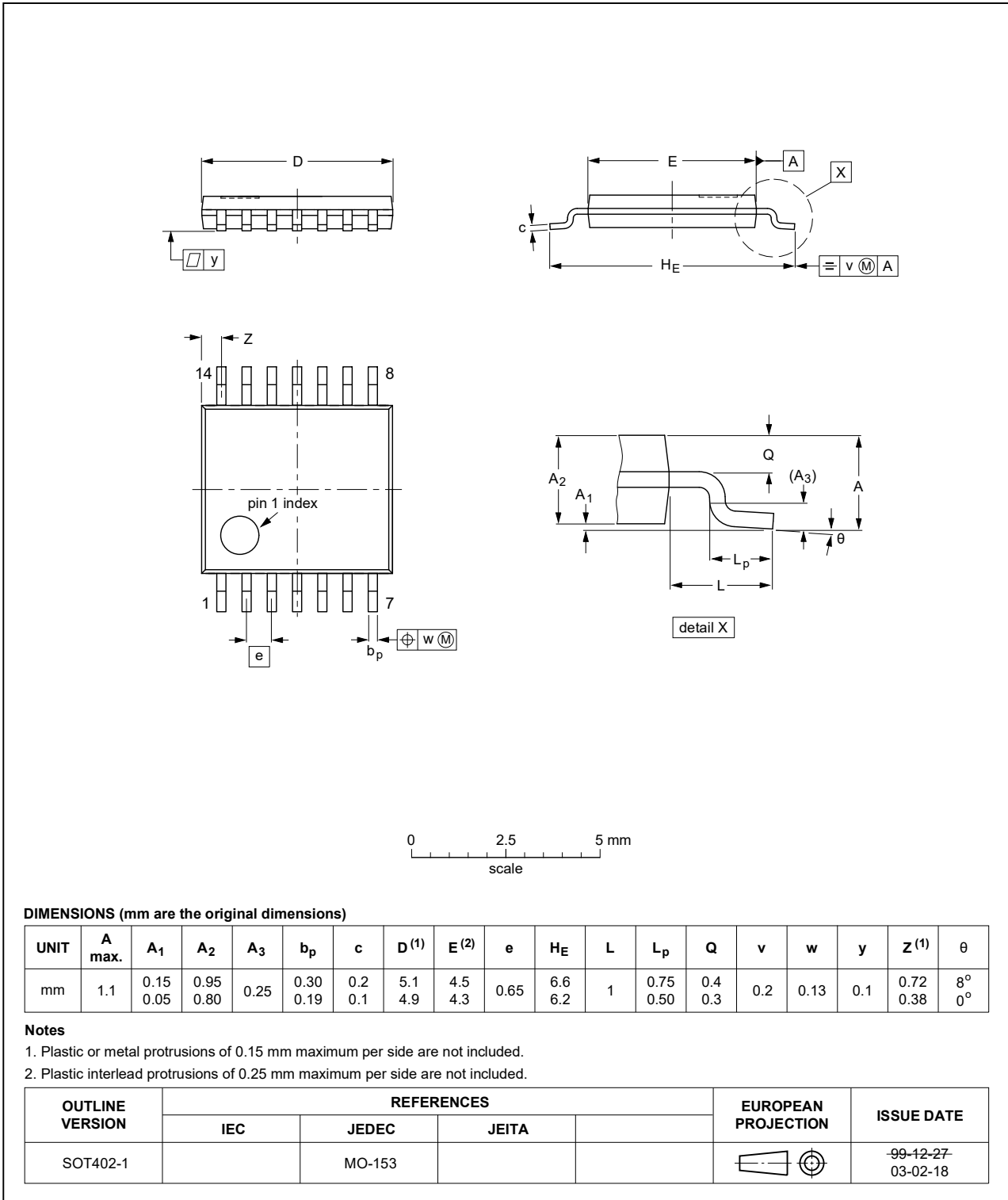


Fig. 7. Package outline SOT402-1 (TSSOP14)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LSF0204_Q100 v.2	20201028	Product data sheet	-	LSF0204_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Table 7</a>: <math>f_{\max}</math> values corrected.</li> </ul>			
LSF0204_Q100 v.1	20200818	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 28 October 2020

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