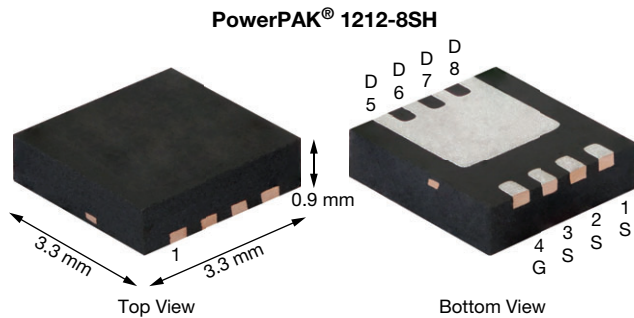


N-Channel 30 V (D-S) Fast Switching MOSFET



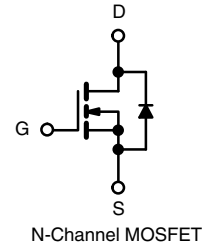
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Synchronous rectification
- Load switch



PRODUCT SUMMARY	
V _{DS} (V)	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0075
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.0082
Q _g typ. (nC)	18
I _D (A)	17.8
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH112DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	10 S	STEADY STATE	UNIT	
Drain-source voltage	V _{DS}	30	30	V	
Gate-source voltage	V _{GS}	±12	±12		
Continuous drain current (T _J = 150 °C) ^a	I _D	T _C = 25 °C	17.8	11.3	A
		T _C = 70 °C	14.2	9.1	
Pulsed drain current	I _{DM}	60	60		
Continuous source current (diode conduction) ^a	I _S	3.2	1.3		
Single avalanche current	I _{AS}	L = 0.1 mH	20	20	mJ
Single avalanche energy			E _{AS}	20	
Maximum power dissipation ^a	P _D	T _C = 25 °C	3.8	1.5	W
		T _C = 70 °C	2	0.8	
Operating junction and storage temperature range	T _J , T _{stg}	-50 to +150		°C	
Soldering recommendations (peak temperature) ^{b, c}		260			

Notes

- Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^a	t ≤ 10 s	R _{thJA}	24	33	°C/W
	Steady state		65	81	
Maximum junction-to-foot (drain)	Steady state	R _{thJC}	1.9	2.4	

Note

a. Surface mounted on 1" x 1" FR4 board

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6	-	1.5	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V	-	-	±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	40	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 17.8 A	-	0.0060	0.0075	Ω
		V _{GS} = 4.5 V, I _D = 17 A	-	0.0065	0.0082	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 17.8 A	-	97	-	S
Diode forward voltage ^a	V _{SD}	I _S = 3.2 A, V _{GS} = 0	-	0.7	1.2	V
Dynamic ^b						
Input capacitance	C _{ISS}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	2610	-	pF
Output capacitance	C _{OSS}		-	340	-	
Reverse transfer capacitance	C _{RSS}		-	145	-	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 17.8 A	-	18	27	nC
Gate-source charge	Q _{gs}		-	6.2	-	
Gate-drain charge	Q _{gd}		-	3.1	-	
Gate resistance	R _g	f = 1 MHz	0.5	1.2	1.8	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω	-	10	15	ns
Rise time	t _r		-	10	15	
Turn-off delay time	t _{d(off)}		-	65	100	
Fall time	t _f		-	10	15	
Body diode reverse recovery time	t _{rr}	I _F = 3.2 A, di/dt = 100 A/μs	-	30	60	nC
Body diode reverse recovery charge	Q _{rr}		-	18	-	

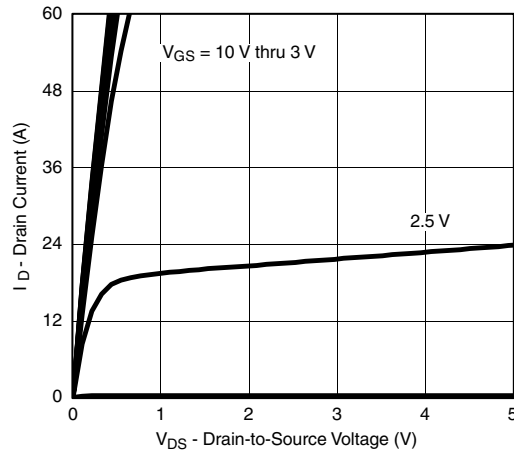
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

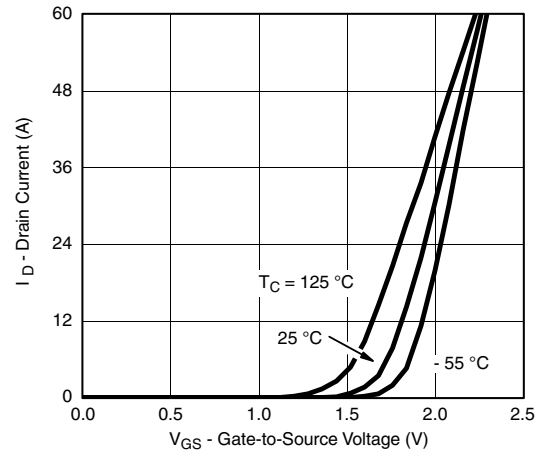
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



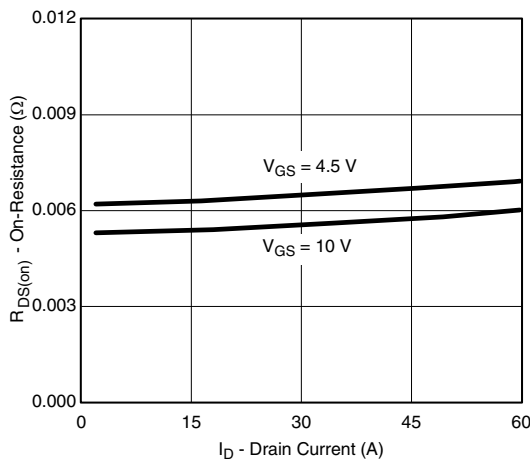
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



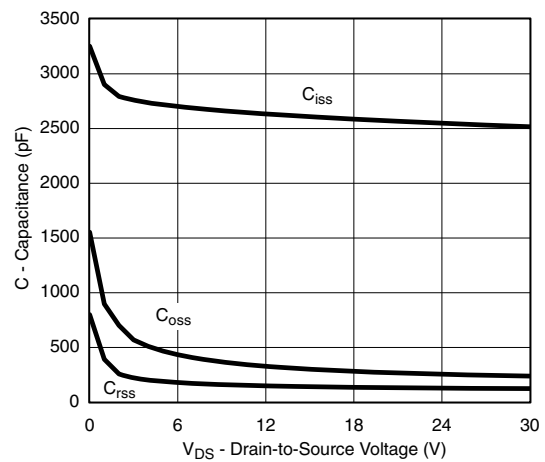
Output Characteristics



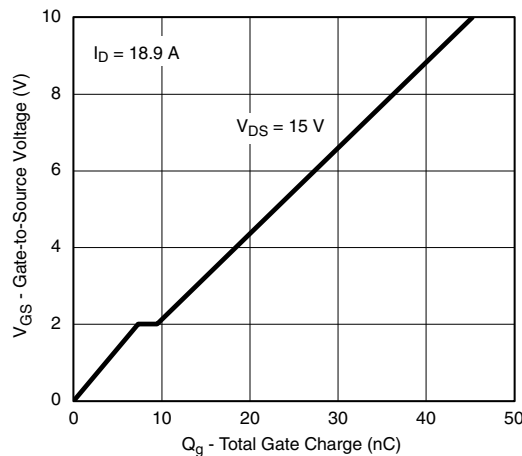
Transfer Characteristics



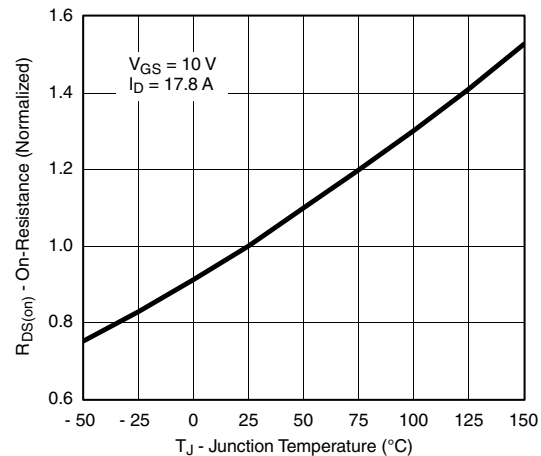
On-Resistance vs. Drain Current



Capacitance



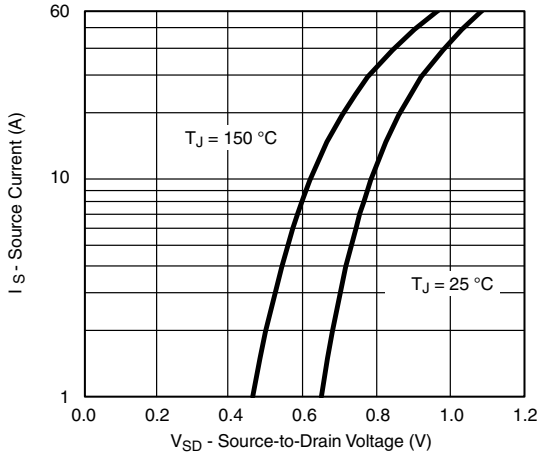
Gate Charge



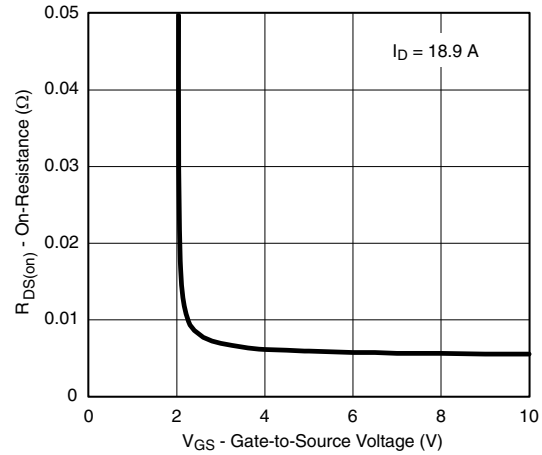
On-Resistance vs. Junction Temperature



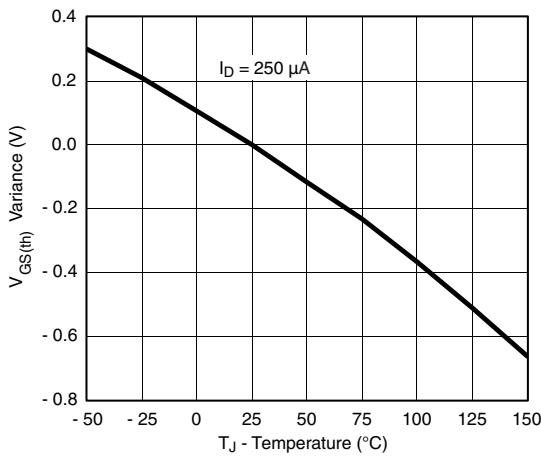
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



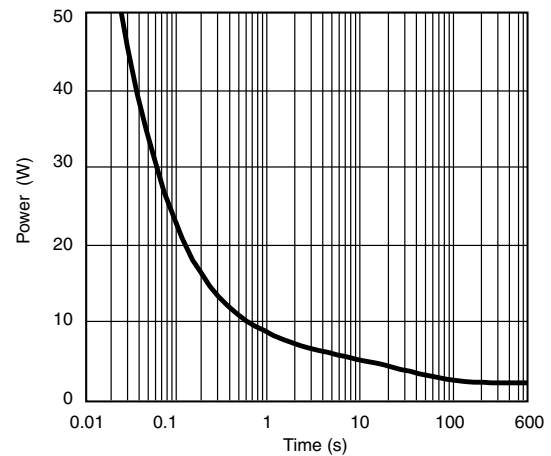
Source-Drain Diode Forward Voltage



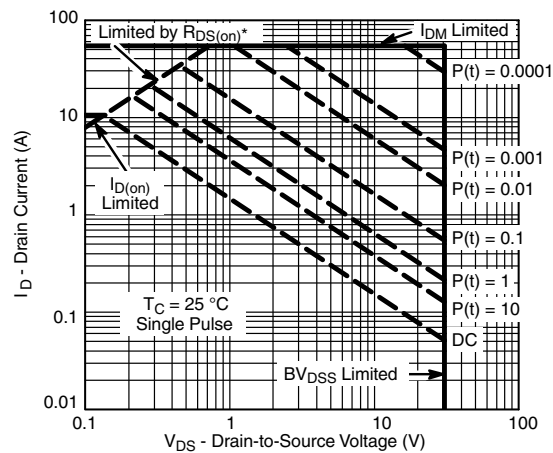
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



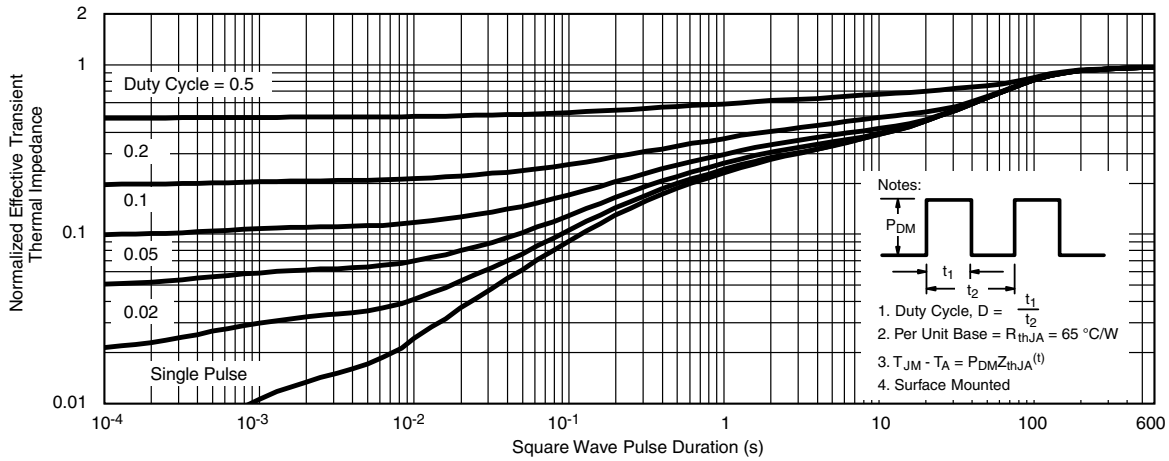
Single Pulse Power, Junction-to-Ambient



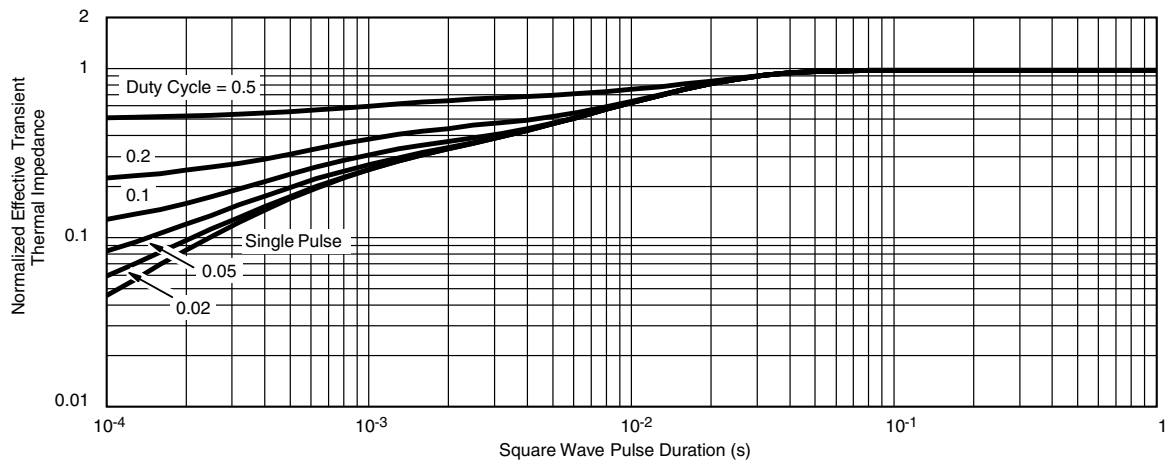
Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

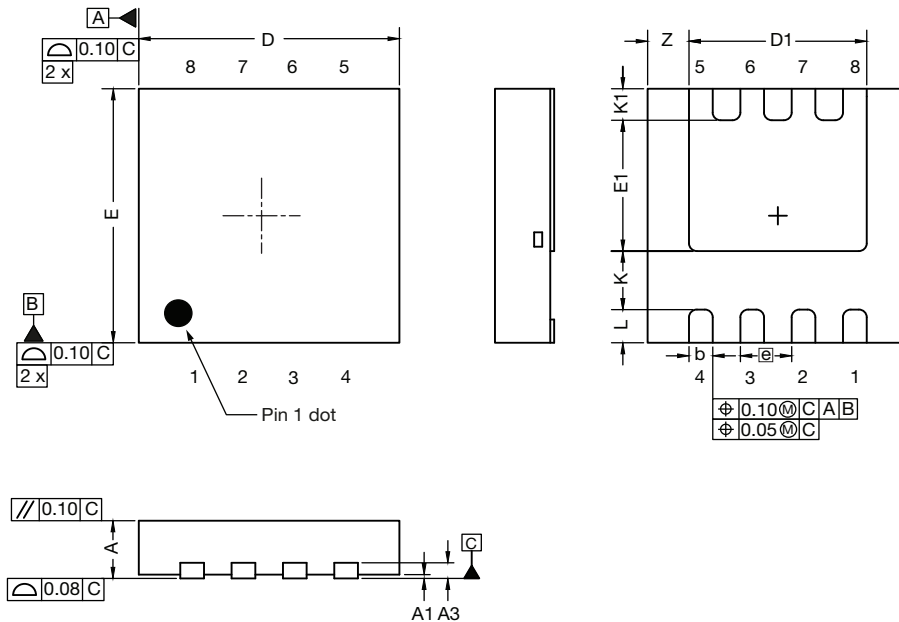


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?79345.



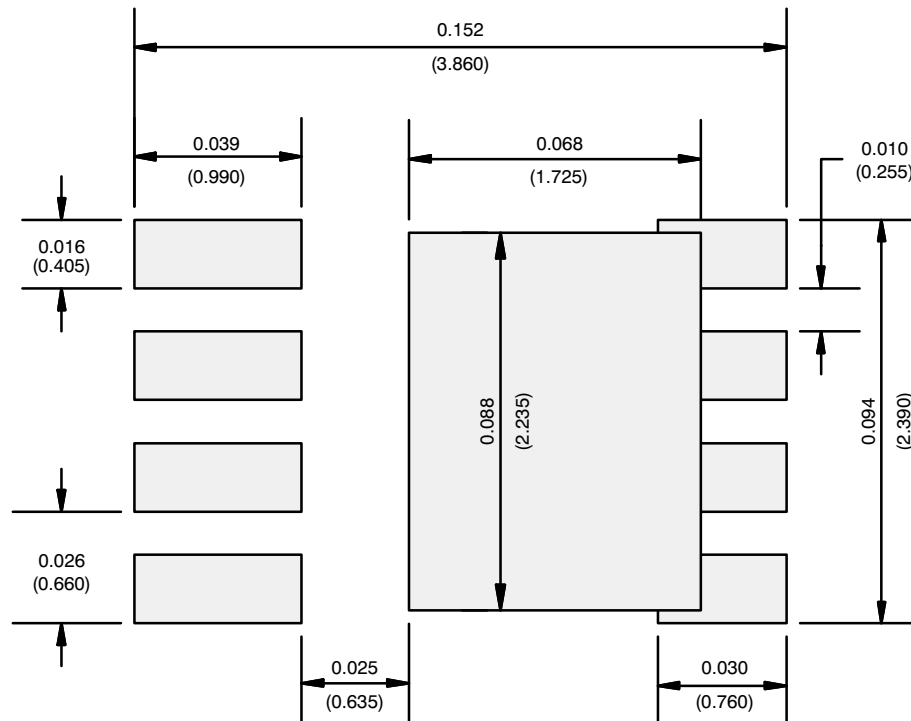
Case Outline for PowerPAK® 1212-SWLH and PowerPAK® 1212-8SH



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: S20-0930-Rev. C, 07-Dec-2020
DWG: 6062

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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