RE46C194

CMOS Low-Voltage Photoelectric Smoke Detector ASIC with Interconnect and Timer Mode

Features

- 3V Lithium or Two AA Battery Operation
- Low Quiescent Current Consumption
- Programmable IRED Drive Current
- Programmable Photo Amp Setup
- 6-Bit ADC
- Programmable Alarm Limits
- Long-Term Drift Adjustment
- Chamber Test
- 9-Minute Timer for Hush Operation
- Programmable Feature Selection
- Low Battery Test
- Temporal or Continuous Horn Pattern
- Horn Synchronization
- Auto Alarm Locate
- Local Alarm Memory
- Interconnect up to 40 Detectors
- Remote CO Alarm Response
- Compatible with the RE46C191

Description

The RE46C194 is a low-power, low-voltage CMOS photoelectric type smoke detector IC. With minimal external components, this circuit will provide all the required features for a photoelectric smoke detector.

The design incorporates a programmable gain photo amplifier for use with an infrared emitter/detector pair.

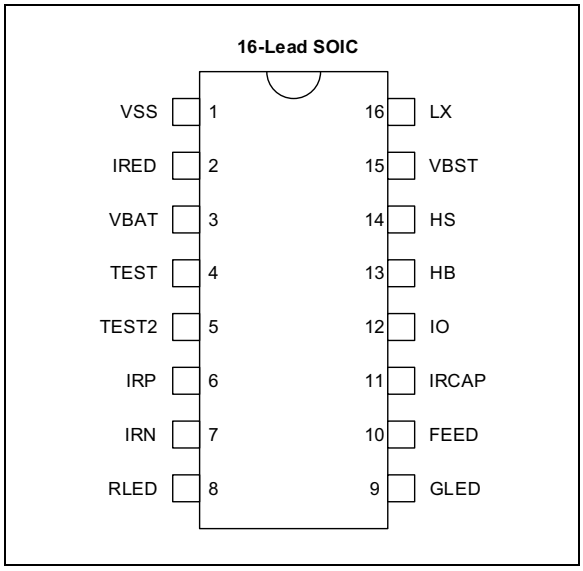
An internal oscillator strobes power to the smoke detection circuitry every 10 seconds to keep the standby current to a minimum. If smoke is sensed, the detection rate is increased to verify an Alarm condition. A High Gain mode is available for push-button chamber testing.

A check for a Low-Battery condition is performed every 86 seconds and chamber integrity is tested once every 43 seconds, when in Standby mode. The temporal horn pattern supports the NFPA 72 emergency evacuation signal.

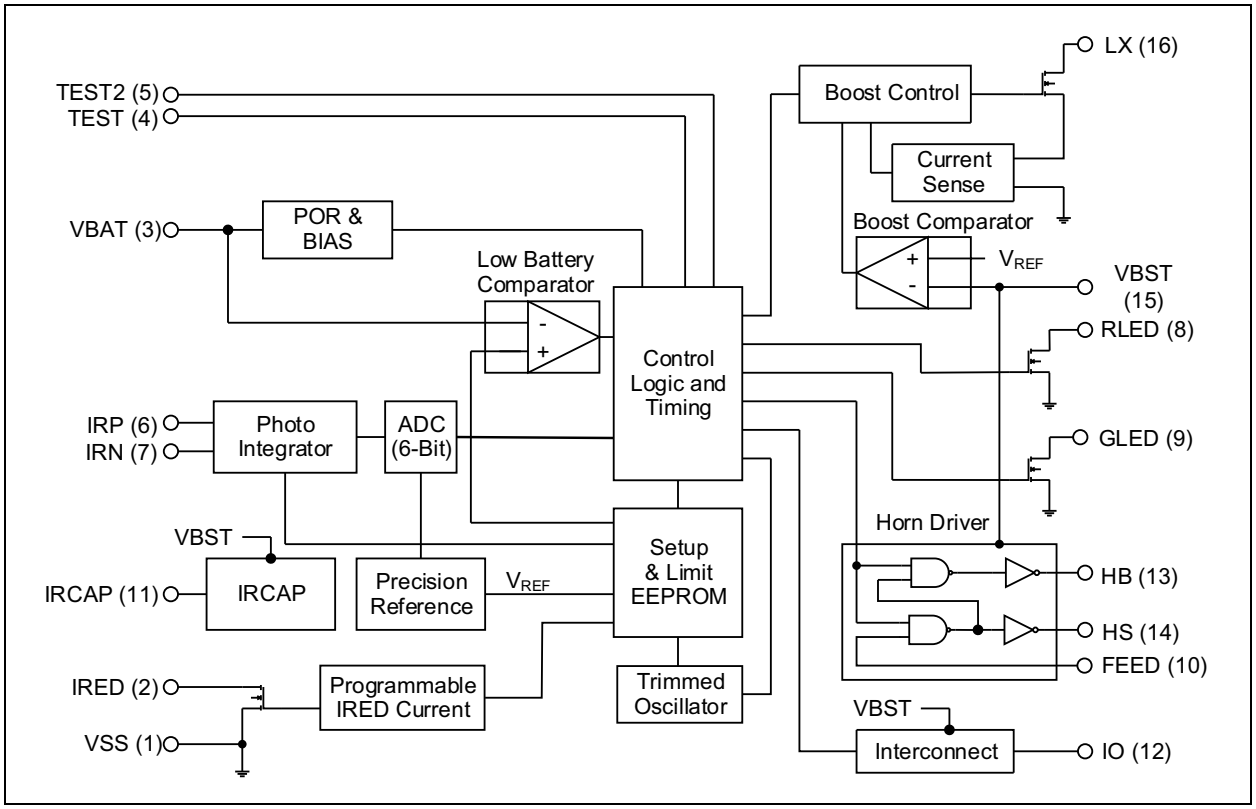
An interconnect pin allows multiple detectors to be connected such that, when one unit alarms, all units will sound.

An internal 9-minute timer can be used for a Hush mode.

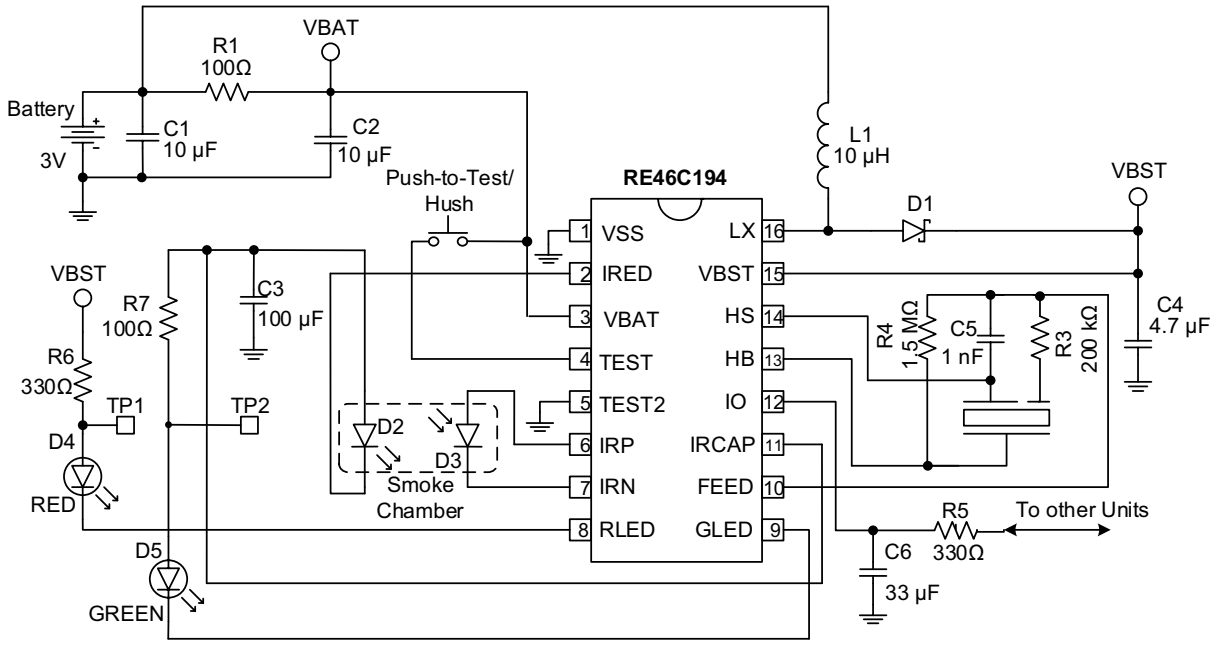
Package Types



Functional Block Diagram



Typical Application



Note 1: C2 should be located as close as possible to the device power pins, and C1 should be located as close as possible to the VSS power input connection.

2: R3, R4 and C5 are typical values and may be adjusted to maximize sound pressure.

3: The boost regulator in High Boost mode (e.g. V_{BST} = 8.5V or 10V) can draw current pulses of greater than 0.6A and is therefore very sensitive to series resistance. Critical components of this resistance are the inductor DC resistance, the internal resistance of the battery and the resistance in the connections from the inductor to the battery, as well as from the inductor to the LX pin and from the V_{SS} pin to the battery. In order to function properly under full load at V_{BAT} = 2V, the total of the inductor and interconnect resistances should not exceed 0.3Ω. The internal battery resistance should be no more than 0.5Ω and a low ESR capacitor of 10 µF or more should be connected in parallel with the battery, to average the current draw over the boost converter cycle.

4: Schottky diode D1 must have a maximum peak current rating of at least 0.8A. For best results it should have a forward voltage specification of less than 0.5V at 0.8A and low reverse leakage.

5: Inductor L1 must have a maximum peak current rating of at least 0.8A.

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

Supply Voltage ..... V_{DD} = 5.5V, V_{BST} = 13V
Input Voltage Range Except FEED and TEST Pins ..... V_{IN} = -0.3V to V_{DD} + 0.3V
FEED Input Voltage Range ..... V_{INFD} = -10V to 22V
TEST Input Voltage Range ..... V_{INTEST} = -0.3V to VBST + 0.3V
LX Voltage ..... V_{LX} = -0.3V to 13V
IRCAP Voltage ..... V_{IRCAP} = 5.5V
Input Current Except FEED Pin ..... I_{IN} = 10 mA
Continuous Operating Current (HS, HB and VBST Pins) ..... I_O = 20 mA
Continuous Operating Current (IRED Pin) ..... I_{OIR} = 300 mA
Operating Temperature ..... T_A = 0°C to +60°C
Storage Temperature ..... T_{STG} = -55°C to +125°C
ESD Human Body Model ..... V_{HBM} = 2 kV
ESD Machine Model ..... V_{MM} = 150V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = 0°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** to **Note 4**).

Parameters	Symbol	Test Pins	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{BAT}	3	2	—	5	V	Operating
Supply Current	I_{BAT1}	3	—	1	2	µA	Standby, inputs low, no loads, Boost off, no Smoke Check
Standby Boost Current	I_{BST1}	15	—	100	—	nA	Standby, inputs low, no loads, Boost off, no Smoke Check
IRCAP Supply Current	I_{IRCAP}	11	—	500	—	µA	During Smoke Check
Boost Voltage	V_{BST1}	15	3.3	3.6	3.9	V	IRCAP charging for Smoke Check, GLED operation; I_{OUT} = 20 mA
	V_{BST2}	15	8	8.5	9		No local alarm, RLED Operation, I_{OUT} = 20 mA, IO as an input
	V_{BST3}	15	9.4	10	10.6		
Input Leakage	I_{INOPP}	6	-200	—	200	pA	$I_{RP} = V_{BAT}$ or V_{SS}
	I_{INOPN}	7					$I_{RN} = V_{BAT}$ or V_{SS}
	I_{IHF}	10	—	20	50	µA	FEED = 22V, V_{BST} = 9V
	I_{ILF}	10	-50	-15	—		FEED = -10V, V_{BST} = 10.7V
Input Voltage Low	V_{IL1}	10	—	—	2.7	V	FEED, V_{BST} = 9V
	V_{IL2}	12	—	—	800	mV	No local alarm, IO as an input
Input Voltage High	V_{IH1}	10	6.2	—	—	V	FEED; V_{BST} = 9V
	V_{IH2}	12	2	—	—		No local alarm, IO as an input
IO Hysteresis	V_{HYST1}	12	—	150	—	mV	
Input Pull-Down Current	I_{PD1}	4, 5	3	10	30	µA	$V_{IN} = V_{BAT}$
	I_{PDIO1}	12	20	—	80	µA	$V_{IN} = V_{BAT}$
	I_{PDIO2}	12	—	—	140	µA	V_{IN} = 15V
Output Voltage Low	V_{OL1}	13, 14	—	—	500	mV	I_{OL} = 16 mA, V_{BST} = 9V
	V_{OL2}	8	—	—	300		I_{OL} = 10 mA, V_{BST} = 9V
	V_{OL3}	9	—	—			I_{OL} = 10 mA, V_{BST} = 3.6V
Output High Voltage	V_{OH1}	13, 14	8.5	—	—	V	I_{OL} = 16 mA, V_{BST} = 9V

Note 1: Wherever a specific V_{VBST} value is listed under test conditions, the VBST is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guard-banded limits.

4: Not production tested.

DC Electrical Characteristics (Continued)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = 0°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** to **Note 4**).

Parameters	Symbol	Test Pins	Min.	Typ.	Max.	Units	Conditions
Output Current	I_{IOH1}	12	-4	-5	—	mA	Alarm, V_{IO} = 3V or V_{IO} = 0V, V_{BST} = 9V
	I_{IODMP}		5	15	—		At Conclusion of Local Alarm or Test, V_{IO} = 1V
	I_{IRED50}	2	45	50	55		IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (50 mA option selected; T_A = +25°C)
	$I_{IRED100}$		90	100	110		IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (100 mA option selected; T_A = +25°C)
	$I_{IRED150}$		135	150	165		IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (150 mA option selected; T_A = +25°C)
	$I_{IRED200}$		180	200	220		IRED on, V_{IRED} = 1V, V_{BST} = 5V, IRCAP = 5V, (200 mA option selected; T_A = +25°C)
IRED Current Temperature Coefficient	T_{CIRED}	—	—	0.5	—	%/°C	VBST = 5V, IRCAP = 5V (**Note 4**)
Low Battery Alarm Voltage	V_{LB1}	3	2.05	2.1	2.15	V	Falling edge; 2.1V nominal selected
	V_{LB2}		2.15	2.2	2.25		Falling edge; 2.2V nominal selected
	V_{LB3}		2.25	2.3	2.35		Falling edge; 2.3V nominal selected
	V_{LB4}		2.35	2.4	2.45		Falling edge; 2.4V nominal selected
	V_{LB5}		2.45	2.5	2.55		Falling edge; 2.5V nominal selected
	V_{LB6}		2.55	2.6	2.65		Falling edge; 2.6V nominal selected
	V_{LB7}		2.65	2.7	2.75		Falling edge; 2.7V nominal selected
	V_{LB8}		2.75	2.8	2.85		Falling edge; 2.8V nominal selected
Low Battery Hysteresis	V_{LBHYST}	3	—	100	—	mV	
IRCAP Turn On Voltage	V_{TIR1}	11	3.6	4	4.4	V	Falling edge; V_{BST} = 5V; I_{OUT} = 20 mA
IRCAP Turn Off Voltage	V_{TIR2}	11	4	4.4	4.8	V	Rising edge; V_{BST} = 5V; I_{OUT} = 20 mA

Note 1: Wherever a specific V_{VBST} value is listed under test conditions, the VBST is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guard-banded limits.

4: Not production tested.

AC Electrical Characteristics

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = 0°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** to **Note 4**).

Parameters	Symbol	Test Pins	Min.	Typ.	Max.	Units	Conditions
Time Base							
Internal Clock Period	T_{PCLK}	—	9.8	10.4	11	ms	PROGSET, IO = high
RLED Indicator							
On Time	T_{ON1}	8	9.8	10.4	11	ms	Operating
Standby Period	T_{PLED1}		320	344	368	s	Standby, no Alarm
Local Alarm Period	T_{PLED2A}		0.94	1	1.06	s	Local Alarm condition with temporal horn pattern
	T_{PLED2B}		625	667	710	ms	Local Alarm condition with continuous horn pattern
Hush Timer period	T_{PLED4}		10	10.7	11.4	s	Timer Mode, no Local Alarm
External Alarm Period	T_{PLED0}		LED IS NOT ON			s	Remote Alarm only
GLED Indicator							
Latched Alarm Period	T_{PLED3}	9	40	43	46	s	Latched Alarm condition, LED enabled
Latched Alarm Pulse Train (3x) off Time	T_{OFLED}		1.25	1.33	1.41	s	
Latched Alarm LED Enabled Duration	T_{LALED}		22.4	23.9	25.3	Hours	
Smoke Check							
Smoke Check Duration	T_{PUL}	2	2.82	3	3.18	ms	Standby
Smoke Check Period with Temporal Horn Pattern	T_{PER0}		10	10.7	11.4	s	Standby, no Alarm
	T_{PER1A}		1.88	2	2.12	s	Standby, after one valid smoke sample
	T_{PER2A}		0.94	1	1.06	s	Standby, after two consecutive valid smoke samples
	T_{PER3A}		0.94	1	1.06	s	Local Alarm (three consecutive valid smoke samples)
	T_{PER4A}		235	250	265	ms	Push button test, >1 chamber detections
	T_{PER4C}		313	333	353	ms	Push button test, no chamber detections
	T_{PER5A}		7.5	8	8.5	s	In Remote Alarm

Note 1: See timing diagram for Horn Pattern (Figure 4-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested, and are based on characterization data.

5: See timing diagram for Horn Synchronization and AAL.

AC Electrical Characteristics (Continued)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = 0°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** to **Note 4**).

Parameters	Symbol	Test Pins	Min.	Typ.	Max.	Units	Conditions
Smoke Check Period with Continuous Horn pattern	T_{PER0}	2	10	10.7	11.4	s	Standby, no Alarm
	T_{PER1B}		2.5	2.7	2.9	s	Standby, after one valid smoke sample
	T_{PER2B}		1.25	1.33	1.41	s	Standby, after two consecutive valid smoke samples
	T_{PER3B}		1.25	1.33	1.41	s	Local Alarm (three consecutive valid smoke samples)
	T_{PER4B}		313	333	353	ms	Push button test
	T_{PER5B}		10	10.7	11.4	s	In Remote Alarm
Chamber Test Period	T_{PCT1}		40	43	46	s	Standby, no Alarm
Long Term Drift Sample Period	T_{LTD}		400	430	460	s	Standby, no Alarm, LTD enabled
Hush Timer Operation							
Hush Timer Period	T_{TPER}	—	480	516	546	s	No Alarm
Low Battery							
Low Battery Sample Period	T_{PLB1}	3	320	344	368	s	RLED on
	T_{PLB2}		80	86	92		RLED off
Horn Operation							
Low Battery Horn Period	T_{HPER1}	13	40	43	46	s	Low battery, no Alarm
Chamber Fail Horn Period	T_{HPER2}		40	43	46	s	Chamber failure
Low Battery Horn On Time	T_{HON1}		9.8	10.4	11	ms	Low battery, no Alarm
Chamber Fail Horn On Time	T_{HON2}		9.8	10.4	11	ms	Chamber Failure
Chamber Fail Horn Off Time	T_{HOF1}		305	325	345	ms	Failed Chamber, no Alarm, 3x chirp option
Alarm On Time with Temporal Horn Pattern	T_{HON2A}		470	500	530	ms	Local or Remote Alarm (**Note 1**)
Alarm Off Time with Temporal Horn Pattern	T_{HOF2A}		470	500	530	ms	Local or Remote Alarm (**Note 1**)
	T_{HOF3A}		1.4	1.5	1.6	s	Local or Remote Alarm (**Note 1**)
Alarm On time with Continuous Horn Pattern	T_{HON2B}		235	250	265	ms	Local or Remote Alarm (**Note 1**)
Alarm Off Time with Continuous Horn Pattern	T_{HOF2B}		78	83	88	ms	Local or Remote Alarm (**Note 1**)
Push-to-Test Alarm Memory On Time	T_{HON4}		9.8	10.4	11	ms	Alarm memory active, Push-to-Test
Push-to-Test Alarm Memory Horn Period	T_{HPER4}		235	250	265	ms	Alarm memory active, Push-to-Test

Note 1: See timing diagram for Horn Pattern (Figure 4-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested, and are based on characterization data.

5: See timing diagram for Horn Synchronization and AAL.

AC Electrical Characteristics (Continued)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = 0°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** to **Note 4**).

Parameters	Symbol	Test Pins	Min.	Typ.	Max.	Units	Conditions
CO Alarm Period	T_{HPER5}	7, 8	5.5	5.8	6.1	s	CO Alarm horn period
CO Alarm On Time	T_{HON5}		95	100	105	ms	CO Alarm
CO Alarm Off Time	T_{HOF6}		95	100	105	ms	CO Alarm horn off time between pulses
	T_{HOF7}		4.8	5.1	5.4	s	CO Alarm horn off time between pulse trains
Detection							
IRED On Time	T_{IRON}	2	—	100	—	µs	Prog Bits 38, 39 = 0, 0
				200			Prog Bits 38, 39 = 1, 0
				300			Prog Bits 38, 39 = 0, 1
				400			Prog Bits 38, 39 = 1, 1
Interconnect Signal Operation (IO)							
IO Active Delay	T_{IODLY1}	12	3.5	3.7	3.9	s	From start of Local Alarm to IO active
Remote Alarm Delay with Temporal Horn Pattern	$T_{IODLY2A}$		0.77	0.81	0.86	s	No Local Alarm, from IO active to alarm
Remote Alarm Delay with Continuous Horn Pattern	$T_{IODLY2B}$		0.29	0.31	0.34	s	No Local Alarm, from io active to alarm
IO Filter	T_{IOFILT}		—	—	290	ms	IO pulse width filtered
IO Pulse On Time for CO Alarm	T_{IOPW1}		23	—	290	ms	No Local Alarm, 2 valid pulses required for CO
IO Pulse Off Time for CO Alarm	T_{IOTO1}		—	—	5.4	s	IO = low
IO Charge Dump Duration	T_{IODMP}		0.475	0.5	0.525	s	At conclusion of local alarm or test
Horn Synchronization							
IO Pulse Period	T_{PIO1}	2	3.8	4	4.2	s	Local Alarm, temporal horn pattern, SyncEn = 1 (**Note 5**)
IO Pulse On Time	T_{ONIO}		3.41	3.59	3.77	s	Local Alarm, temporal horn pattern, HS = 1
Horn Sync IO Dump	T_{IODMP2}		95	100	105	ms	Local Alarm, HS = 1, IO dump active
Horn Sync IO Dump Delay	T_{IODLY4}		285	300	315	ms	Local Alarm, HS = 1
Horn Sync Contention Window	T_{IOCW}		294	310	326	ms	Local Alarm, HS = 1, IO = 0, no IO dump, IO pull-down

Note 1: See timing diagram for Horn Pattern (Figure 4-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested, and are based on characterization data.

5: See timing diagram for Horn Synchronization and AAL.

AC Electrical Characteristics (Continued)

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = 0°C to +60°C, V_{BAT} = 3V, V_{BST} = 4.2V, **Typical Application** (unless otherwise noted) (**Note 1** to **Note 4**).

Parameters	Symbol	Test Pins	Min.	Typ.	Max.	Units	Conditions
Auto Alarm Locate (AAL)							
IO Cycle Period	T_{PIO2}	2	15.2	16	16.8	s	Local Alarm, temporal horn pattern, HS = 1, AAL = 1
IO Cycle Off Time	T_{OFIO}		4.19	4.41	4.63		Local Alarm, temporal horn pattern, HS = 1, AAL = 1, IO off time between IO pulse trains (3x)

Note 1: See timing diagram for Horn Pattern (Figure 4-2).

2: T_{PCLK} and T_{IRON} are 100% production tested. All other AC parameters are verified by functional testing.

3: Typical values are for design information only.

4: Limits over the specified temperature range are not production tested, and are based on characterization data.

5: See timing diagram for Horn Synchronization and AAL.

Temperature Characteristics

Electrical Specifications: All limits specified for V_{BAT} = 3V, V_{BST} = 4.2V and V_{SS} = 0V, except where noted in the Electrical Characteristics.

Parameters	Symbol	Min.	Typ.	Max.	Units	Coditions
Temperature Ranges						
Operating Temperature Range	T_A	0	—	+60	°C	
Storage Temperature Range	T_{STG}	-55	—	+125	°C	
Thermal Package Resistances						
Thermal Resistance, 16L-SOIC (150 mil.)	θ_{JA}	—	86.1	—	°C/W	

NOTES:

2.0 PIN DESCRIPTIONS

TABLE 2-1: PIN FUNCTION TABLE

Pins	Symbol	Function
1	VSS	Connect to the negative supply voltage.
2	IRED	Provides a regulated and programmable pulsed current for the infrared emitter diode.
3	VBAT	Connect to the positive supply or battery voltage.
4	TEST	This input is used to invoke Test modes and the Timer mode. This input has an internal pull-down.
5	TEST2	Test input for Test and Programming modes. This input has an internal pull-down.
6	IRP	Connect to the anode of the photo diode.
7	IRN	Connect to the cathode of the photo diode.
8	RLED	Open drain NMOS output, used to drive a visible LED. This pin provides load current for the low battery test, and is a visual indicator for Alarm and Hush modes.
9	GLED	Open drain NMOS output used to drive a visible LED to provide visual indication of an Alarm Memory condition.
10	FEED	Usually connected to the feedback electrode through a current limiting resistor. If not used, this pin must be connected to VBAT or VSS.
11	IRCAP	Used to charge and monitor the IRED capacitor.
12	IO	This bidirectional pin provides the capability to interconnect multiple detectors in a single system. This pin has an internal pull-down device and a charge dump device.
13	HB	This pin is connected to the metal electrode of a piezoelectric transducer.
14	HS	This pin is a complementary output to HB, connected to the ceramic electrode of the piezoelectric transducer.
15	VBST	Boosted voltage produced by DC-DC converter.
16	LX	Open drain NMOS output, used to drive the boost converter inductor. The inductor should be connected from this pin to the positive supply through a low resistance path.

NOTES:

3.0 DEVICE DESCRIPTION

3.1 Standard Internal Timing

The internal oscillator is trimmed to ±6% tolerance. In standby operation the boost regulator is powered on once every 10 seconds, the IRCAP is charged from VBST and then the detection circuitry is active for 3 ms. Prior to completion of the 3 ms period, the infrared LED, IRED, is active for a user-programmable duration of 100-400 µs. During this IRED pulse, the photo diode current is integrated and then digitized. The result is compared to a limit value stored in EEPROM during calibration to determine the photo chamber status. If a smoke condition is present, the period to the next detection decreases, and additional checks are made.

3.2 Smoke Detection Circuit

The smoke detection circuitry consists of an IRED driver and an integrating photo amplifier with gain. The output of the photo amp is digitized by a 6-bit ADC. A smoke check consists of two integrations, one with the IRED off and one with the IRED on. The integration with the IRED off allows light leakage, leakage current and offset effects to be measured. This digitized result is subtracted from the result with the IRED on to produce the final digitized result. The digitized result is compared to the stored alarm limit at the conclusion of the smoke check.

When the digitized result is greater than or equal to the alarm limit, a smoke detection occurs. Three consecutive smoke detections will cause the device to go into Local Alarm and activate the horn and interconnect circuits. The RLED will turn on for 10 ms at a 1 Hz rate in Local Alarm. Once in Local Alarm, the alarm limit is changed to the hysteresis alarm limit. In Local Alarm, the boost regulator operates in High Boost mode, which provides consistent audibility of the horn over battery life.

The IRED driver is all internal and both the IRED on time and the IRED current are user programmable. The IRED on time and the photo amp integration period are the same.

The integrating photo amp has three separate gain settings:

- Normal Gain for Standby and Hysteresis Operation.
- Low Gain for Hush Operation.
- High Gain for Chamber Test and Push-to-Test Operation.

There are four separate sets of alarm limits which are user programmable:

- Normal Alarm Limit
- Hysteresis Alarm Limit
- Hush Alarm Limit
- Chamber Test Alarm Limit

3.3 Battery Test

Once every 86 seconds, the status of the battery voltage is checked by enabling the boost converter for 10 ms and comparing a fraction of the VDD voltage to an internal reference. In each period of 344 seconds, the battery voltage is checked four times. Three checks are unloaded and one check is performed with the RLED enabled, which provides a battery load. The High Boost mode is active only for the loaded low battery test. If the low battery test fails, the horn will pulse on for 10 ms every 43 seconds and will continue to pulse until the failing condition passes.

As an option, a Low Battery Hush mode can be invoked. If a Low Battery condition exists and the TEST input is driven high, the RLED will turn on. If the TEST input is held for more than 0.5 seconds, the unit will enter the Push-To-Test operation (see **Section 3.5 "Push-To-Test"**). After the TEST input is driven low, the unit enters Low Battery Hush mode and the 10 ms horn pulse is silenced for 8 hours. At the end of the 8 hours, the audible indication will resume if the low battery condition still exists. The activation of the test button will also initiate the 9-minute Hush mode (see **Section 3.6 "Hush Operation"**).

3.4 Chamber Test

Once every 43 seconds a chamber test is activated. A check of the photo chamber is made by amplifying the background reflections of the chamber. In chamber test, the normal gain is doubled and the chamber test alarm limit is used for the alarm limit. If the signal level exceeds the chamber test alarm limit, the chamber test passes. If two consecutive chamber tests fail, the horn will pulse on for 10 ms three times with a pulse separation of 330 ms and a 43 second period. The three-pulse sequence will continue until the failing condition passes. The boost regulator operates in low boost mode for the chamber test.

The chamber test and battery test audible indicators are separated by approximately 20 seconds.

3.5 Push-To-Test

Push-To-Test (PTT) occurs when the TEST input pin is driven high (V_{IH}). The smoke detection rate increases to once every 250 ms after one internal clock cycle. A check of the photo chamber is made by amplifying the background reflections of the chamber. In Push-To-Test, the normal gain is doubled and the chamber test alarm limit is used for the alarm limit. After the required three consecutive smoke detections, the device will go into a Local Alarm condition. When the TEST input is driven low (V_{IL}), the photo amplifier normal gain and normal alarm limit are selected, after one clock cycle. The detection rate continues once every 250 ms until three consecutive No Smoke conditions are detected. At this point, the device returns to standby timing. In addition, after the TEST input goes low, the device enters the Hush mode (see **Section 3.6 "Hush Operation"**).

3.6 Hush Operation

When Hush mode is started, the unit is immediately reset out of Local Alarm and the horn is silenced. In Hush mode, the photo amp gain is reduced to one half the normal gain setting to lower the unit's sensitivity. In addition, there is a separate user-selectable hush alarm level which sets the Local Alarm condition in hush. When a High Local Smoke condition exceeds the hush alarm level, the unit can be placed into a Local Alarm condition. The RLED is turned on for 10ms every 10s to indicate the unit is in Hush mode. The Hush mode period is 9 minutes. After this period times out, the unit goes back to its standby operation.

If the unit is currently in Hush mode, then PTT will test the unit with the chamber test gain and alarm limits. Upon release of PTT, a new Hush mode will be initiated.

Four user-selectable options control hush operation.

The first option allows the hush function to be disabled.

The Hush-In-Alarm-Only option allows the unit to enter hush operation only for a Local Alarm condition when the TEST input goes low. The unit is immediately reset out of alarm and the horn is silenced. If the Hush-In-Alarm-Only option is not selected, then anytime a release of PTT occurs the Hush mode is initiated. This is Hush-On-Demand.

The Smart Hush option allows Hush mode to be terminated early. Hush mode can be canceled by a high local smoke alarm, a remote smoke alarm or PTT. A high local smoke alarm is the local smoke alarm caused by a smoke level which exceeds the hush alarm level.

Hush with no alarm is another user selectable option. This option allows the local alarm to be canceled with the PTT, but a high local smoke condition will not place the unit into a Local Alarm condition.

3.7 Long-Term Drift Adjustment

As an option, a Long-Term Drift (LTD) Adjustment for the photo chamber can be enabled. If this option is selected during calibration, a normal no-smoke baseline integration measurement must be made using Test mode T8. This value is stored in EEPROM. During normal operation, a new baseline value is calculated by making 64 integration measurements over a period of 8 hours. The measurements are averaged, and the averaged value is used to calculate the long-term drift adjustment.

The long-term drift adjustment is calculated by subtracting the original baseline long-term drift value from the averaged long-term drift value. The long-term drift adjustment is scaled for the operating mode and added to the alarm limits stored in EEPROM during calibration. The new alarm limits are not stored in EEPROM. The LTD adjustment only affects the normal, hysteresis, and hush alarm limits. The chamber test limit is not changed by the LTD adjustment.

Long term drift sampling is suspended during the Hush, Local Alarm, or Remote Alarm conditions. Any long-term drift values being saved for a new long-term drift average calculation are discarded when long-term drift sampling is suspended. The long-term drift sampling is restarted after the Hush, Local Alarm, or Remote Alarm condition has ended.

In order to limit the amount of change the long-term drift adjustment can make, a normal alarm limit maximum value, NAM[5:0], must be set. The NAM[5:0] value must be larger than the normal alarm limit value. When the LTD adjustment to the normal alarm limit is equal to or greater than the NAM[5:0] value, the chamber failure triple-horn chirp is sounded.

3.8 Alarm Memory

The Alarm Memory feature allows easy identification of any unit that had previously been in a Local Alarm condition. The Local Alarm memory feature is user-programmable.

When a detector exits a Local Alarm condition, the Alarm Memory latch is set. The GLED can be used to visually identify any unit that had previously been in a Local Alarm condition. The GLED flashes three times. The duration of the flash is 10 ms. Each flash is separated by 1.3s from the next flash. This pattern will repeat every 43 seconds. In order to preserve battery power; this visual indication will stop after a period of 24 hours.

The user will still be able to identify a unit with an active alarm memory by pressing the Push-to-Test button. When this button is active, the horn will pulse on for 10 ms every 250 ms.

If the Alarm Memory condition is set, then any time the Push-to-Test button is pressed and released, the Alarm Memory latch is reset.

The initial 24-hour visual indication is not displayed if a low battery condition exists.

3.9 Interconnect Operation

The bidirectional IO pin allows the interconnection of multiple detectors. In a Local Alarm condition, this pin is driven high immediately through a constant current source that is biased by the boost regulator, VBST, operating in High Boost mode (see **Section 3.13 "Boost Regulator"**). Shorting this output to ground will not cause excessive current. The IO is ignored as an input during a Local Alarm.

The IO pin also has an NMOS discharge device that is active for 1.3 seconds after the conclusion of any type of Local Alarm. This device helps to quickly discharge any capacitance associated with the interconnect line.

If a remote, active-high signal is detected, the device goes into Remote Alarm and the horn will be active. RLED will be off, indicating a Remote Alarm condition. Internal protection circuitry allows the signaling unit to have a higher supply voltage than the signaled unit, without excessive current draw.

The interconnect input has a 336 ms nominal digital filter. This allows the interconnection to other types of alarms (carbon monoxide, for example) that may have a pulsed interconnect signal.

As a user programmable option, the smart interconnect (smart IO) function can be selected. If the IO input is pulsed high twice with a nominal pulse on time greater than 23ms and with a period of less than 5.4s, a CO Alarm condition is detected, and the CO temporal horn pattern will sound. The CO temporal pattern will sound at least two times if a CO alarm condition is detected.

3.10 Horn Pattern

The smoke alarm horn pattern can be either a temporal horn pattern or a continuous horn pattern, depending on user selection. The temporal horn pattern supports the NFPA 72 emergency evacuation signal. The continuous horn pattern is a 70% duty cycle continuous horn pattern.

If a CO alarm is detected through the IO, the unit will sound the CO horn pattern. The CO horn pattern consists of 4 chirps every 5.8s. Each chirp is 100 ms long and the chirps are separated by 100 ms.

The RLED will not turn on when the horn is sounding.

3.11 Horn Synchronization

The horn synchronization function is a user programmable function.

In an interconnected system, if one unit goes into Local Alarm then other units will go into Remote Alarm. The IO line is driven high by the originating local smoke unit and stays high during the alarm.

If the horn synchronization function is enabled, then at the end of every temporal horn pattern and when the horn is off, the origination unit will drive IO low, then high again. This periodic IO pulsing high and low will cause the remote smoke units to go into and out of Remote Alarm repeatedly. Each time when a unit goes into Remote Alarm, its timing is reset. The horn pattern of all remote smoke units will be synchronized with the horn pattern of the originating unit.

A protection circuit ensures that the unit which goes into Local Alarm first will be the master unit which conducts the horn synchronization. The units which go into Local Alarm later will not drive the IO line. This avoids bus contention problem.

This function works with the temporal horn pattern only.

3.12 Auto Alarm Locate

Auto Alarm Locate (AAL) is a user-programmable function. To use AAL, horn synchronization must be selected for the temporal horn pattern. AAL may be used with either the temporal or the continuous horn pattern.

The purpose of AAL is to let users quickly find the local alarm units just by listening. The local alarm units will sound the horn pattern without interruption. The remote alarm units will sound the pattern with an interruption. Every 16s the remote units are silenced for 4.7s.

The originating unit conducts the IO cycling. For the temporal horn pattern, every fourth temporal pattern the IO is driven low for one temporal pattern. In the remaining three temporal patterns, IO is still pulsing to keep the horn synchronized. For continuous horn patterns the IO sends no synchronization pulse but drives IO low for 4.4s to produce a 4.7s silence on remote alarms.

The RLED of the origination unit and other units in local alarm will be turned on for 10 ms every 1s. RLED of remote smoke units will be off.

3.13 Boost Regulator

The RE46C194 uses a boost regulator to provide a regulated voltage of 3.6V in Standby operation. This provides consistent operation during Low Battery conditions. During a Local Alarm, Remote Alarm, PTT or Battery Test, the boost regulator operates in High Boost mode. This high boost voltage insures the horn achieves the correct sound pressure level and the IO signal is compatible with products that operate from 9V. The high boost voltage is user selectable and may be set to 8.5V or 10.0V.

The boost regulator uses an adjustable minimum off time hysteretic architecture with current mode control. The peak inductor current is 0.6A with a minimum fixed off time of 1.6 µs.

The boost regulator uses soft start when switching from Low Boost to High Boost operation to limit inrush current. The inrush current is the result of charging the boost capacitor from the low boost voltage to the high boost voltage. Once the high boost voltage is reached the boost regulator only has to provide the load current. Limiting the boost voltage ramp rate controls the magnitude of the inrush current.

During soft start the effective charging current will be about 12 mA. This corresponds to a maximum boost voltage ramp rate of 2 ms for a boost voltage of 8.5V. RLED will not turn on during boost regulator soft start.

4.0 USER PROGRAMMING AND TEST MODES

User programming and test modes provide the means to configure the RE46C194 for a particular application and evaluate the smoke detector's performance. Parametric programming allows the photo amp gain and integration time along with the IRED current and low battery voltage to be selected. Table 4-1 lists the parametric characteristics that can be selected for the application. The typical full-scale photodiode current that a particular combination of photo amp gain and integration time can accommodate is included in the table. Only one gain factor, GF, and one integration time can be used for the smoke detector.

TABLE 4-1: PARAMETRIC PROGRAMMING

Parametric Programming		**Range**		**Resolution**	
IRED Period		100 µs to 400 µs		100 µs	
IRED Current Sink		50 mA to 200 mA		50 mA	
Low Battery Detection Voltage		2.1V to 2.8V		100 mV	
Photo Detection Limits		**Typical Full-Scale Photodiode Input Current (nA).**			
Gain		**Integration Time**			
		100 µs	**200 µs**	**300 µs**	**400 µs**
Normal Gain	GF = 1	58	29	19.4	14.5
	GF = 2	29	14.5	9.6	7.2
	GF = 3	14.5	7.2	4.8	3.6
	GF = 4	7.2	3.6	2.4	1.8
Hush Gain	GF = 1	116	58	38.8	29
	GF = 2	58	29	19.4	14.5
	GF = 3	29	14.5	9.6	7.2
	GF = 4	14.5	7.2	4.8	3.6
Chamber Test Gain	GF = 1	29	14.5	9.6	7.2
	GF = 2	14.5	7.2	4.8	3.6
	GF = 3	7.2	3.6	2.4	1.8
	GF = 4	3.6	1.8	1.2	0.9

Note 1: GF is the user-selectable Photo Integration Gain Factor. Once selected, it applies to all modes of operation. For example, if GF = 1 and integration time is selected to be 100 µs, the ranges will be as follows: Normal/Hysteresis = 58 nA, Hush = 116 nA, Chamber Test = 29 nA.

2: Nominal measurement resolution in each case will be 1/63 of the maximum input range.

3: The same current resolution and ranges applies to the limits.

In addition to the parametric setup of the smoke detector, different features can be selected to customize the device for a particular application. The features are described in Table 4-2.

TABLE 4-2: FEATURES PROGRAMMING

Feature	Options
Long-Term Drift Adjustment	Enable/Disable
Low Battery Hush	Enable/Disable
Hush	Enable/Disable
Hush in Alarm Only versus Hush on demand	Enable/Disable
Hush with No Alarm (for Europe)	Enable/Disable
Smart Hush (Cancel Hush for High Smoke, Remote Alarm, PTT)	Enable/Disable
Alarm Memory	Enable/Disable
Smart IO with CO Alarm Sensing	Enable/Disable
Horn Pattern	Temporal/Continuous
Horn Synchronization	Enable/Disable
Auto Alarm Locate	Enable/Disable
Boost Voltage	8.5V or 10V

4.1 Calibration and Programming Procedures

Fourteen separate programming and test modes are available for user customization of the RE46C194. To enter these modes after power-up, TEST2 must be driven to VBAT and held at that level. The TEST input is then clocked to step through the test modes. The TEST input has two logic high conditions. FEED and IO are reconfigured to become test mode inputs, while RLED, GLED and HB become test mode outputs. The test mode functions for each pin are outlined in Table 4-3.

When TEST2 is held at VBAT, TEST becomes a tri-state input with nominal input levels at VSS, VBAT and VBST. A test clock occurs whenever the TEST input switches between VSS and VBST. The TEST Data column represents the state of TEST when used as a data input, which would be either VSS or VBAT. The TEST pin can therefore be used as both a clock, to change modes and as a data input, once a mode is set. Other pin functions are described in Table 4-3.

The 6-bit ADC used to digitize the integrator output is composed of a counter, a DAC, and a comparator. The comparator output is available on the HB output for certain test modes and is designated as SmkComp in Table 4-3. The DAC output is available in certain test modes on the RLED pin and is designated as DAC in Table 4-3.

TABLE 4-3: TEST MODE FUNCTIONS

Mode	Description	TEST Clock	TEST Data	TEST2	FEED	IO	RLED	GLED	HB
	VIH	VBST	VBAT	VBAT	VBST	VBAT	—	—	—
	VIL	VSS	VSS	VSS	VSS	VSS	—	—	—
T0	Horn Test	0	HornEn	VBAT	FEED	IO	RLED	GLED	HB
T1	Low Battery Test	1	not used	VBAT	FEED	LBstrb	RLED	GLED	LBout
T2	System Setup (22 bits)	2	ProgData	VBAT	ProgCLK	ProgEn	RLED	GLED	HB
T3	Norm Lim Set (6 bits)	3	not used	VBAT	CalCLK	IntLat(3)	DAC	IntegOut	SmkComp(1)
T4	Hyst Lim Set (6 bits)	4	not used	VBAT	CalCLK	IntLat(3)	DAC	IntegOut	SmkComp(1)
T5	Hush Lim Set (6 bits)	5	not used	VBAT	CalCLK	IntLat(3)	DAC	IntegOut	SmkComp(1)
T6	Ch Test Lim Set (6 bits)	6	not used	VBAT	CalCLK	IntLat(3)(4)	DAC	IntegOut	SmkComp(1)
T7	Normal Alarm Max Limit (6 bits)	7	not used	VBAT	CalCLK	IntLat(3)(4), ProgEn	DAC	IntegOut	SmkComp(1)
T8	Serial Read/Write (58 bits)	8	ProgData	VBAT	ProgCLK	ProgEn	RLED	GLED	Serial Out
T9	LTD Baseline (6 bits)	9	not used	VBAT	MeasEn	ProgEn	DAC	IntegOut	HB
T10	Norm Lim Check	10	not used	VBAT	MeasEn	not used	DAC	IntegOut	SCMP(2)
T11	Hyst Lim Check	11	not used	VBAT	MeasEn	not used	DAC	IntegOut	SCMP(2)
T12	Hush Lim Check	12	not used	VBAT	MeasEn	not used	DAC	IntegOut	SCMP(2)
T13	Ch Test Lim Check	13	not used	VBAT	MeasEn	not used	DAC	IntegOut	SCMP(2)
T14	Normal Alarm Max Limit Check	14	not used	VBAT	MeasEn	not used	DAC	IntegOut	SCMP(2)

Note 1: SmkComp (HB) - digital comparator output (high if DAC < IntegOut; low if DAC > IntegOut).

2: SCMP (HB) - digital output representing comparison of measurement value and associated limit. Signal is valid only after MeasEn has been asserted and measurement has been made. (SCMP high if measured value > limit; low if measured value < limit).

3: IntLat (IO) - digital input used for two purposes. If FEED is at a logic high level, then a low to high transition on IntLat will initiate an integration cycle. If FEED is at a logic low level, then a low to high transition on IntLat will latch the present state of the limits (DAC level) for later storage. T3-T6 limits are latched, but not stored until ProgEn is asserted in T7 mode.

4: At the end of T7 mode, in order to store the limits, the IO input must be pulsed twice consecutively with FEED held low. The first pulse will latch the data and the second will store the data in EEPROM.

The HS pin is used as an error flag when programming the RE46C194. When an Error condition exists, the HS pin will be asserted high after the program enable, ProgEn, pulse on the IO pin is driven low. The HS pin will remain high until the particular test mode is exited. The HS error flag can be asserted for test modes T7, T8, and T9.

Two possible Error conditions can cause HS to be asserted high. First, if the hysteresis alarm limit is set to a value greater than or equal to the normal alarm limit, this can cause a problem in normal operation. Second, if the normal alarm limit max is set to a value less than or equal to the normal alarm limit when LTD is enabled. In the second case, the RE46C194 can indicate a chamber fail after power up.

4.2 Horn Test

Test mode T0 allows the horn to be enabled indefinitely for audibility testing. The detailed steps are as follows:

1. Power up with bias conditions as shown in Figure 4-3 or Figure 4-5.
2. The TEST input should be driven to VBAT while TEST2 is held at VSS.
3. TEST2 pin should be driven high to VBAT to enable the horn and driven to VSS to disable the horn.

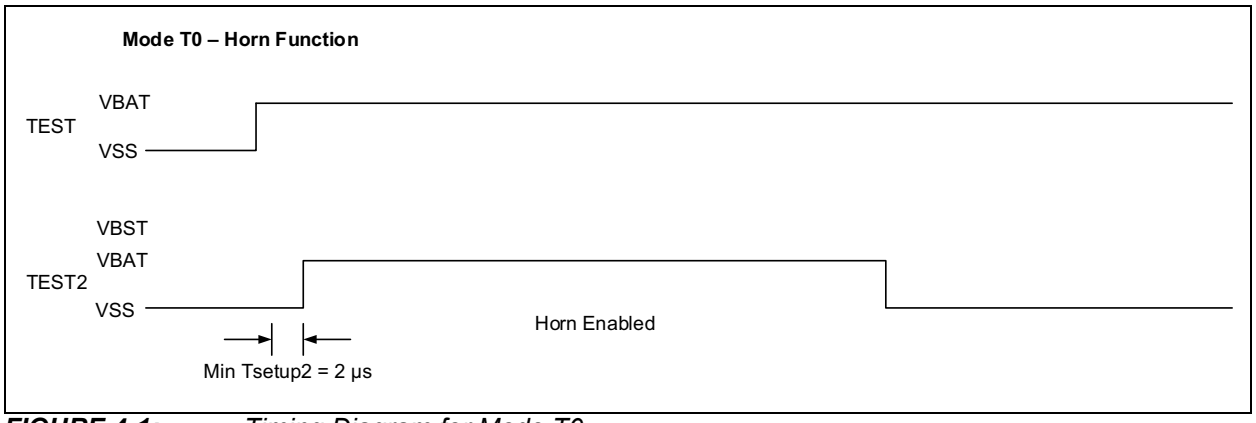


FIGURE 4-1: *Timing Diagram for Mode T0.*

4.3 Low Battery Test

This mode allows the user to enable the internal low battery circuitry to perform a low battery test. To enter this mode, follow these steps:

1. Power up with the bias conditions shown in Figure 4-3 or Figure 4-5. VBST should be connected to 5V through a diode, so VBST can enter High Boost operation.
2. Drive TEST2 input from VSS to VBAT to enter the Programming mode. TEST2 must remain high at VBAT through the following steps.
3. Apply one clock pulse to the TEST input to enter the T1 mode. The RLED and GLED will turn on.
4. Drive the IO input from VSS to VBAT. This will enable the boost converter. Monitor the HB output for the low battery comparator status.
5. Lower or increase VBAT and repeat step 4.

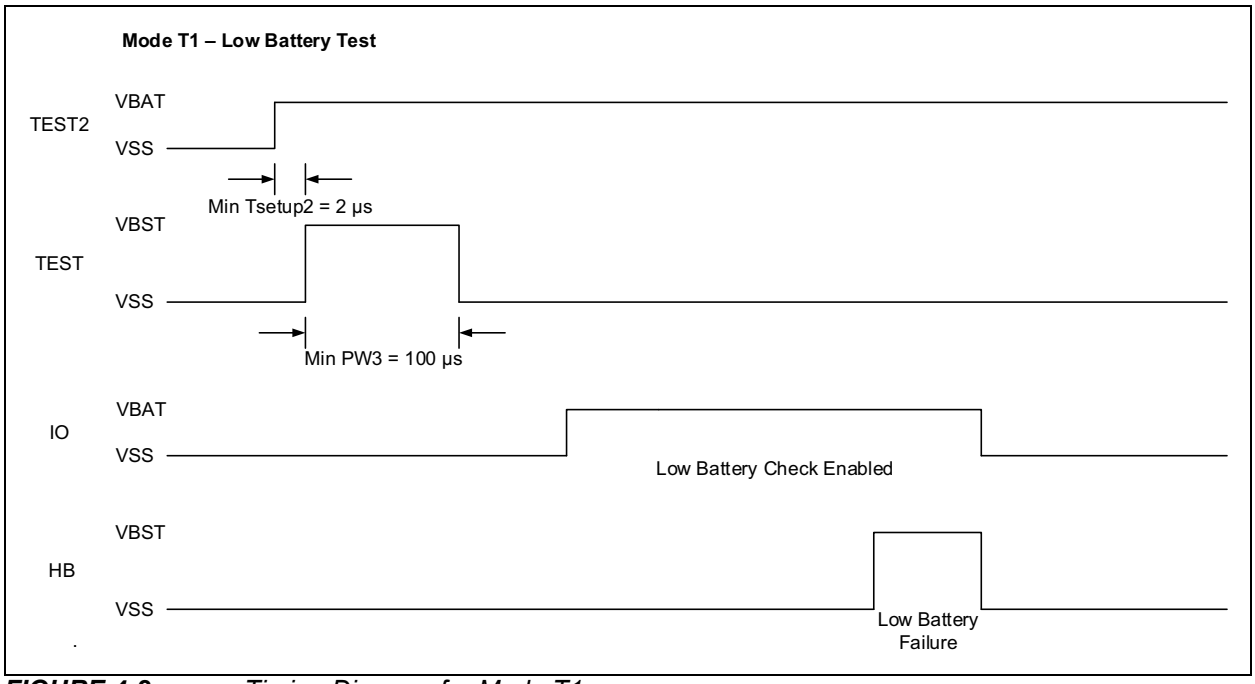


FIGURE 4-2: *Timing Diagram for Mode T1.*

4.4 System Setup

Test mode T2 allows the parametric and feature selections to be programmed into EEPROM. For test mode T2 only 22 bits (36 to 57) of Register 4-1 will be loaded. Alternatively, test mode T8 “Serial Read/Write,” allows the parametric selections, feature selections and alarm limits to be programmed into EEPROM and read back. For test mode T8, all 58 bits of Register 4-1 will be loaded. For test mode T2, 22 bits are clocked in serially using TEST as a data input and FEED as a clock input, and are then stored in EEPROM.

The System Setup steps are as follows:

1. Power up with bias conditions as shown in Figure 4-3 or Figure 4-5.
2. At power-up TEST = TEST2 = FEED = IO = VSS.
3. Drive the TEST2 input from VSS to VBAT to enter the Programming mode. TEST2 must remain high at VBAT through Step 5.
4. Using TEST as the data input and FEED as the clock, shift in the values selected from Register 4-1.
5. After shifting in the data, pulse IO high to VBAT 10 times with a 5 ms on 5 ms off cycle to store the shift register contents into EEPROM.
6. If any changes are required, drive TEST2 low to VSS and return to Step 2. All bit values must be reentered.

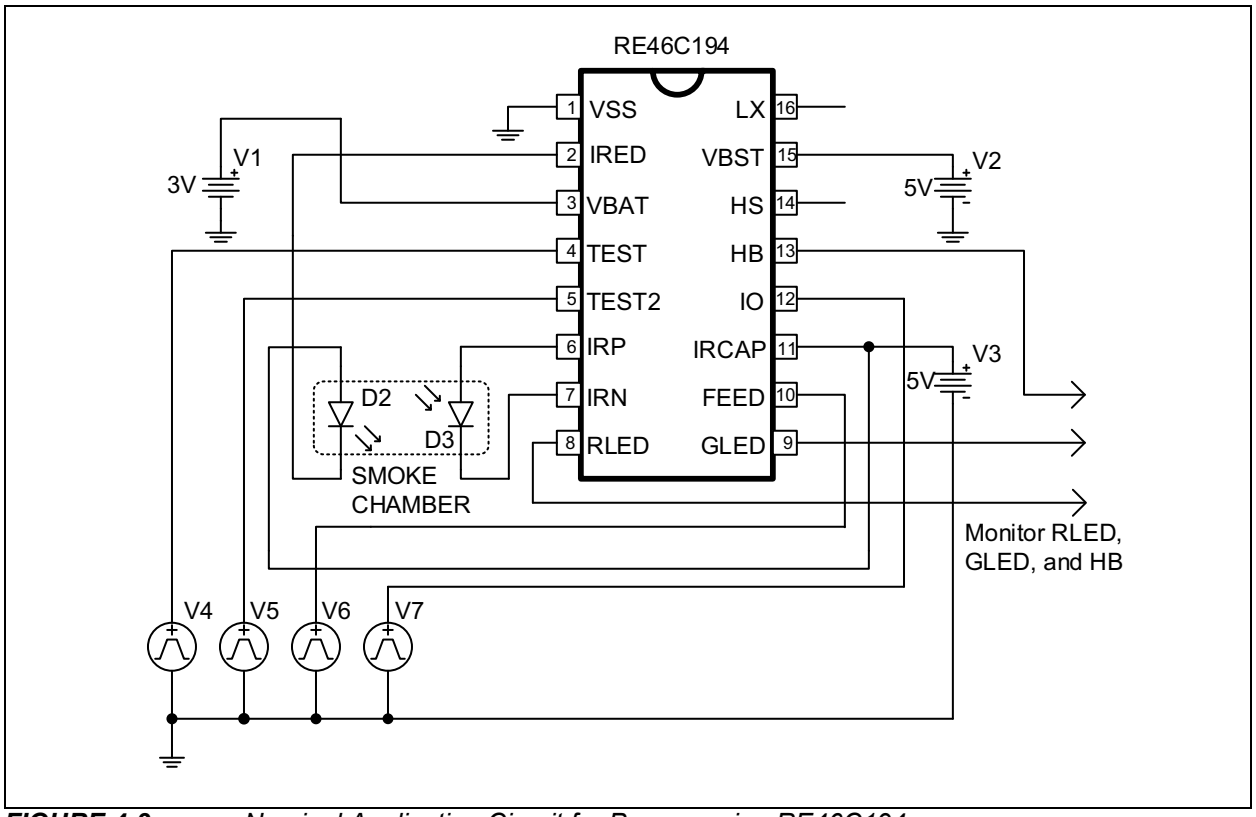


FIGURE 4-3: *Nominal Application Circuit for Programming RE46C194.*

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER

U	U	U	U	U	U	RW	RW
						FB	HBV
bit 57							

RW	RW	RW	RW	RW	RW	RW	RW
AM	AAL	HS	HP	CO	LTD	HNA	HIAO
bit 55							bit 48

RW	RW	RW	RW	RW	RW	RW	RW
SHush	Hush	LBH	LB2	LB1	LB0	IRC1	IRC0
bit 47							bit 40

RW	RW	RW	RW	RW	RW	RW	RW
IT1	IT0	GF1	GF0	NL5	NL4	NL3	NL2
bit 39							bit 32

RW	RW	RW	RW	RW	RW	RW	RW
NL1	NL0	HYL5	HYL4	HYL3	HYL2	HYL1	HYL0
bit 31							bit 24

RW	RW	RW	RW	RW	RW	RW	RW
HUL5	HUL4	HUL3	HUL2	HUL1	HUL0	CTL5	CTL4
bit 23							bit 16

RW	RW	RW	RW	RW	RW	RW	RW
CTL3	CTL2	CTL1	CTL0	NAM5	NAM4	NAM3	NAM2
bit 15							bit 8

RW	RW	RW	RW	RW	RW	RW	RW
NAM1	NAM0	LTD5	LTD4	LTD3	LTD2	LTD1	LTD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 57 **FB:** Factory Bit
Must be set to 0.

bit 56 **HBV:** High VBST Voltage
0 = 10.0V
1 = 8.5V

bit 55 **AM:** Alarm Memory
0 = Disable
1 = Enable

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER (CONTINUED)

bit 54 **AAL:** Auto Alarm Locate
0 = Disable
1 = Enable

bit 53 **HS:** Horn Synchronization
0 = Disable
1 = Enable

bit 52 **HP:** Horn Pattern
0 = Continuous Horn Pattern
1 = Temporal Horn Pattern

bit 51 **CO:** Smart IO - CO Alarm
0 = Disable
1 = Enable

bit 50 **LTD:** Long Term Drift Enable
0 = Disable
1 = Enable

bit 49 **HNA:** Hush No Alarm Option
0 = Disable (Hush with High Smoke Alarm Threshold Enabled)
1 = Enable (Hush with High Smoke Alarm Threshold Disabled)

bit 48 **HIAO:** Hush in Alarm Only Option
0 = Disable (Hush on Demand)
1 = Enable (Hush in Alarm Only)

bit 47 **SHush:** Smart Hush Option
0 = Never Cancel
1 = Canceled for high smoke level, interconnect alarm, or second push of the TEST button (as described above)

bit 46 **Hush:** Hush Option
0 = Disable
1 = Enable

bit 45 **LBH:** Low Battery Hush Enable
0 = Disable
1 = Enable

bit 44-42 **LB2, LB1, LB0[44:42]:** Low Battery Trip Point
000 = 2.1V
001 = 2.2V
010 = 2.3V
011 = 2.4V
100 = 2.5V
101 = 2.6V
110 = 2.7V
111 = 2.8V

bit 41-40 **IRC1, IRC0[41:40]:** IRED Current
00 = 50 mA
01 = 100 mA
10 = 150 mA
11 = 200 mA

bit 39-38 **IT1, IT0[39:38]:** Integration Time
00 = 100 µs
01 = 200 µs
10 = 300 µs
11 = 400 µs

REGISTER 4-1: CONFIGURATION AND CALIBRATION SETTINGS REGISTER (CONTINUED)

bit 37-36 **GF1, GF0[37:36]:** Gain Factor

00 = 1
01 = 2
10 = 3
11 = 4

bit 35-30 **NL5, NL4, NL3, NL2, NL1, NL0[35:30]:** Normal Limits (see **Section 3.2 "Smoke Detection Circuit"**)

000000 = 0
000001 = 1
...
111110 = 62
111111 = 63

bit 29-24 **HYL5, HYL4, HYL3, HYL2, HYL1, HYL0[29:24]:** Hysteresis Limits (see **Section 3.2 "Smoke Detection Circuit"**)

000000 = 0
000001 = 1
...
111110 = 62
111111 = 63

bit 23-18 **HUL5, HUL4, HUL3, HUL2, HUL1, HUL0[23:18]:** Hush Limits (see **Section 3.6 "Hush Operation"**)

000000 = 0
000001 = 1
...
111110 = 62
111111 = 63

bit 17-12 **CTL5, CTL4, CTL3, CTL2, CTL1, CTL0[17:12]:** Chamber Test Limits (see **Section 3.3 "Battery Test"**)

000000 = 0
000001 = 1
...
111110 = 62
111111 = 63

bit 11-6 **NAM5, NAM4, NAM3, NAM2, NAM1, NAM0[11:6]:** Normal Alarm Maximum Value (see **Section 3.9 "Interconnect Operation"**)

000000 = 0
000001 = 1
...
111110 = 62
111111 = 63

bit 5-0 **LTD5, LTD4, LTD3, LTD2, LTD1, LTD0[5:0]:** Long Term Drift (see **Section 3.9 "Interconnect Operation"**)

000000 = 0
000001 = 1
...
111110 = 62
111111 = 63

For the following options, the sequence to be loaded into the register is shown in Example 4-1:

- Photo Amp Gain Factor = 1
- Integration Time = 200 µs
- IRED Current = 100 mA
- Low Battery Trip = 2.2V
- Smart Hush Option = Never Cancel
- Tone Select = Temporal
- High Boost Voltage = 8.5V
- Enable:
  Low Battery Hush, Hush Option, Hush In Alarm Only, Smart IO, Alarm Memory,
- Disable:
  Long Term Drift, Horn Synchronization, Auto Alarm Locate, Smart Hush, Hush No Alarm Option

EXAMPLE 4-1:

Data	—	—	—	—	—	—	0	1
Bit #	—	—	—	—	—	—	57	56

Data	1	0	0	1	1	0	0	1
Bit #	55	54	53	52	51	50	49	48

Data	0	1	1	0	0	1	0	1
Bit #	47	46	45	44	43	42	41	40

Data	0	1	0	0	—	—	—	—
Bit #	39	38	37	36	—	—	—	—

The timing diagram for test mode T2 is shown in Figure 4-4. The minimum pulse width for FEED is 10 µs, while the minimum pulse width for TEST is 100 µs.

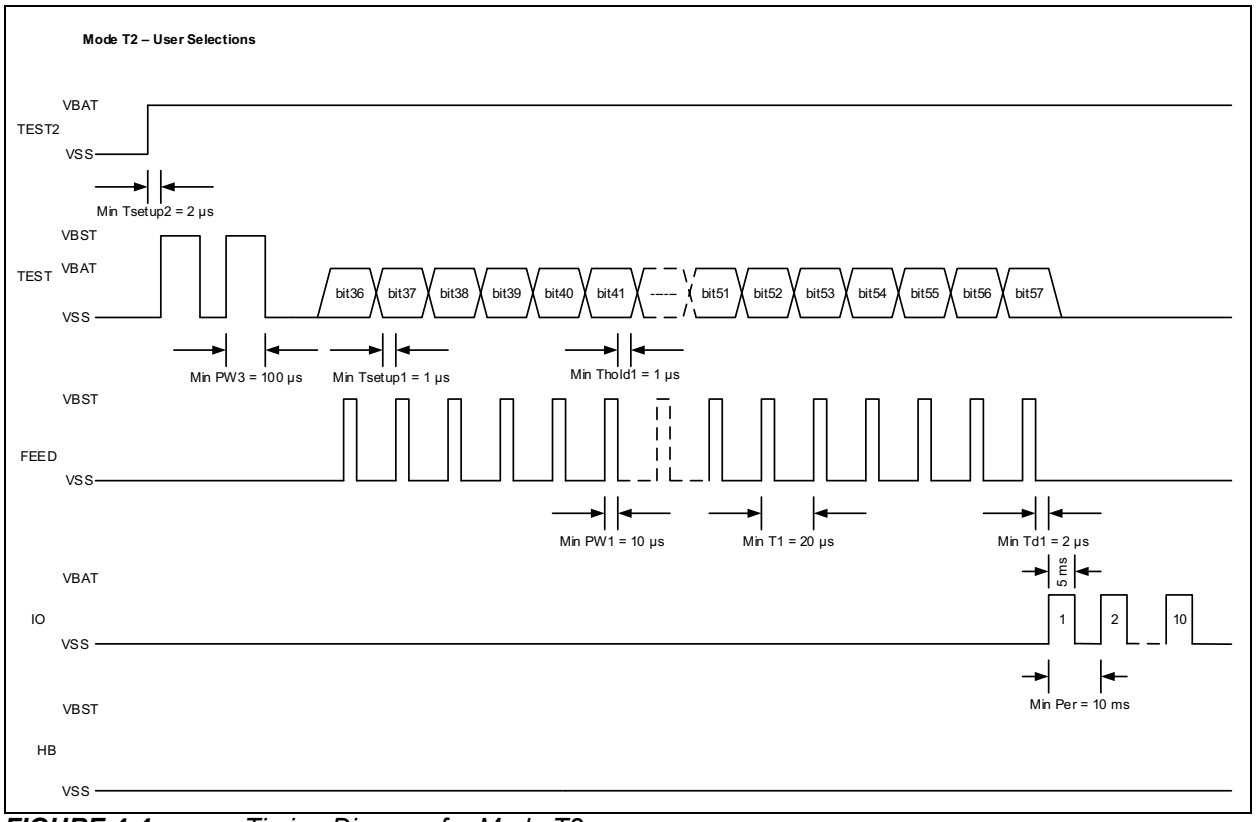


FIGURE 4-4: *Timing Diagram for Mode T2.*

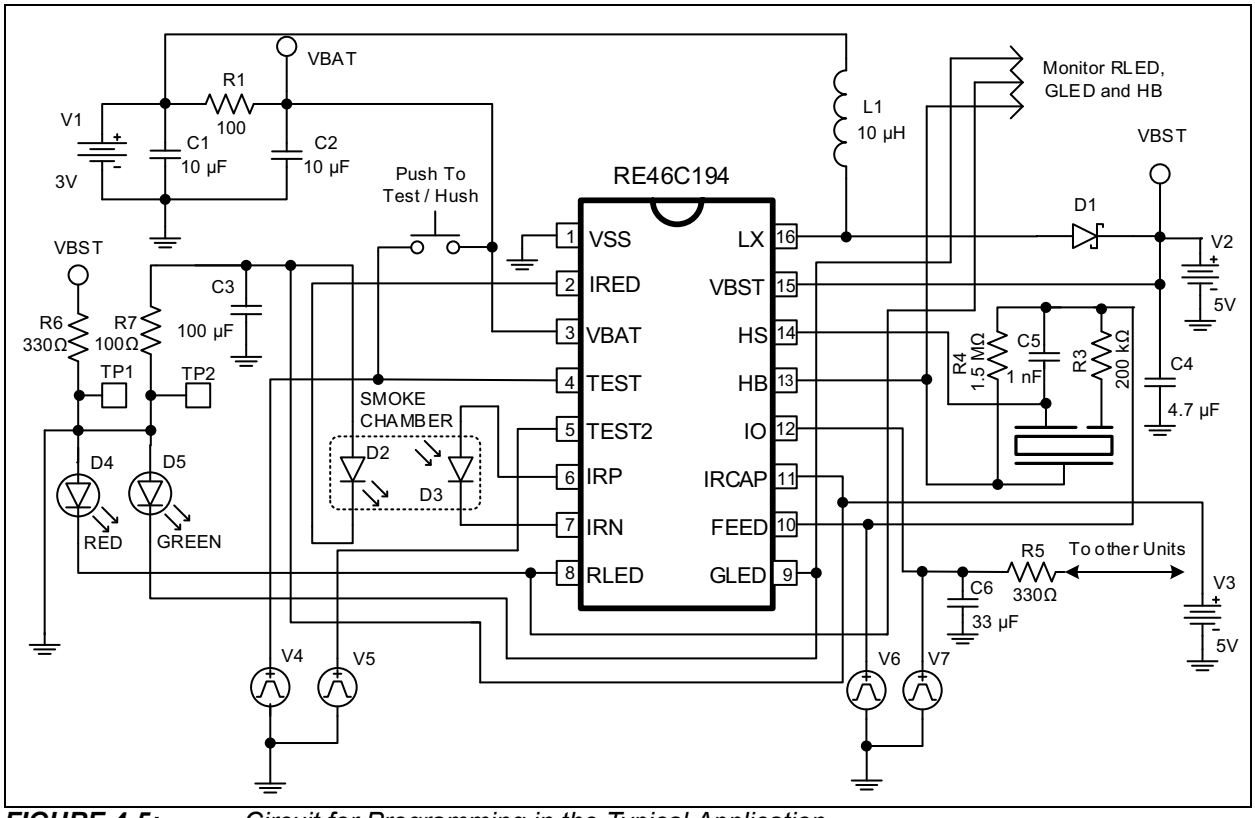


FIGURE 4-5: *Circuit for Programming in the Typical Application.*

4.5 Smoke Calibration

A separate calibration mode is entered for each measurement mode (Normal, Hysteresis, Hush, Chamber Test and Alarm Max) so that independent limits can be set for each. In all calibration modes, the integrator output can be accessed at the GLED output. The DAC output voltage, which represents the smoke detection level, can be accessed at the RLED output. The SmkComp output voltage is the result of the comparison of the DAC with the integrator output and can be accessed at HB. The FEED input can be clocked to step up the smoke detection level at RLED. Once the desired smoke threshold is reached, the IO input is pulsed from low to high to store the result.

The calibration procedure is described in the following steps:

1. Power up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive the TEST2 input from VSS to VBAT to enter the Programming mode. TEST2 must remain high at VBAT through Step 8.
3. Apply three clock pulses to the TEST input to enter T3 mode. This initiates the calibration mode for Normal Limit setting. The Integrator output will appear at GLED and the smoke detection level at RLED.
4. At this point, clock FEED to increase the smoke detection level as needed. Pulling IO high with FEED at a logic high level will initiate an integration measurement. The integrator output signal will appear at GLED. The sequence of incrementing the limit, performing an integration measurement and monitoring the HB output for the resulting comparison can be repeated until the desired threshold is reached. Once the desired smoke threshold is reached, with FEED held low, the IO input should be pulsed low to high to latch the smoke detection level.
5. Apply a clock pulse to the TEST input to enter T4 mode. This initiates the calibration mode for Hysteresis Limit. The sequence in Step 4 should be repeated to set the Hysteresis Limit.
6. Apply a clock pulse to the TEST input to enter T5 mode and initiate calibration for Hush Limit. Repeat Step 4 to set the Hush Limit.
7. Apply a clock pulse to the TEST input to enter T6 mode and initiate calibration for Chamber Test Limit. Repeat Step 4 to set the Chamber Test Limit.
8. Apply a clock pulse to the TEST input to enter T7 mode and initiate calibration for Normal Alarm Max Limit. Repeat Step 4 to set the Normal Alarm Max Limit. If LTD is not enabled, this limit set function does not have to be performed but the value must be latched as described in the next step.
9. After pulsing the IO input to latch the Normal Alarm Max Limit, the IO input must be pulsed ten times with 5 ms pulses using a 10 ms period to store the latched limits into EEPROM.
10. HS will be asserted high if the normal alarm max limit is less than or equal to the normal alarm limit or if the hysteresis alarm limit is greater than or equal to the normal alarm limit.

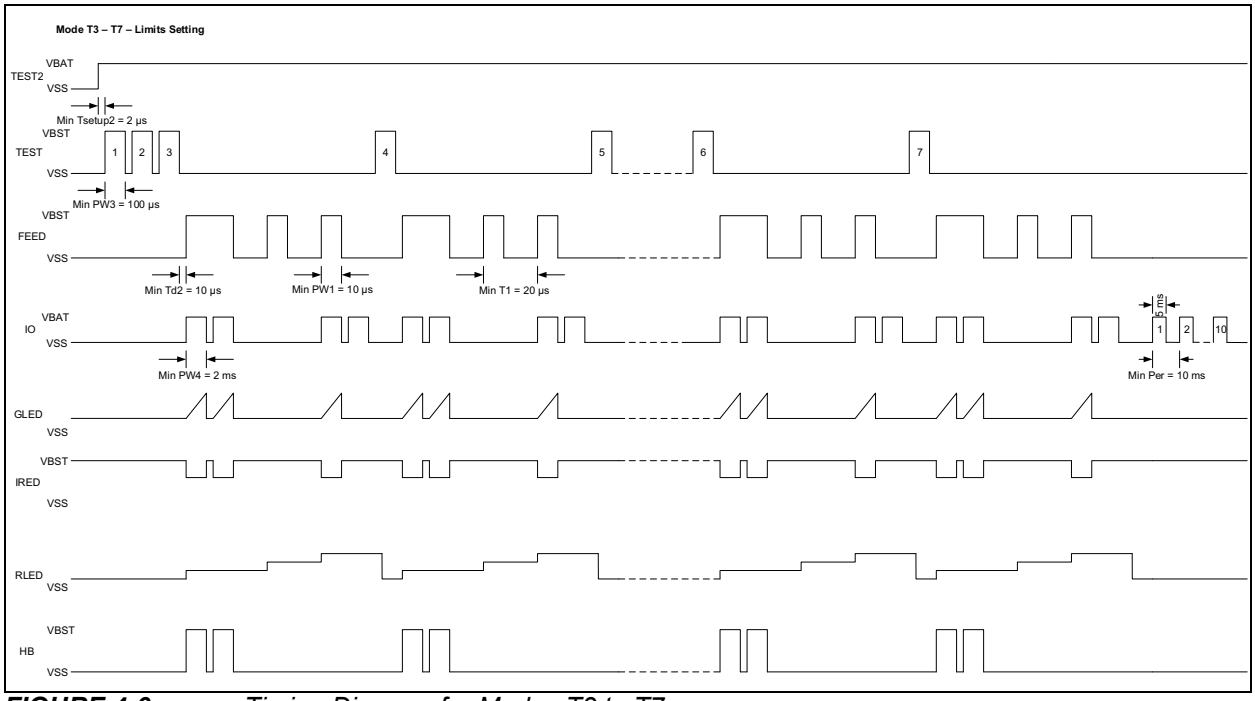


FIGURE 4-6: *Timing Diagram for Modes T3 to T7.*

4.6 Serial Read/Write

The alarm limits, LTD baseline and system setup information can be entered directly from the Serial Read/Write mode.

To enter the Serial Read/Write mode, follow these steps:

1. Power up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive TEST2 input from VSS to VBAT to enter into Programming mode. TEST2 must remain high at VBAT until all data has been entered and stored in EEPROM.
3. Pulse the TEST input 8 times to VBST to enter test mode T8. This enables the Serial Read/Write mode.
4. TEST now acts as a data input (High = VBAT, Low = VSS). FEED acts as the clock input (High = VBST, Low = VSS). Clock in the alarm limits, LTD baseline, functional and parametric options. The data sequence follows the pattern described in Register 4-1. A serial data output is available at HB.
5. After the 58 bits have been entered, pulse IO high to VBAT 10 times with a 5 ms pulse width and a 10 ms period to store the shift register contents into EEPROM.
6. HS will be asserted high if the normal alarm max limit is less than or equal to the normal alarm limit or if the hysteresis alarm limit is greater than or equal to the normal alarm limit.

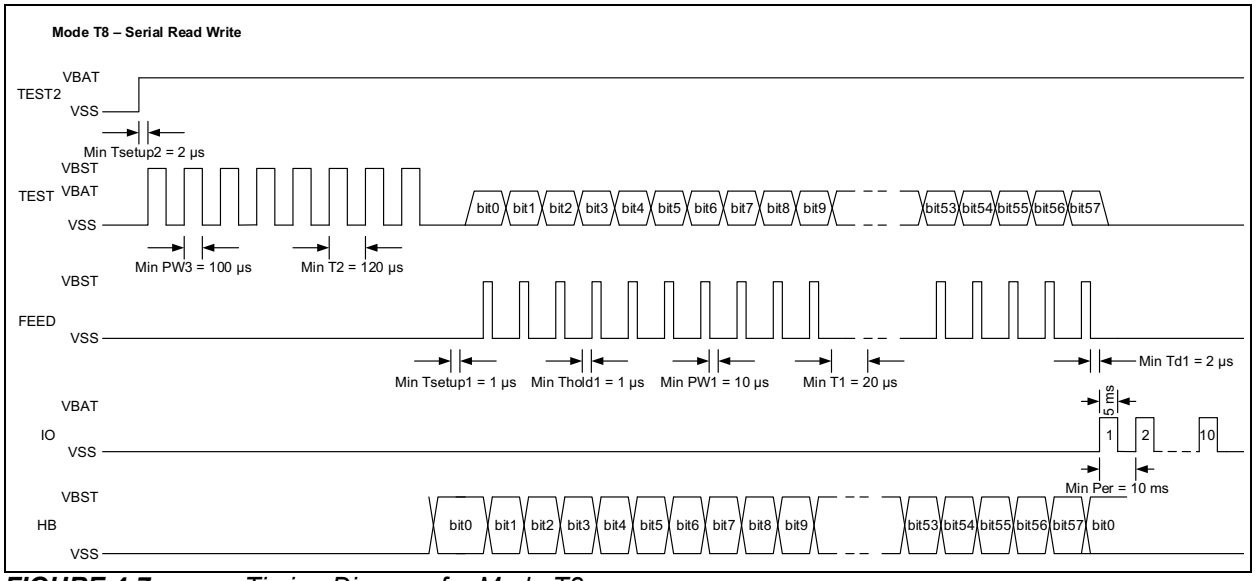


FIGURE 4-7: *Timing Diagram for Mode T8.*

4.7 LTD Baseline Measurement

If the Long-Term Drift Adjustment is enabled, a Long-Term Drift Baseline must be set. If an accurate value is known based on previous chamber characterization, it can be loaded above in T8 with the serial data. If not, zeros can be entered as placeholders in T8 and a long-term drift (LTD) baseline measurement must be made. To do this, the unit should be connected to its smoke chamber and placed in a No-Smoke condition.

1. Power up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive TEST2 input from VSS to VBAT to enter the Programming mode. TEST2 must remain high at VBAT until the measurement is completed.
3. Apply 9 clock pulses (VSS to VBST) to the TEST input to enter T9 mode. This initiates the LTD baseline measurement. The Integrator output will appear at GLED and the smoke detection level at RLED.
4. Pulse FEED from VSS to VBST to make the baseline measurement. The duration of this pulse should be at least 2 ms.
5. To save the LTD baseline measurement to EEPROM, pulse IO ten times from VSS to VBAT with FEED held low. The pulse should be 5 ms wide with a 10 ms period.
6. HS will be asserted high if the normal alarm max limit is less than or equal to the normal alarm limit or if the hysteresis alarm limit is greater than or equal to the normal alarm limit.

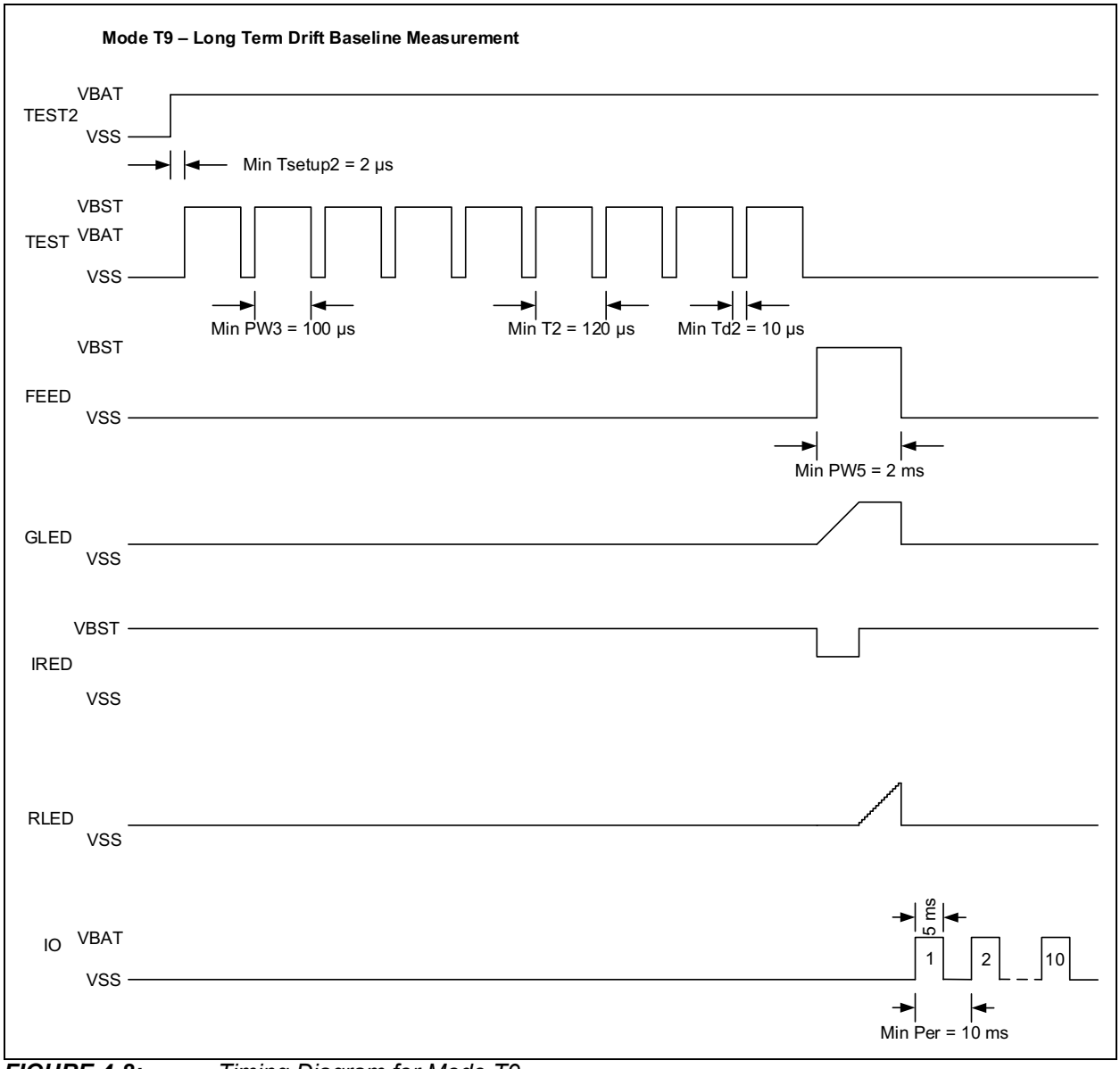


FIGURE 4-8: *Timing Diagram for Mode T9.*

4.8 Limits Verification

After all limits and the LTD baseline have been entered and stored into the memory, additional test modes are available to verify if the limits are functioning as expected.

The procedure is described in the following steps:

1. Power up with the bias conditions shown in Figure 4-3 or Figure 4-5.
2. Drive TEST2 input from VSS to VBAT to enter the Programming mode. TEST2 must remain high at VBAT through Step 7 described below.
3. Apply ten clock pulses to the TEST input to enter the T10 test mode. This initiates the verification mode for the Normal Limits setting. The integrator output will appear at GLED and the smoke detection level, DAC, at RLED.
4. At this point, pulse FEED high for at least 2 ms to initiate a smoke check. When the smoke detection level exceeds the alarm threshold, the HB output will be asserted high. The test is repeated each time FEED is clocked high.
5. Apply a clock pulse to the TEST input to enter the T11 mode and initiate verification for Hysteresis Limits. Repeat Step 4 to verify the Hysteresis Limit.
6. Apply a clock pulse to the TEST input to enter the T12 mode and initiate verification for Hush Limits. Repeat Step 4 to verify the Hush Limit.
7. Apply a clock pulse to the TEST input to enter the T13 mode and initiate verification for Chamber Test Limits. Repeat Step 4 to verify the Chamber Test Limit.
8. Apply a clock pulse to the TEST input to enter the T14 mode and initiate verification for Alarm Max Limits. Repeat Step 4 to verify the Alarm Max Limit.

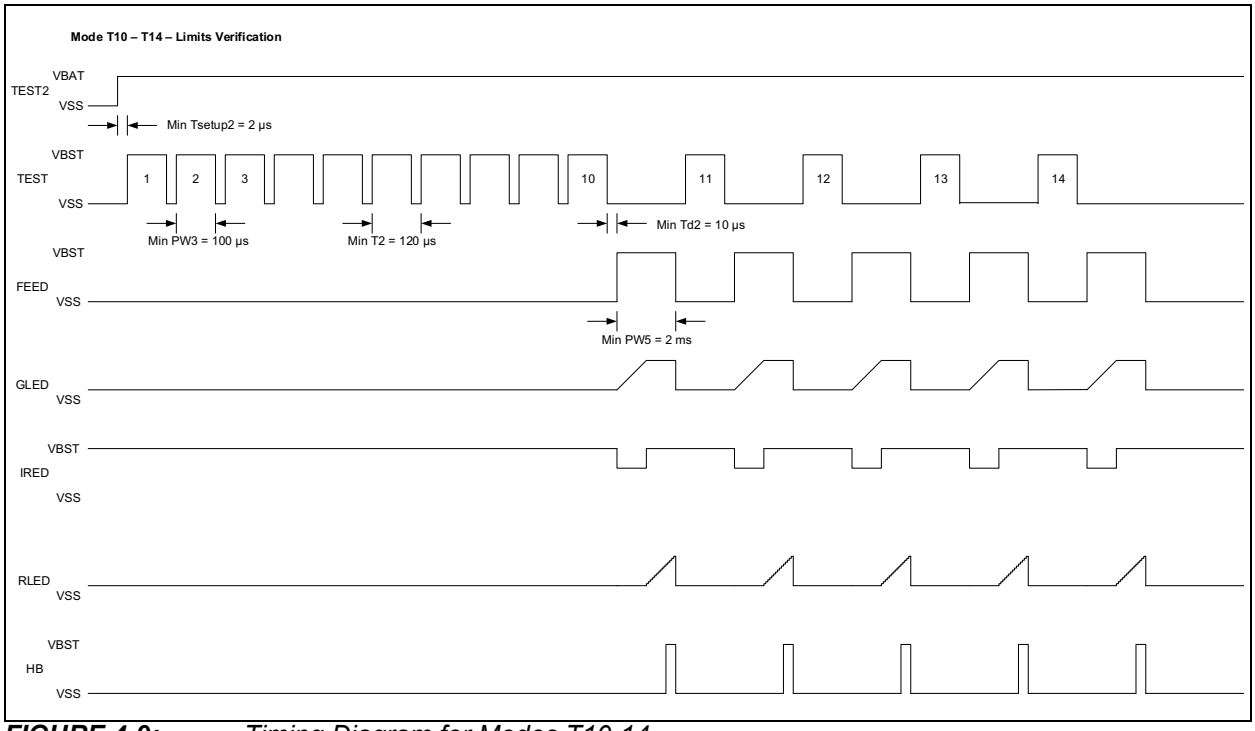


FIGURE 4-9: *Timing Diagram for Modes T10-14.*

NOTES:

5.0 APPLICATION NOTES

5.1 Standby Current Calculation and Battery Life

The supply current shown in the **DC Electrical Characteristics** table is only one component of the average standby current and, in most cases, can be a small fraction of the total, because power consumption generally occurs in relatively infrequent bursts and depends on many external factors. These include the values selected for IRED current and integration time, the VBST and IR capacitor sizes and leakages, the VBAT level, and the magnitude of any external resistances that will adversely affect the boost converter efficiency.

A calculation of the standby current for the battery life is shown in Table 5-1, based on the following parameters:

- VBAT = 3
- V_{BST1} = 3.6
- V_{BST2} = 9
- Boost capacitor size = 4.70E-06
- Boost Efficiency = 8.50E-01
- IRED on time = 2.000E-04
- IRED Current = 1.000E-01

TABLE 5-1: STANDBY CURRENT CALCULATION

Idd Component	Voltage (V)	Current (A)	Duration (s)	Energy (J)	Period (s)	Average Power (W)	Idd Contribution (A)	IBAT (µA)
Fixed Idd	3.0	1.00E-06	1.0	—	1.00	3.00E-06	1.00E-06	1.0
Photo Detection Current								
Chamber Test (excluding IR drive)	3.6	1.00E-03	3.00E-03	1.08E-05	43	2.95E-07	9.85E-08	0.1
IR drive during Chamber Test	3.6	0.1	2.00E-04	7.20E-05	43	1.97E-06	6.57E-07	0.7
Smoke Detection (excluding IR drive)	3.6	1.00E-03	3.00E-03	1.08E-05	10.75	1.18E-06	3.94E-07	0.4
IR drive during Smoke Detection	3.6	0.1	2.00E-04	7.20E-05	10.75	7.88E-06	2.63E-06	2.6
Low Battery Check Current								
Loaded Test								
Load	8.5	2.00E-02	1.00E-02	1.70E-03	344	5.81E-06	1.94E-06	2.1
Boost	V_{BST1} to V_{BST2}	—	—	68.5E-6	344	2.34E-07	7.81E-08	0.1
Unloaded Test								
Load	3.6	1.00E-04	1.00E-02	3.60E-06	43	9.85E-08	3.28E-08	0
						Total	6.82E-06	6.8

The following sections explain the components in Table 5-1 and the calculations in the example.

5.1.1 FIXED IBAT

The IBAT is the “Supply Current” shown in the **DC Electrical Characteristics** table.

5.1.2 PHOTO DETECTION CURRENT

The Photo Detection Current is the current draw caused by the smoke test every 10.75 seconds, and the chamber test every 43 seconds. The current for both the IR diode and the internal measurement circuitry comes primarily from VBST, so the average current must be scaled for both on-time and boost voltage.

The contribution to IBAT is determined by first calculating the energy consumed by each component, given its duration. An average power is then calculated based on the period of the event and the boost converter efficiency (assumed to be 85% in this case). An IBAT contribution is then calculated based on this average power and the given VBAT. For example, the IR drive contribution during chamber test is detailed in Equation 5-1.

EQUATION 5-1:

$$\frac{3.6V \times 0.1A \times 200\,ms}{43s \times 0.85 \times 3V} = 0.657\,mA$$

5.1.3 LOW BATTERY CHECK CURRENT

The Low Battery Check Current is the current required for the low battery test. It includes both the loaded (RLED on) and unloaded (RLED off) tests. The boost component of the loaded test represents the cost of charging the boost capacitor to the higher voltage level. This has a fixed cost for every loaded check, because the capacitor is gradually discharged during subsequent operations, and the energy is generally not recovered. The other calculations are similar to those shown in Equation 5-1. The unloaded test has a minimal contribution because it involves only some internal reference and comparator circuitry. The value of the RLED resistor, R6, in the Typical Application should be set to match the average horn current.

5.1.4 BATTERY LIFE

When estimating the battery life, several additional factors must be considered. These include battery resistance, battery self-discharge rate, capacitor leakages and the effect of the operating temperature on all of these characteristics. Some number of false alarms and user tests should also be included in any calculation.

For ten-year applications, a 3V spiral wound lithium manganese dioxide battery with a laser seal is recommended. These can be found with capacities of 1400 mAh to 1600 mAh.

5.1.5 BOOST REGULATOR

The boost regulator uses a current mode hysteretic architecture. The nominal peak current of the current mode control is 0.6 A. The boost regulator has two operating modes. Low Boost operation provides a nominal boost voltage of 3.6V and is typically used in standby operation. The High Boost operation provides 8.5 V or 10V. The High Boost operation is used for Alarm conditions and loaded low battery check. The boost regulator uses soft start when switching from Low Boost to High Boost operation to limit inrush current.

The boost regulator efficiency is sensitive to series resistance in the high current switching path especially during High Boost operation. From the **Typical Application** schematic, the critical components of this resistance are the inductor DC resistance, the internal resistance of the battery and the resistance in the connections from the inductor to the battery, from the inductor to the LX pin and from the VSS pin to the battery. In order to function properly under full load at V_{DD} = 2V, the total of the inductor and interconnect resistances should not exceed 0.3Ω. The internal battery resistance should be no more than 0.5Ω, and a low ESR capacitor of 10 µF or more should be connected in parallel with the battery, to average the current draw over the boost converter cycle. The Schottky diode, D1, must have a maximum peak current rating of at least 0.8A. For best results it should have forward voltage specification of less than 0.5V at 0.8 A, and low reverse leakage. Inductor, L1 must have a peak current rating of at least 0.8 A.

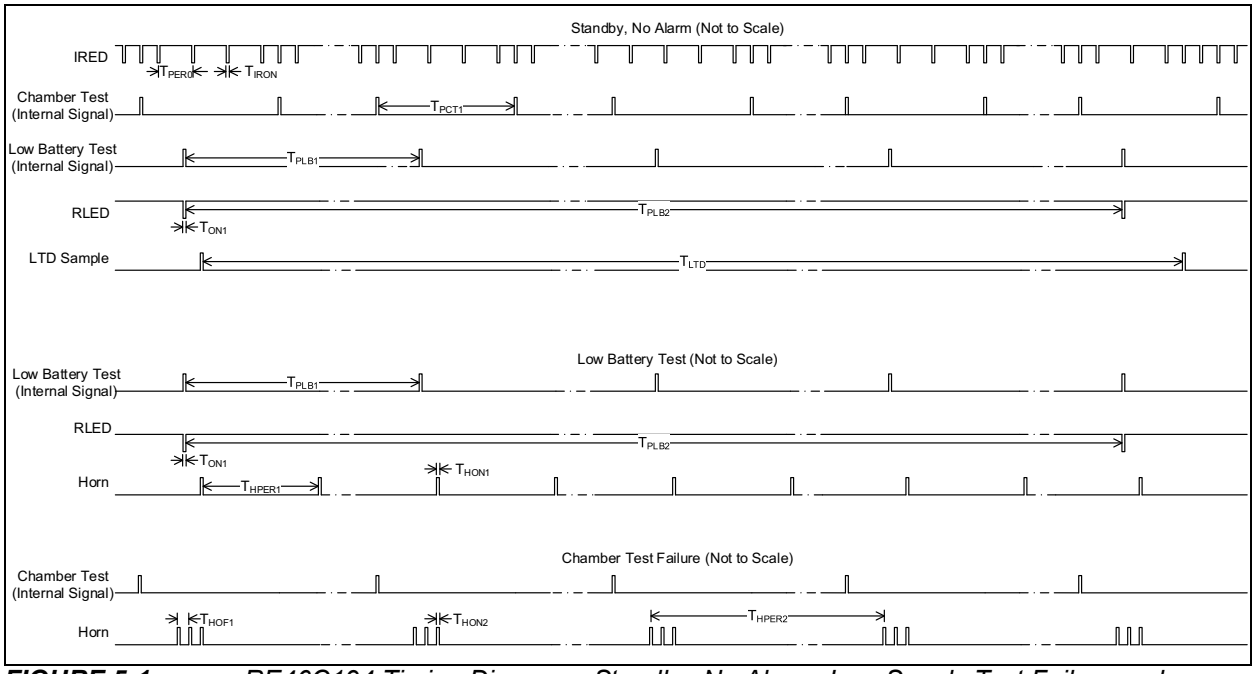


FIGURE 5-1: *RE46C194 Timing Diagram - Standby, No Alarm, Low Supply Test Failure and Chamber Test Failure.*

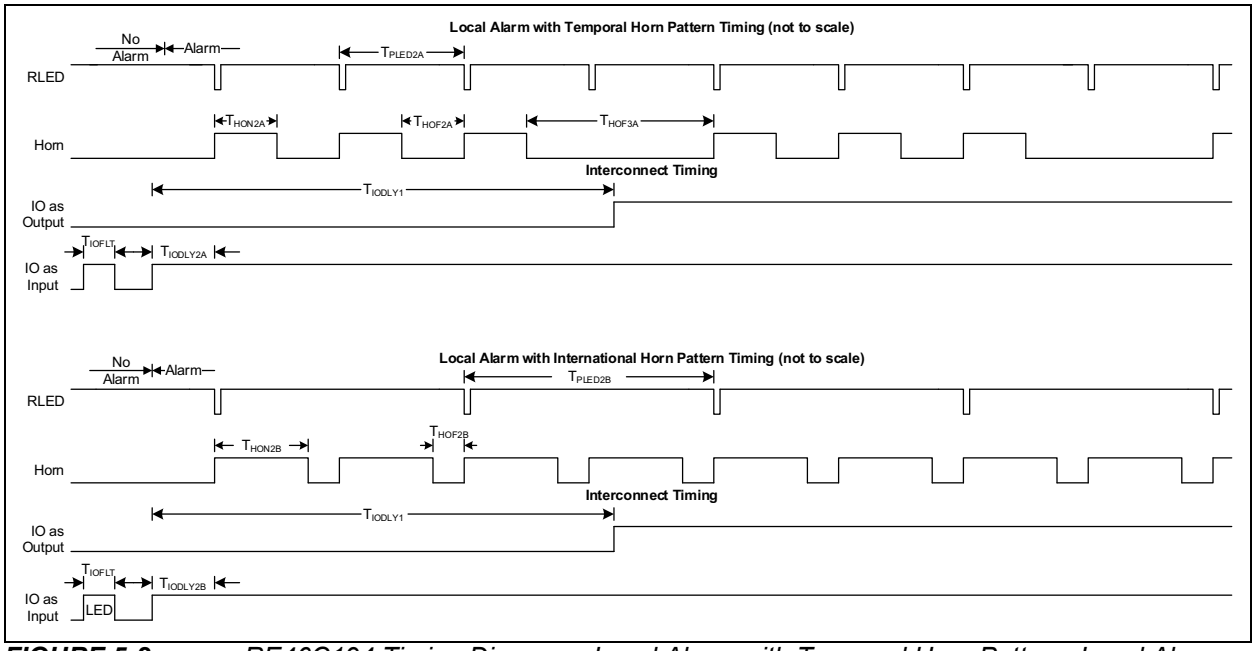


FIGURE 5-2: *RE46C194 Timing Diagram - Local Alarm with Temporal Horn Pattern, Local Alarm with International Horn Pattern.*

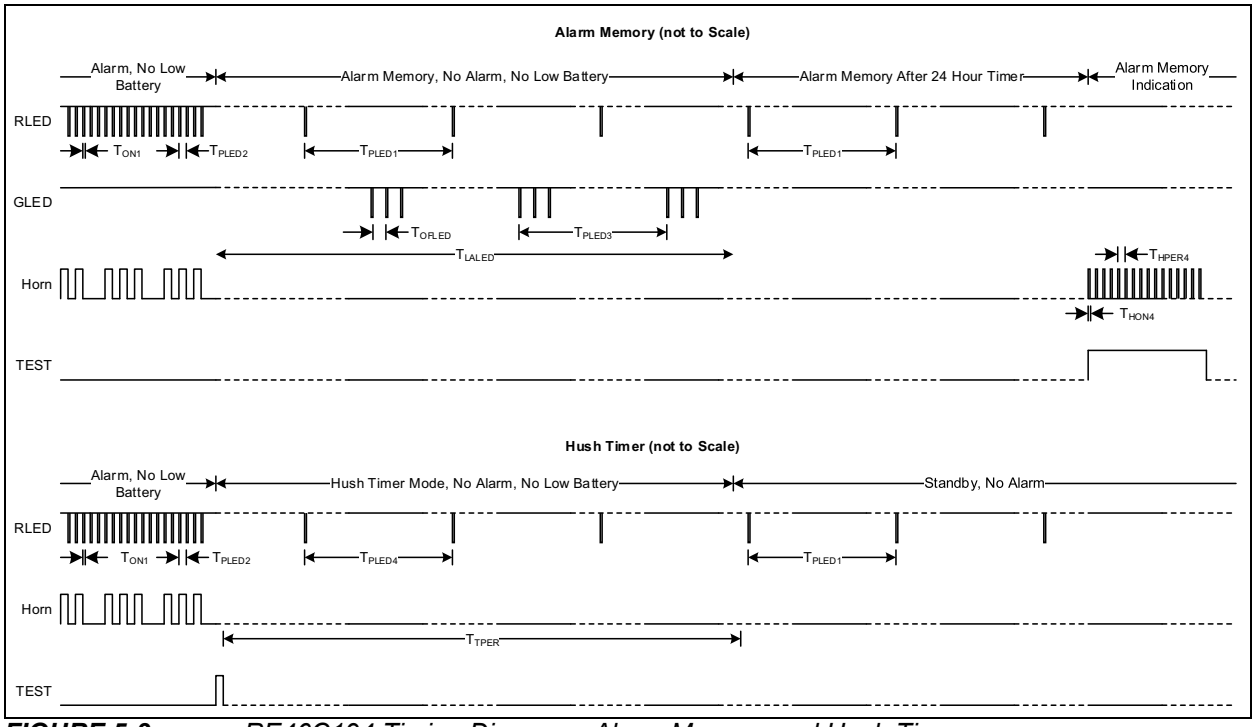


FIGURE 5-3: *RE46C194 Timing Diagram - Alarm Memory and Hush Timer.*

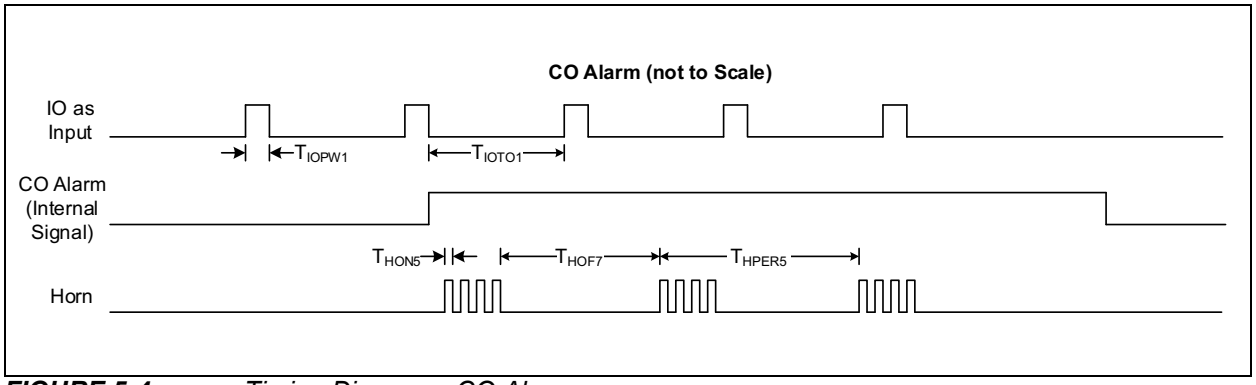


FIGURE 5-4: *Timing Diagram - CO Alarm.*

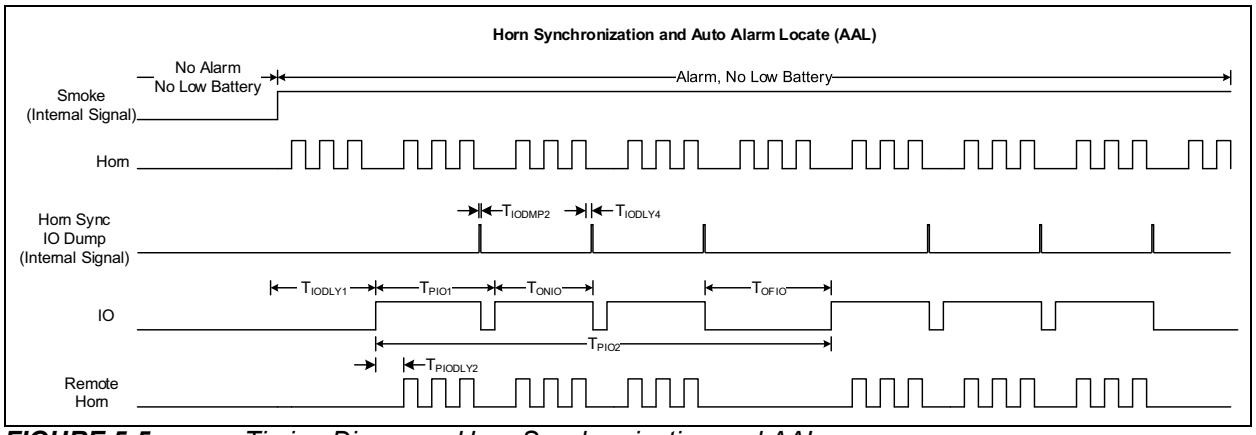
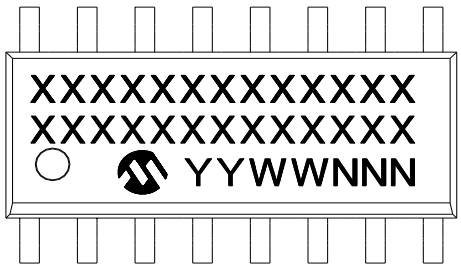


FIGURE 5-5: *Timing Diagram - Horn Synchronization and AAL.*

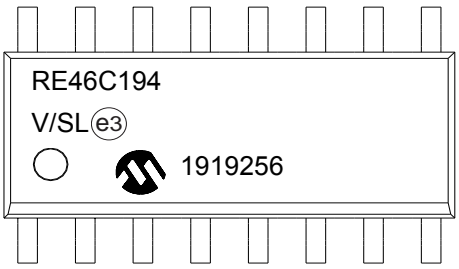
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead SOIC



Example

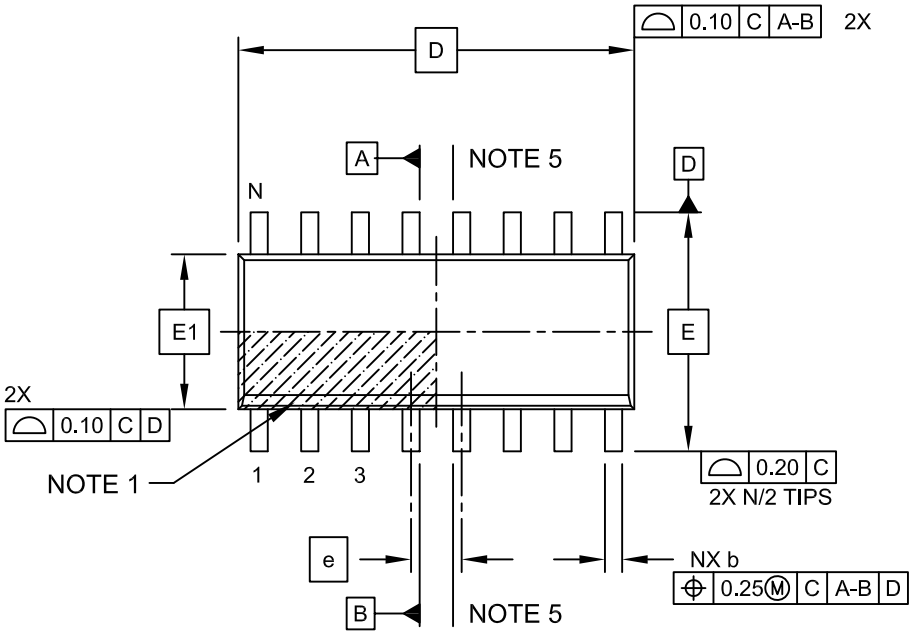


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

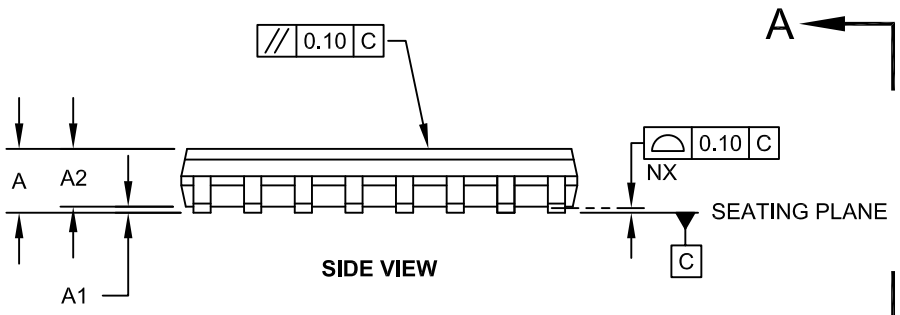
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

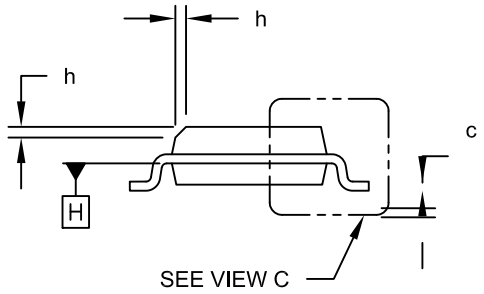
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

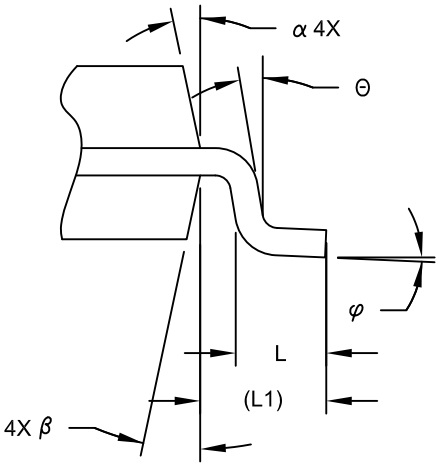


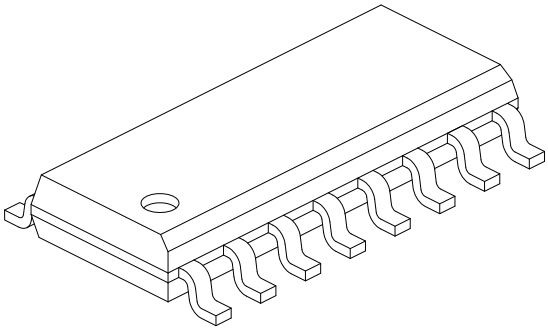
VIEW A-A

Microchip Technology Drawing No. C04-108C Sheet 1 of 2

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		9.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

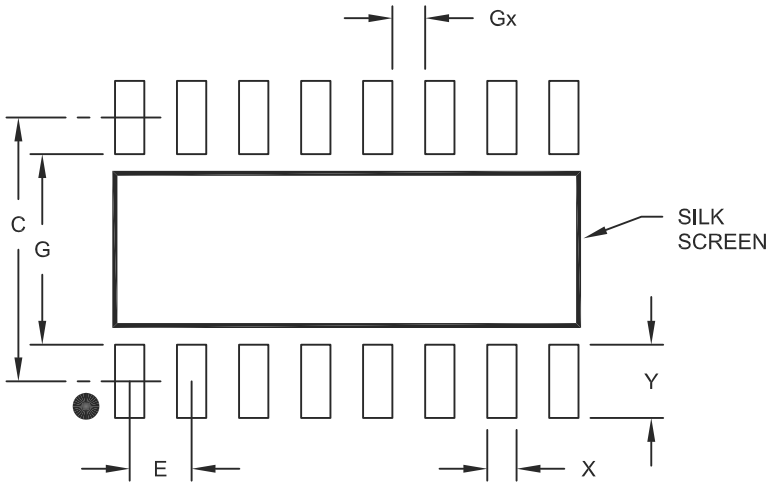
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-108C Sheet 2 of 2

16-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2108A

APPENDIX A: REVISION HISTORY

Revision A (June 2019)

- Original Release of this Data Sheet.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	[X](1)
Device	Package Type	Number of Pins	Tape and Reel

Device:	RE46C194 = CMOS Low-Voltage Photoelectric Smoke Detector ASIC with Interconnect and Timer Mode		
Package Type:	S	=	SOIC (Plastic Small Outline)
Number of Pins:	16	=	16 pins
Tape and Reel Option:	Blank T	= =	Standard packaging (tube or tray) Tape and Reel(1)

Examples:

a) RE46C194S16 16 Lead SOIC package

b) RE46C194S16T Tape and Reel, 16 Lead SOIC package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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