

Features

- Very high-speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to 85 °C
 - Automotive-A: -40 °C to 85 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62138CV25/30/33
- Ultra low standby power
 - Typical standby current: 1 μA
 - Maximum standby current: 5 μA
- Ultra low active power
 - Typical active current: 1.6 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} Features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for Optimum speed and power
- Offered in Pb-free 36-ball VFBGA, 32-pin TSOP II, 32-pin SOIC, 32-pin TSOP I and 32-pin STSOP packages

Functional Description

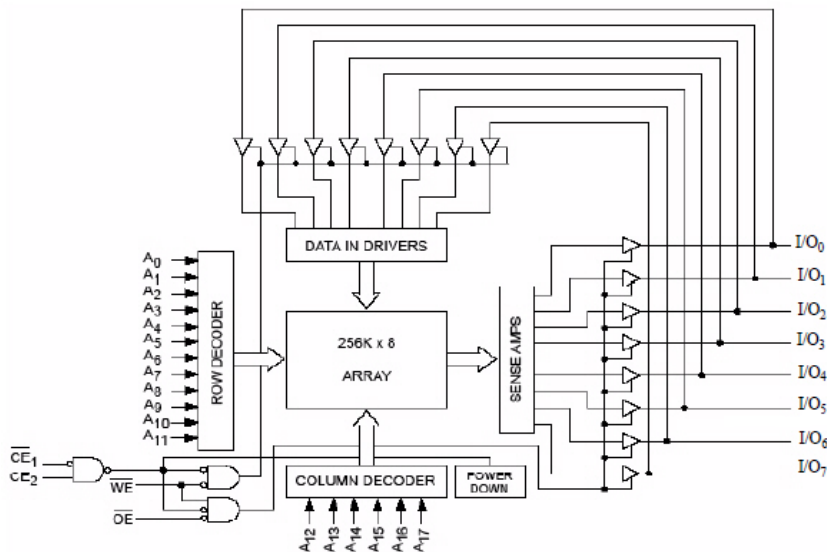
The CY62138FV30 is a high performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Place the device into standby mode reducing power consumption when deselected (\overline{CE}_1 HIGH or CE_2 LOW).

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₇).

To read from the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O₀ through I/O₇) are placed in a high impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW and CE_2 HIGH and \overline{WE} LOW).

Logic Block Diagram



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Pin Configurations

Figure 1. 36-ball VFBGA (Top View) [1]

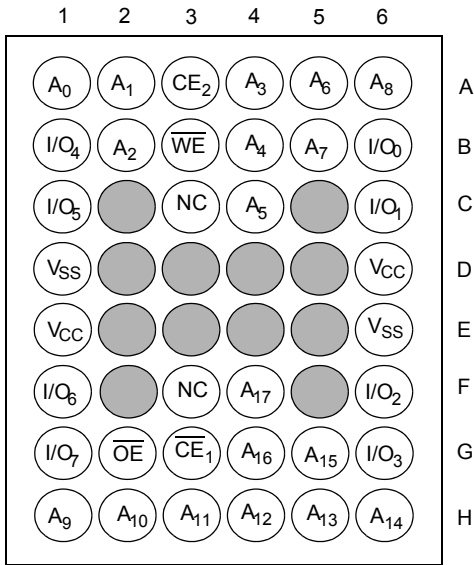


Figure 3. 32-pin TSOP I (Top View)

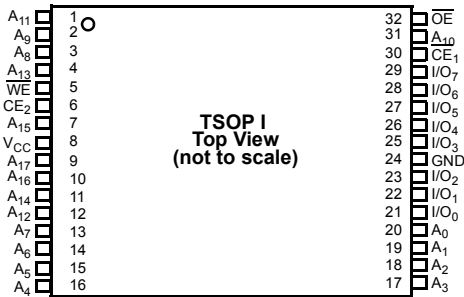


Figure 2. 32-pin SOIC/TSOP II (Top View)

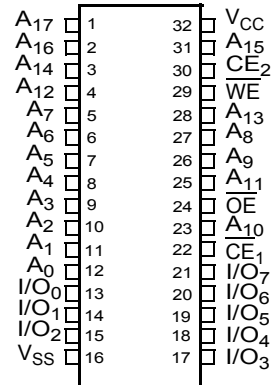
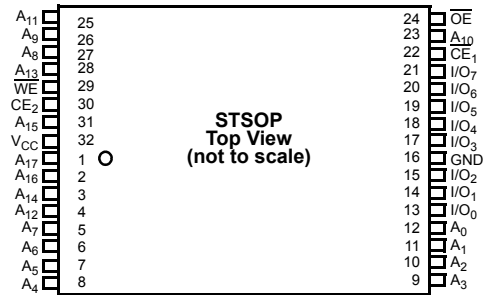


Figure 4. 32-pin STSOP (Top View)



Product Portfolio

| Product | Range | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---------------|---------------------------|---------------------------|---------|----------------------|------------|--------------------------------|-----|---------|-----|-------------------------------|-----|
| | | | | | | Operating I _{CC} (mA) | | | | Standby I _{SB2} (μA) | |
| | | f = 1 MHz | | f = f _{max} | | | | | | | |
| | | Min | Typ [2] | Max | | Typ [2] | Max | Typ [2] | Max | Typ [2] | Max |
| CY62138FV30LL | Industrial / Automotive-A | 2.2 | 3.0 | 3.6 | 45 | 1.6 | 2.5 | 13 | 18 | 1 | 5 |

Notes

1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

| | |
|---|-------------------|
| Storage temperature | -65 °C to +150 °C |
| Ambient temperature with power applied | -55 °C to +125 °C |
| Supply voltage to ground potential | -0.3 V to 3.9 V |
| DC voltage applied to outputs in High Z State ^[3, 4] | -0.3 V to 3.9 V |

| | |
|---|-----------------|
| DC input voltage ^[3, 4] | -0.3 V to 3.9 V |
| Output current into outputs (LOW) | 20 mA |
| Static Discharge Voltage (MIL-STD-883, Method 3015) | > 2001 V |
| Latch-up current | > 200 mA |

Operating Range

| Product | Range | Ambient Temperature | V _{CC} ^[5] |
|---------------|---------------------------|---------------------|--------------------------------|
| CY62138FV30LL | Industrial / Automotive-A | -40 °C to +85 °C | 2.2 V to 3.6 V |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 45 ns (Industrial / Automotive-A) | | | Unit |
|---------------------------------|---|--|-----------------------------------|--------------------|-------------------------|------|
| | | | Min | Typ ^[6] | Max | |
| V _{OH} | Output HIGH voltage | I _{OH} = -0.1 mA | 2.0 | - | - | V |
| | | I _{OH} = -1.0 mA, V _{CC} ≥ 2.70 V | 2.4 | - | - | V |
| V _{OL} | Output LOW voltage | I _{OL} = 0.1 mA | - | - | 0.4 | V |
| | | I _{OL} = 2.1 mA, V _{CC} ≥ 2.70 V | - | - | 0.4 | V |
| V _{IH} | Input HIGH voltage | V _{CC} = 2.2 V to 2.7 V | 1.8 | - | V _{CC} + 0.3 V | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.2 | - | V _{CC} + 0.3 V | V |
| V _{IL} | Input LOW voltage | V _{CC} = 2.2 V to 2.7 V | -0.3 | - | 0.6 | V |
| | | For BGA package | | | | |
| | | V _{CC} = 2.7 V to 3.6 V | -0.3 | - | 0.8 | V |
| I _{IX} | Input leakage current | V _{CC} = 2.2 V to 3.6 V | -0.3 | - | 0.6 | V |
| | | For other packages | | | | |
| I _{OZ} | Output leakage current | GND ≤ V _O ≤ V _{CC} , output disabled | -1 | - | +1 | μA |
| I _{CC} | V _{CC} Operating supply current | f = f _{max} = 1/t _{RC} | - | 13 | 18 | mA |
| | | f = 1 MHz | - | 1.6 | 2.5 | |
| I _{SB1} ^[7] | Automatic CE Power-down current—CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, V _{IN} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V, f = f _{max} (address and data only), f = 0 (OE, and WE), V _{CC} = 3.60 V | - | 1 | 5 | μA |
| I _{SB2} ^[7] | Automatic CE Power-down current—CMOS inputs | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = 3.60 V | - | 1 | 5 | μA |

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25 °C.
- Chip enables (CE₁ and CE₂) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

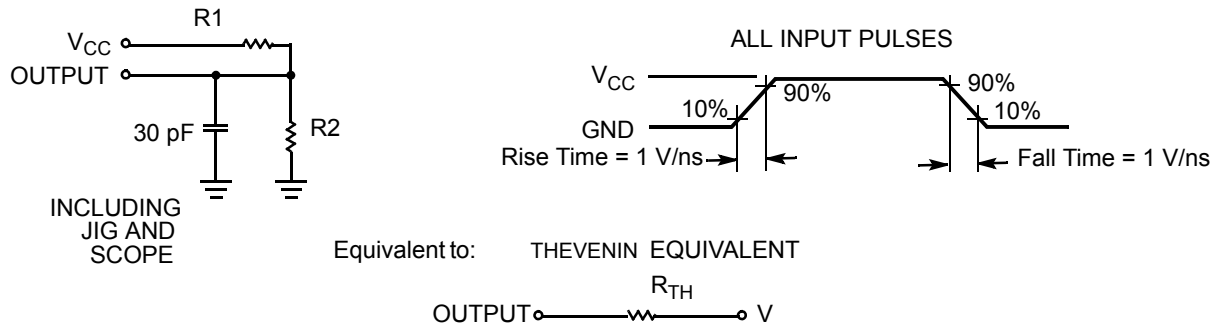
| Parameter ^[8] | Description | Test Conditions | Max | Unit |
|--------------------------|--------------------|--|-----|------|
| C _{IN} | Input Capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ.)} | 10 | pF |
| C _{OUT} | Output Capacitance | | 10 | pF |

Thermal Resistance

| Parameter ^[8] | Description | Test Conditions | 32-pin SOIC | 36-ball VFBGA | 32-pin TSOP II | 32-pin STSOP | 32-pin TSOP I | Unit |
|--------------------------|--|--|-------------|---------------|----------------|--------------|---------------|------|
| Θ _{JA} | Thermal resistance (Junction to Ambient) | Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board | 44.53 | 38.49 | 44.16 | 59.72 | 50.19 | °C/W |
| Θ _{JC} | Thermal resistance (Junction to Case) | | 24.05 | 17.66 | 11.97 | 15.38 | 14.59 | °C/W |

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms



| Parameter | 2.5 V (2.2 V to 2.7 V) | 3.0 V (2.7 V to 3.6 V) | Unit |
|-----------------|------------------------|------------------------|------|
| R ₁ | 16667 | 1103 | Ω |
| R ₂ | 15385 | 1554 | Ω |
| R _{TH} | 8000 | 645 | Ω |
| V _{TH} | 1.20 | 1.75 | V |

Note

8. Tested initially and after any design or process changes that may affect these parameters.

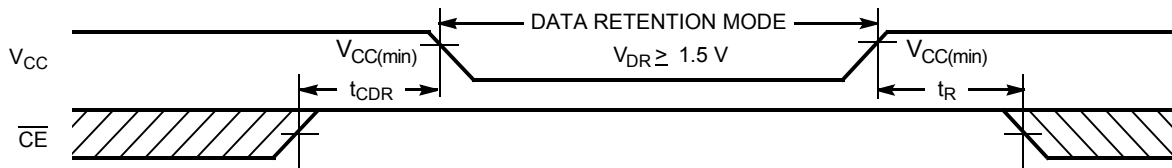
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[9] | Max | Unit |
|----------------------------|--------------------------------------|--|-----|--------------------|-----|---------------|
| V_{DR} | V_{CC} for data retention | | 1.5 | – | – | V |
| I_{CCDR} ^[10] | Data retention current | $V_{CC} = 1.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 1 | 4 | μA |
| t_{CDR} ^[11] | Chip deselect to data retention time | | 0 | – | – | ns |
| t_R ^[12] | Operation recovery time | | 45 | – | – | ns |

Data Retention Waveform

Figure 6. Data Retention Waveform^[13]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(\text{typ})}$, $T_A = 25\text{ }^\circ\text{C}$.
10. Chip enables (\overline{CE}_1 and CE_2) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.
13. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.

Switching Characteristics

Over the Operating Range

| Parameter [14, 15] | Description | 45 ns (Industrial/ Automotive-A) | | Unit |
|-----------------------------|---|-------------------------------------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t_{RC} | Read cycle time | 45 | – | ns |
| t_{AA} | Address to data valid | – | 45 | ns |
| t_{OHA} | Data hold from address change | 10 | – | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to data valid | – | 45 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 22 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z [16] | 5 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z [16, 17] | – | 18 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to Low Z [16] | 10 | – | ns |
| t_{HZCE} | \overline{CE}_1 HIGH or CE_2 LOW to High Z [16, 17] | – | 18 | ns |
| t_{PU} | \overline{CE}_1 LOW and CE_2 HIGH to Power-up | 0 | – | ns |
| t_{PD} | \overline{CE}_1 HIGH or CE_2 LOW to Power-down | – | 45 | ns |
| Write Cycle [18, 19] | | | | |
| t_{WC} | Write cycle time | 45 | – | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to write end | 35 | – | ns |
| t_{AW} | Address setup to write end | 35 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | ns |
| t_{SA} | Address setup to Write Start | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse Width | 35 | – | ns |
| t_{SD} | Data setup to write end | 25 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z [16, 17] | – | 18 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z [16] | 10 | – | ns |

Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tristate parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [AC Test Loads and Waveforms on page 5](#).
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the output enters a high impedance state.
18. The internal write time of the memory is defined by the overlap of \overline{WE} , $CE_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.
19. The minimum write pulse width for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) should be the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 7. Read Cycle 1 (Address Transition Controlled) [20, 21]

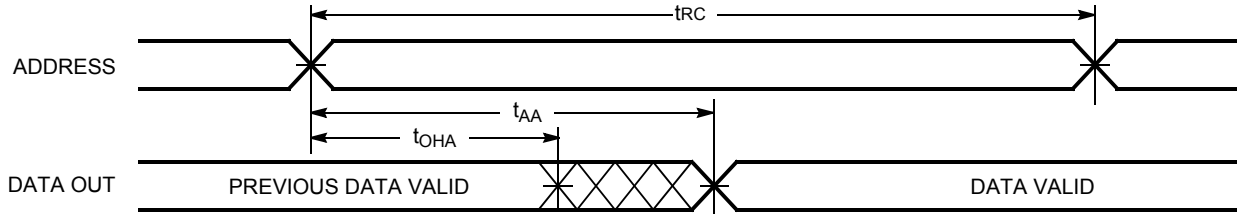


Figure 8. Read Cycle No. 2 (\overline{OE} Controlled) [21, 22, 23]

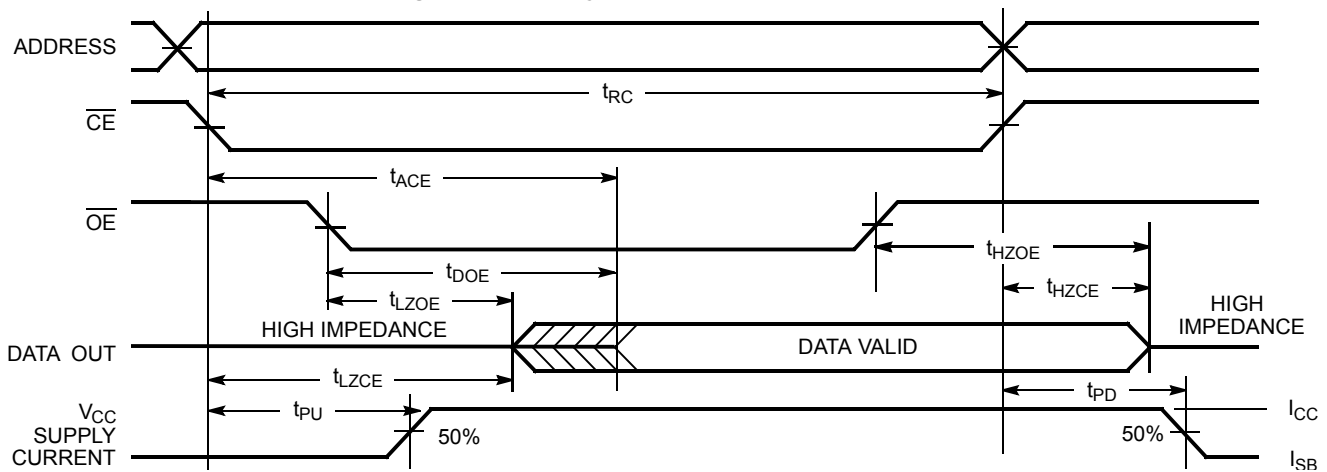
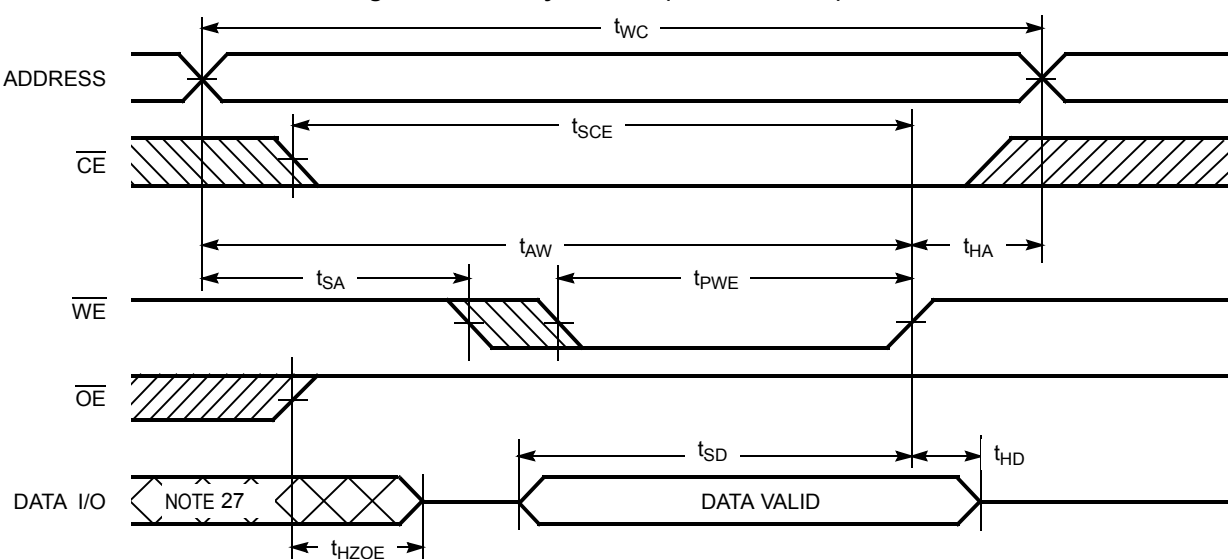


Figure 9. Write Cycle No. 1 (\overline{WE} Controlled) [23, 24, 25, 26]



Notes

- 20. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- 21. WE is HIGH for read cycle.
- 22. Address valid before or similar to \overline{CE}_1 transition LOW and CE_2 transition HIGH.
- 23. CE is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 24. The internal write time of the memory is defined by the overlap of WE, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.
- 25. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 26. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
- 27. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled) [28, 29, 30, 31]

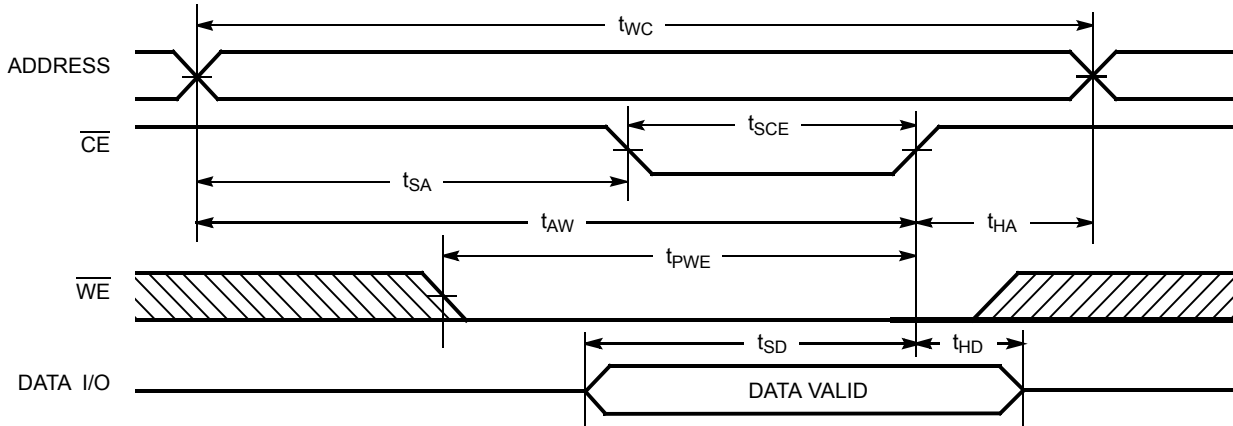
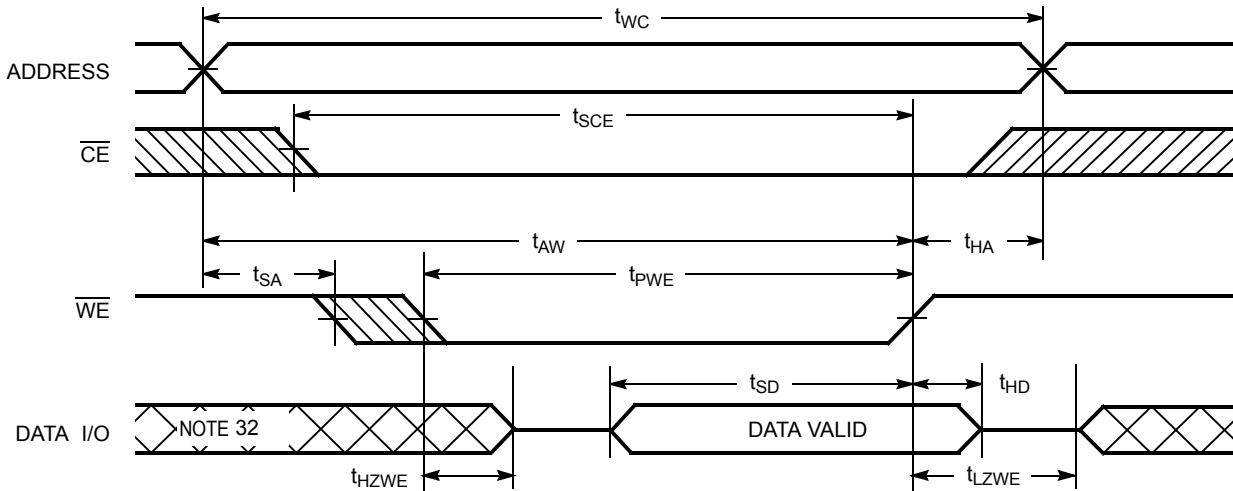


Figure 11. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [28, 31, 33]



Notes

28. \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
29. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. Reference the data input setup and hold timing to the edge of the signal that terminates the write.
30. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
31. If \overline{CE}_1 goes HIGH or CE_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in high impedance state.
32. During this period, the I/Os are in output state. Do not apply input signals.
33. The minimum write pulse width for Write Cycle No. 2 (\overline{WE} controlled, \overline{OE} LOW) should be the sum of t_{HZWE} and t_{SD} .

Truth Table

| \overline{CE}_1 | CE_2 | \overline{WE} | \overline{OE} | Inputs/Outputs | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|----------------|---------------------|----------------------|
| H | X ^[34] | X | X | High Z | Deselect/Power-down | Standby (I_{SB}) |
| X ^[34] | L | X | X | High Z | Deselect/Power-down | Standby (I_{SB}) |
| L | H | H | L | Data out | Read | Active (I_{CC}) |
| L | H | H | H | High Z | Output disabled | Active (I_{CC}) |
| L | H | L | X | Data in | Write | Active (I_{CC}) |

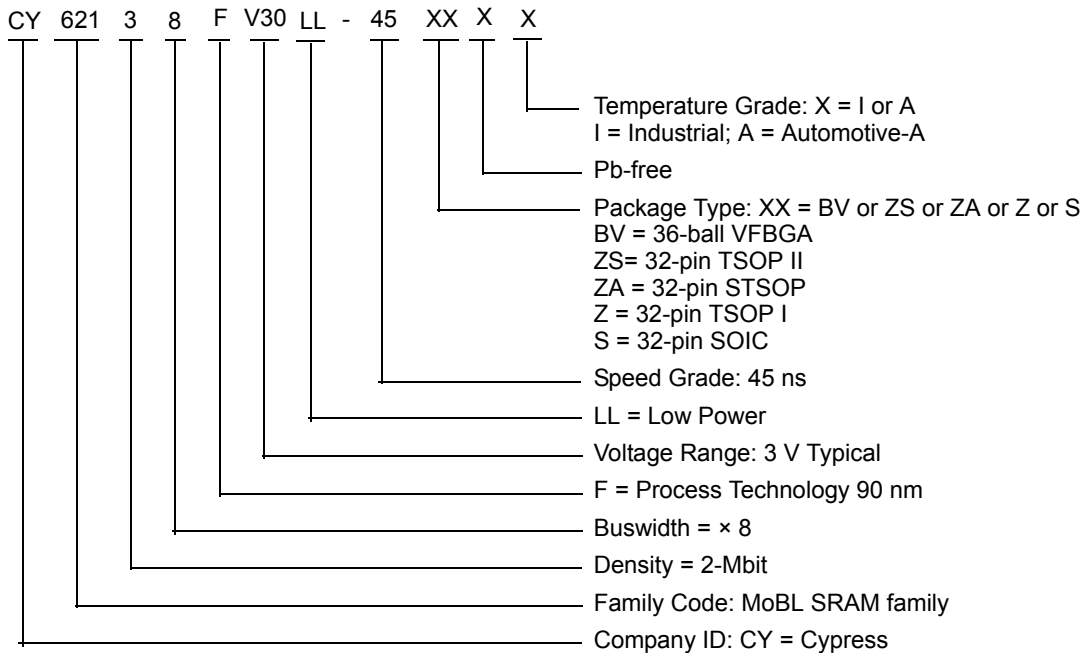
Note

34. The 'X' (Don't care) state for the Chip enables (\overline{CE}_1 and CE_2) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

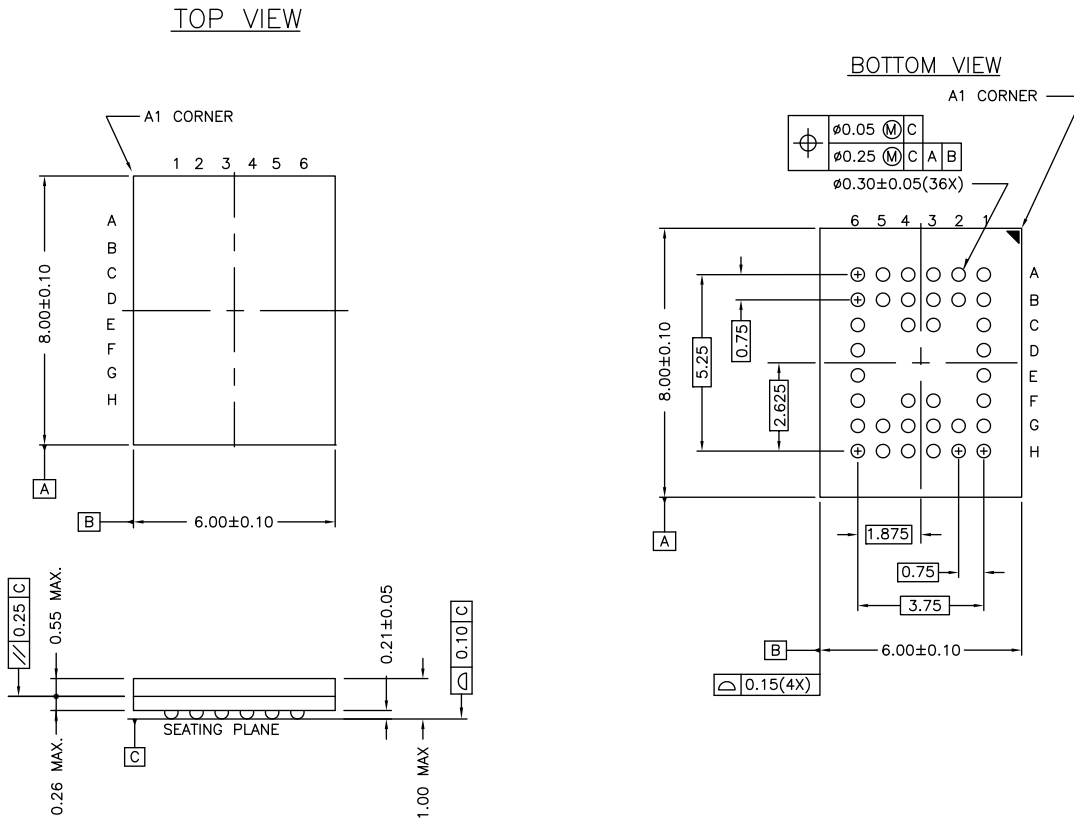
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|----------------------|-----------------|-------------------------|-----------------|
| 45 | CY62138FV30LL-45BVXI | 51-85149 | 36-ball VFBGA (Pb-free) | Industrial |
| | CY62138FV30LL-45ZAXI | 51-85094 | 32-pin STSOP (Pb-free) | |
| | CY62138FV30LL-45ZXI | 51-85056 | 32-pin TSOP I (Pb-free) | |
| | CY62138FV30LL-45SXI | 51-85081 | 32-pin SOIC (Pb-free) | |
| | CY62138FV30LL-45ZAXA | 51-85094 | 32-pin STSOP (Pb-free) | Automotive-A |

Ordering Code Definitions



Package Diagrams

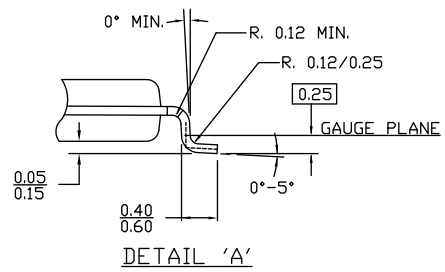
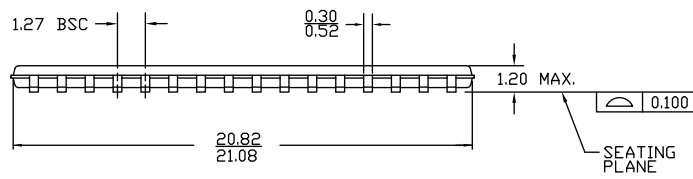
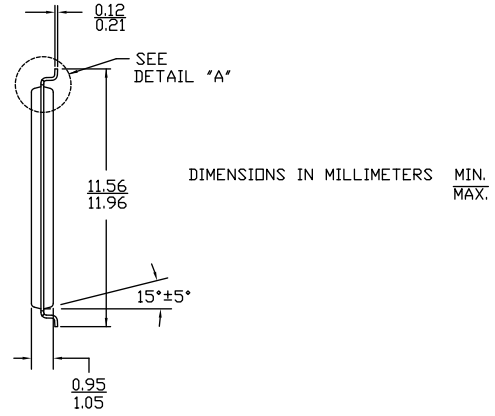
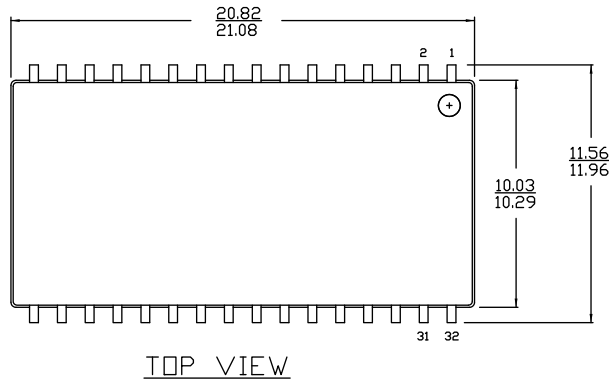
Figure 12. 36-ball VFBGA (6 × 8 × 1.0 mm) BV36A Package Outline, 51-85149



51-85149 *E

Package Diagrams (continued)

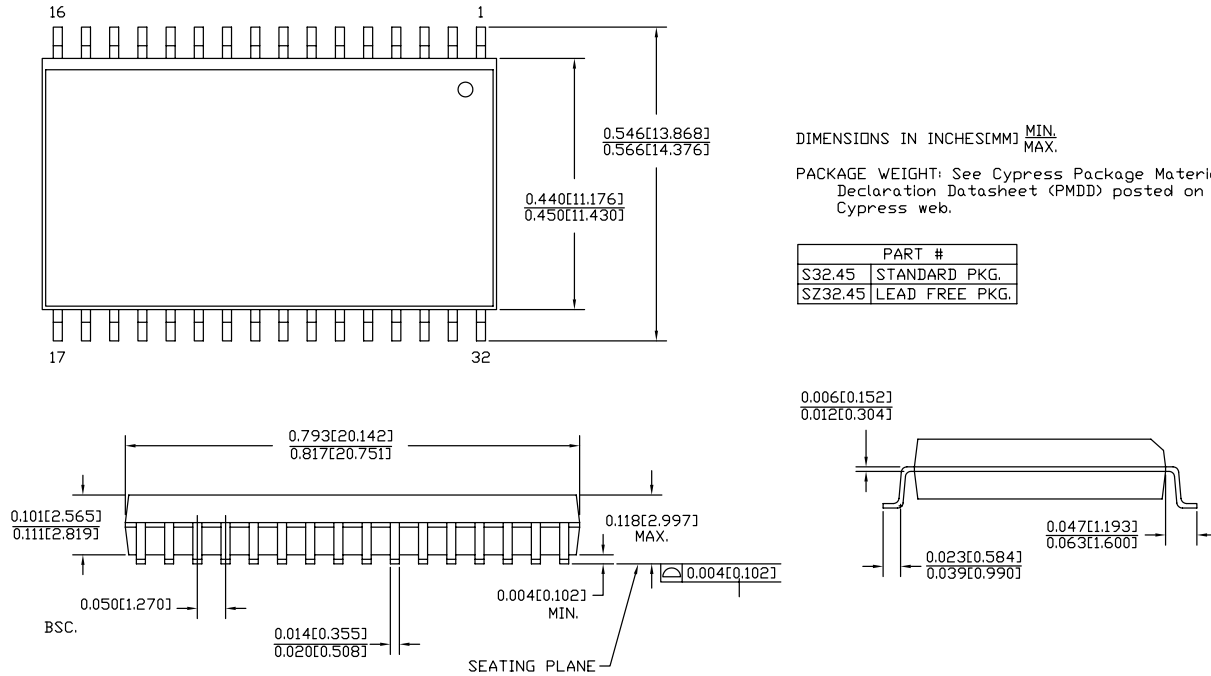
Figure 13. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



51-85095 *B

Package Diagrams (continued)

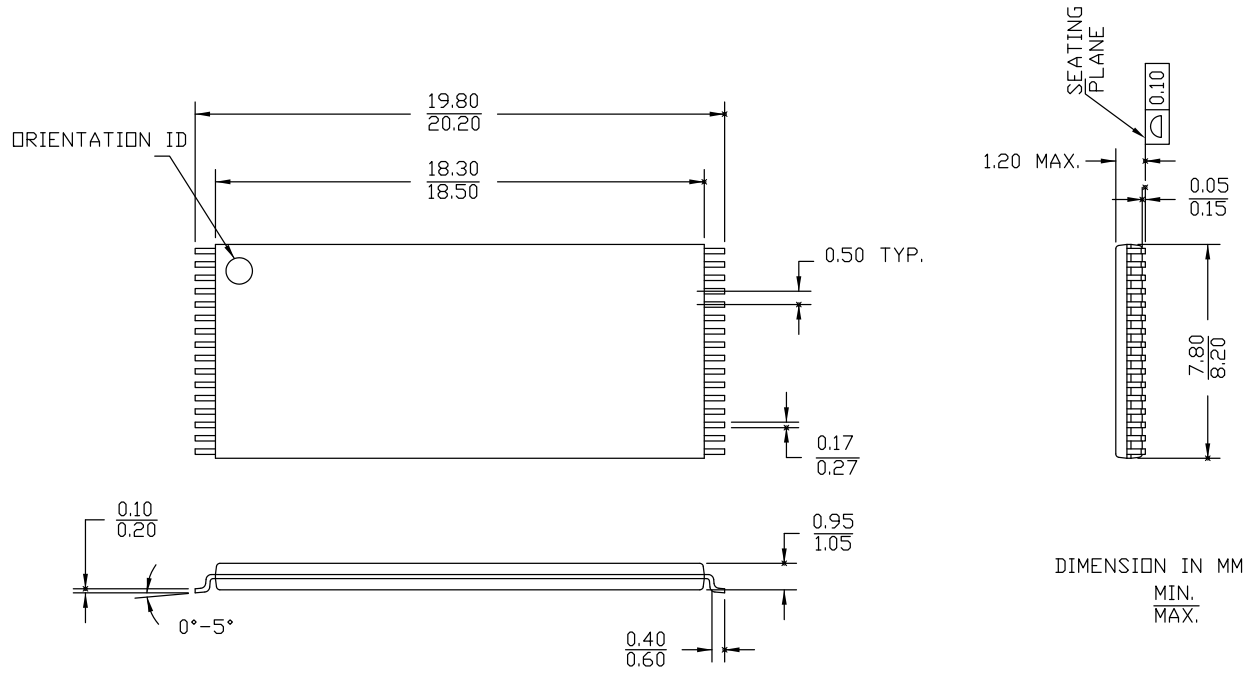
Figure 14. 32-pin Molded SOIC (450 Mil) S32.45/SZ32.45 Package Outline, 51-85081



51-85081 *E

Package Diagrams (continued)

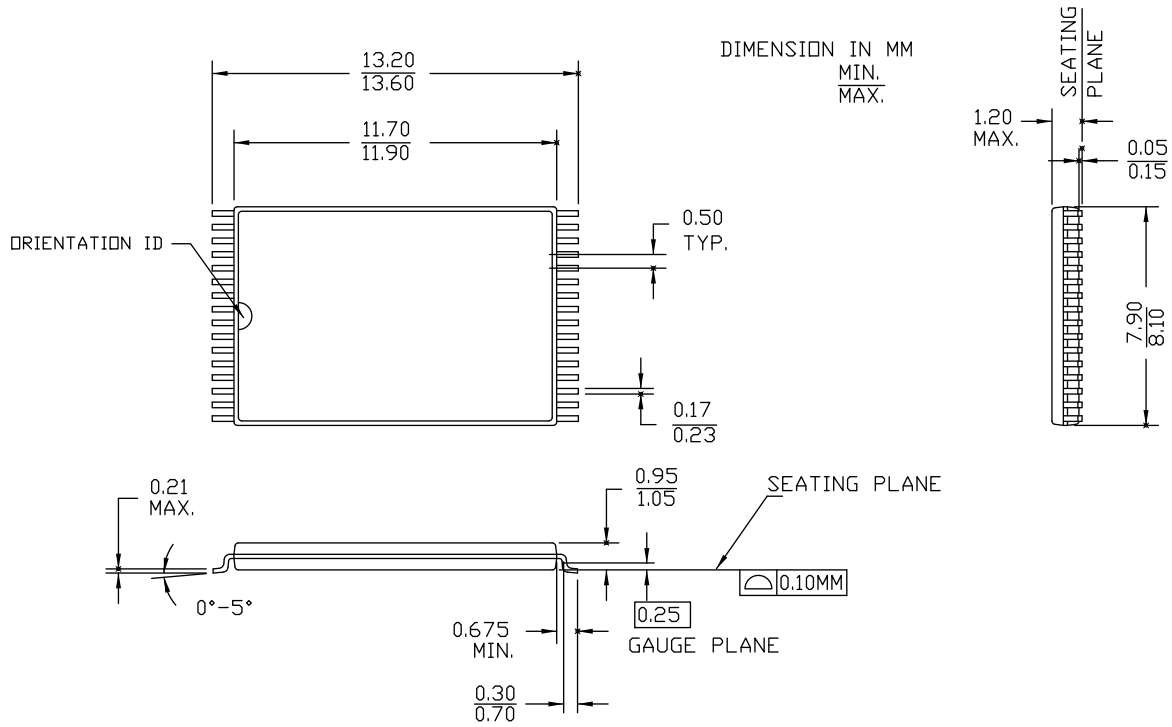
Figure 15. 32-pin TSOP I (8 × 20 × 1.0 mm) Z32R Package Outline, 51-85056



51-85056 *G

Package Diagrams (continued)

Figure 16. 32-pin STSOP (8 × 13.4 × 1.2 mm) ZA32 Package Outline, 51-85094



51-85094 *G

Acronyms

| Acronym | Description |
|---------|---|
| BGA | Ball Grid Array |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| OE | Output Enable |
| SOIC | Small-Outline Integrated Circuit |
| SRAM | Static Random Access Memory |
| STSOP | Small Thin Small Outline Package |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| WE | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY62138FV30 MoBL [®] , 2-Mbit (256 K × 8) Static RAM Document Number: 001-08029 | | | | |
|---|---------|-----------------|-----------------|--|
| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
| ** | 463660 | See ECN | NXR | New data sheet. |
| *A | 467351 | See ECN | NXR | Added 32-pin TSOP II package, 32 pin TSOP I and 32 pin STSOP packages Changed ball A3 from NC to CE ₂ in 36-ball FBGA pin out |
| *B | 566724 | See ECN | NXR | Converted from Preliminary to Final Corrected typo in 32 pin TSOP II pin configuration diagram on page #2 (changed pin 24 from CE ₁ to OE and pin 22 from CE to CE ₁) Changed the I _{CC(max)} value from 2.25 mA to 2.5 mA for test condition f=1 MHz Changed the I _{SB2(typ)} value from 0.5 μA to 1 μA Changed the I _{SB2(max)} value from 2.5 μA to 5 μA Changed the I _{CCDR(typ)} value from 0.5 μA to 1 μA and I _{CCDR(max)} value from 2.5 μA to 4 μA |
| *C | 797956 | See ECN | VKN | Added 32-pin SOIC package Updated VIL spec for SOIC, TSOP-II, TSOP-I, and STSOP packages on Electrical characteristics table |
| *D | 809101 | See ECN | VKN | Corrected typo in the Ordering Information table |
| *E | 940341 | See ECN | VKN | Added footnote #7 related to I _{SB2} and I _{CCDR} |
| *F | 2769239 | 09/25/09 | VKN / AESA | Included Automotive-A information |
| *G | 3055119 | 10/12/2010 | RAME | Updated and converted all tablenotes into Footnote Added Ordering Code Definitions . Updated All Package Diagrams . Added Acronyms and Units of Measure table Updated data sheet as per new template. |
| *H | 3061313 | 10/15/2010 | RAME | Minor changes: Corrected "IO" to "I/O" |
| *I | 3078557 | 11/04/2010 | RAME | Corrected 55 C to -55C in Ambient Temperature with Power applied in Maximum Ratings Section |
| *J | 3235744 | 04/20/2011 | RAME | Removed the note "For best practice recommendations, refer to the Cypress application Note "System Design Guidelines" at http://www.cypress.com " in page 1 and its reference in Functional Description . Updated Package Diagrams . |
| *K | 3285093 | 06/16/2011 | RAME | Updated in new template. |
| *L | 3845087 | 12/18/2012 | TAVA | Updated Ordering Information (Updated part numbers). Updated Package Diagrams : spec 51-85149 – Changed revision from *D to *E. spec 51-85081 – Changed revision from *C to *E. |
| *M | 4099045 | 08/19/2013 | VINI | Updated Switching Characteristics : Added Note 14 and referred the same note in "Parameter" column. Updated in new template. |

Document History Page (continued)

| Document Title: CY62138FV30 MoBL [®] , 2-Mbit (256 K × 8) Static RAM Document Number: 001-08029 | | | | |
|---|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
| *N | 4377056 | 05/12/2014 | MEMJ | <p>Updated Switching Characteristics: Added Note 19 and referred the same note in "Write Cycle".</p> <p>Updated Switching Waveforms: Added Note 33 and referred the same note in Figure 11.</p> <p>Updated Package Diagrams: spec 51-85056 – Changed revision from *F to *G. spec 51-85094 – Changed revision from *F to *G.</p> <p>Completing Sunset Review.</p> |

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