

S128 Microcontroller Group

Datasheet

Renesas Synergy™ Platform

Synergy Microcontrollers

S1 Series

The integrated module for Digital Addressable Lighting Interface (DALI) communications is designed for compliance to IEC 62386 version 2 (DALI 2) when used with suitable software and hardware.

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Ultra low power 32-MHz Arm® Cortex®-M0+ core, up to 256-KB code flash memory, 24-KB SRAM, Digital Addressable Lighting Interface, Capacitive Touch Sensing Unit, 14-bit A/D Converter, 8-bit D/A Converter, security and safety features.

Features

■ Arm Cortex-M0+ Core

- Arm®v6-M architecture
- Maximum operating frequency: 32 MHz
- Arm® Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, BPU, CoreSight™ MTB-M0+
- CoreSight Debug Port: SW-DP

■ Memory

- Up to 256-KB code flash memory
- 4-KB data flash memory (100,000 erase/write cycles)
- Up to 24-KB SRAM
- Memory protection units
- 128-bit unique ID

■ Connectivity

- USB 2.0 Full-Speed (USBFS) module
 - On-chip transceiver with voltage regulator
 - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 3
 - UART
 - Simple IIC
 - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I²C bus interface (IIC) × 2
- Controller Area Network (CAN) module
- Digital Addressable Lighting Interface (DALI)

■ Analog

- 14-bit A/D Converter (ADC14)
- 8-bit D/A Converter (DAC8) × 3
- High-Speed Analog Comparator (ACMPHS) × 3
- Low-Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 4
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 32-bit (GPT32)
- General PWM Timer 16-bit High Resolution (GPT16H) × 3
- General PWM Timer 16-bit (GPT16) × 3
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety

- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management

- Low power modes
- Realtime clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption

- AES128/256
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)

- Capacitive Touch Sensing Unit (CTSUS)

■ Multiple Clock Sources

- Main clock oscillator (MOSC)
 - (1 to 20 MHz when VCC = 2.4 to 5.5 V)
 - (1 to 8 MHz when VCC = 1.8 to 5.5 V)
 - (1 to 4 MHz when VCC = 1.6 to 5.5 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
 - (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
 - (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
 - (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports

- Up to 53 input/output pins
 - Up to 3 CMOS input
 - Up to 50 CMOS input/output
 - Up to 5V tolerant input/output
 - Up to 2 high current (20 mA)

■ Operating Voltage

- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages

- Ta = -40°C to +85°C
 - 36-pin LGA (4 mm × 4 mm, 0.5 mm pitch)
- Ta = -40°C to +105°C
 - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
 - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
 - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
 - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
 - 32-pin QFN (5 mm × 5 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm[®]-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates an energy-efficient Arm Cortex[®]-M0+ 32-bit core that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 256 KB code flash memory
- 24-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- 14-bit A/D Converter (ADC14)
- 8-bit D/A Converter (DAC8)
- Security features.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M0+ core	<ul style="list-style-type: none"> • Maximum operating frequency: up to 32 MHz • Arm Cortex-M0+ core: <ul style="list-style-type: none"> - Revision: r0p1-00rel0 - Armv6-M architecture profile - Single-cycle integer multiplier. • Arm Memory Protection Unit (Arm MPU) <ul style="list-style-type: none"> - Armv6 Protected Memory System Architecture - 8 protect regions. • SysTick timer <ul style="list-style-type: none"> - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB of code flash memory. See section 42, Flash Memory in User's Manual.
Data flash memory	4 KB of data flash memory. See section 42, Flash Memory in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). See section 41, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating mode	Two operating modes: <ul style="list-style-type: none"> • Single-chip mode • SCI boot mode. See section 3, Operating Modes in User's Manual.

Table 1.3 System (2 of 2)

Feature	Functional description
Resets	<p>13 resets:</p> <ul style="list-style-type: none"> • RES pin reset • Power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • CPU stack pointer error reset • Software reset. <p>See section 5, Resets in User's Manual.</p>
Low Voltage Detection (LVD)	<p>The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 7, Low Voltage Detection (LVD) in User's Manual.</p>
Clock	<ul style="list-style-type: none"> • Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDG-dedicated on-chip oscillator • Clock out support. <p>See section 8, Clock Generation Circuit in User's Manual.</p>
Clock Frequency Accuracy Measurement Circuit (CAC)	<p>The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.</p> <p>See section 9, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.</p>
Interrupt Controller Unit (ICU)	<p>The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module. The ICU also controls NMI interrupts. See section 12, Interrupt Controller Unit (ICU) in User's Manual.</p>
Key Interrupt Function (KINT)	<p>A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 18, Key Interrupt Function (KINT) in User's Manual.</p>
Low Power Mode	<p>Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 10, Low Power Modes in User's Manual.</p>
Register Write Protection	<p>The register write protection function protects important registers from being overwritten because of software errors. See section 11, Register Write Protection in User's Manual.</p>
Memory Protection Unit (MPU)	<p>Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 14, Memory Protection Unit (MPU) in User's Manual.</p>
Watchdog Timer (WDT)	<p>The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 24, Watchdog Timer (WDT) in User's Manual.</p>
Independent Watchdog Timer (IWDG)	<p>The Independent Watchdog Timer (IWDG) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDG provides functionality to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDG can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 25, Independent Watchdog Timer (IWDG) in User's Manual.</p>

Table 1.4 Event Link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 16, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 15, Data Transfer Controller (DTC) in User's Manual.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with one channel and a 16-bit timer with six channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 20, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 19, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 22, Asynchronous General Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 23, Realtime Clock (RTC) in User's Manual.

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 27, Serial Communications Interface (SCI) in User's Manual.
Digital Addressable Lighting Interface (DALI)	A Digital Addressable Lighting Interface (DALI) module is provided. DALI is an international open lighting control communication protocol that includes dimming control of electronic ballasts and LED lights from different manufacturers. The DALI interface module is designed to allow compliance with international standard IEC62386-101 Edition 1.0/2.0 (DALI 2), that includes software control. See section 28, Digital Addressable Lighting Interface (DALI) in User's Manual.

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
I ² C bus interface (IIC)	The 2-channel I ² C bus interface (IIC) conforms with and provides a subset of the NXP I ² C (Inter-Integrated Circuit) bus interface functions. See section 29, I ² C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 31, Serial Peripheral Interface (SPI) in User's Manual.
Control Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 30, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module is a USB controller that can operate as a device controller. The module supports full-speed and low-speed transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 5 pipes. Pipe 0 and pipe 4 to pipe 7 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. The MCU supports Battery Charging Specification revision 1.2. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply 3.3 V. See section 26, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

Table 1.8 Analog

Feature	Functional description
14-bit A/D Converter (ADC14)	A 14-bit successive approximation A/D converter is provided. Up to 21 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 33, 14-Bit A/D Converter (ADC14) in User's Manual.
8-bit D/A Converter (DAC8)	An 8-bit D/A converter (DAC8) is provided. See section 34, 8-Bit D/A Converter (DAC8) in User's Manual.
Temperature Sensor (TSN)	The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application. See section 35, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	The analog comparator compares a test voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the test voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output) and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 37, High-Speed Analog Comparator (ACMPHS) in User's Manual.
Low-Power Analog Comparator (ACMPLP)	The analog comparator compares a reference input voltage and analog input voltage. The comparison result can be read by software and also be output externally. The reference input voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin, an output from internal D/A converter, or from the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption. See section 38, Low-Power Analog Comparator (ACMPLP) in User's Manual.
Operational Amplifier (OPAMP)	The operational amplifier amplifies small analog input voltages and outputs the amplified voltages. A total of four differential operational amplifier units with two input pins and one output pin are provided. See section 36, Operational Amplifier (OPAMP) in User's Manual.

Table 1.9 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that a finger does not come into direct contact with the electrode. See section 39, Capacitive Touch Sensing Unit (CTSU) in User's Manual.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) Calculator	The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 32, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 40, Data Operation Circuit (DOC) in User's Manual.

Table 1.11 Security

Feature	Functional description
AES	See section 43, AES Engine in User's Manual
True Random Number Generator (TRNG)	See section 44, True Random Number Generator (TRNG) in User's Manual

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

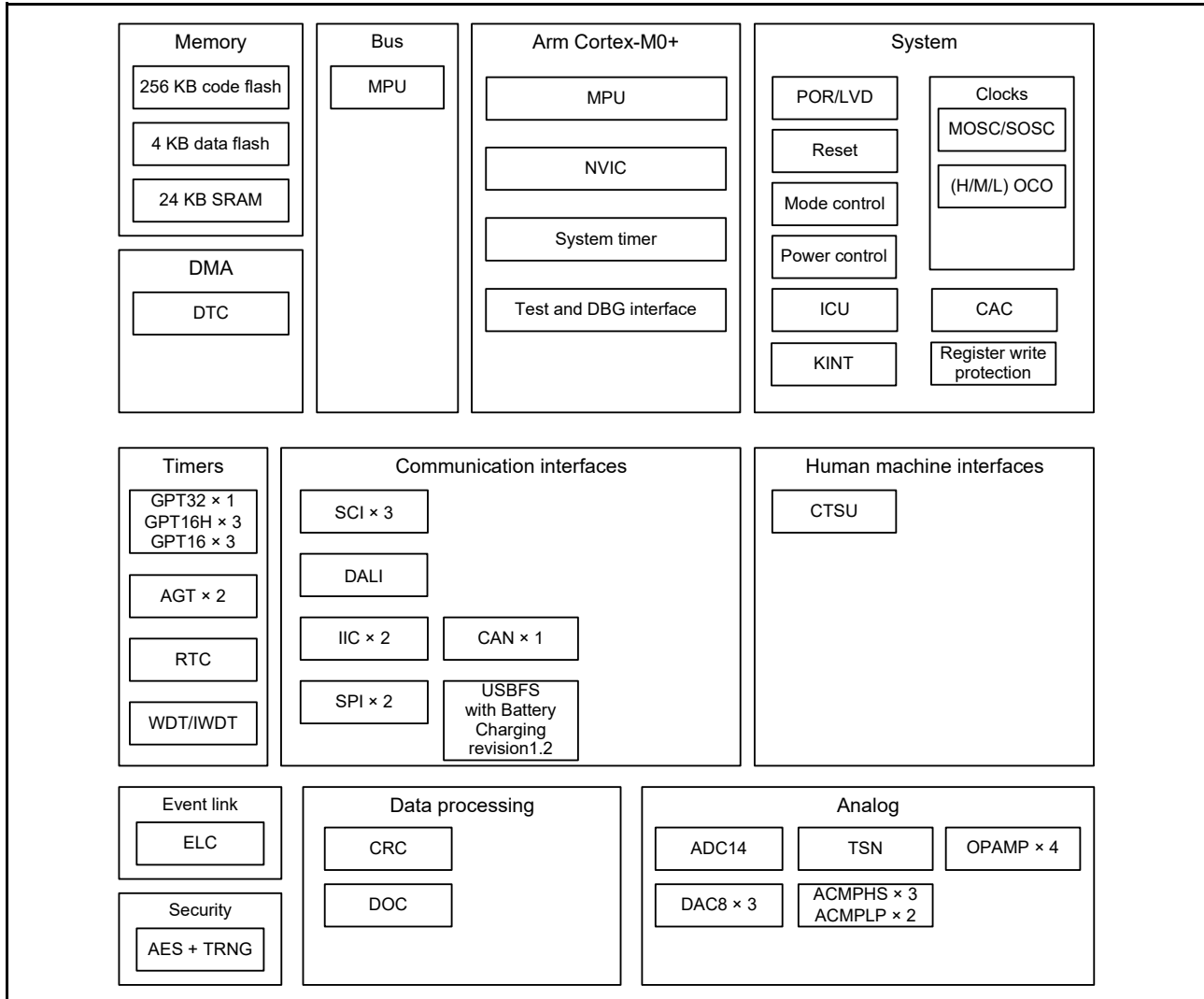


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a product list.

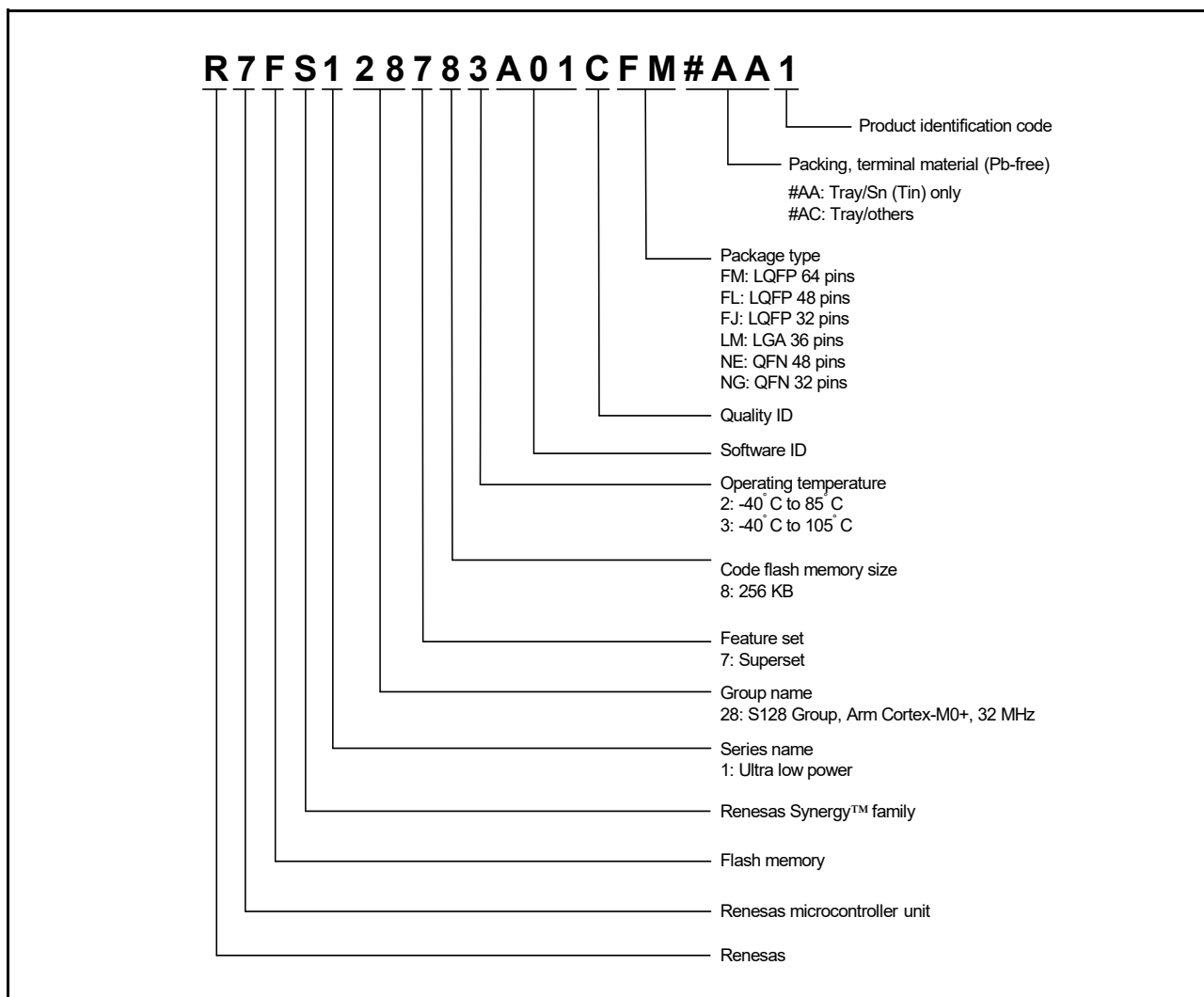


Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FS128783A01CFM	R7FS128783A01CFM#AA1	PLQP0064KB-C	256 KB	4 KB	24 KB	-40 to +105°C
R7FS128783A01CFL	R7FS128783A01CFL#AA1	PLQP0048KB-B				-40 to +105°C
R7FS128783A01CNE	R7FS128783A01CNE#AC1	PWQN0048KB-A				-40 to +105°C
R7FS128782A01CLM	R7FS128782A01CLM#AC1	PWLG0036KA-A				-40 to +85°C
R7FS128783A01CFJ	R7FS128783A01CFJ#AA1	PLQP0032GB-A				-40 to +105°C
R7FS128783A01CNG	R7FS128783A01CNG#AC1	PWQN0032KB-A				-40 to +105°C

1.4 Function Comparison

Table 1.13 Function comparison

Parts number	R7FS128783A01CFM	R7FS128783A01CFL R7FS128783A01CNE	R7FS128782A01CLM	R7FS128783A01CFJ R7FS128783A01CNG
Pin count	64	48	36	32
Package	LQFP	LQFP/QFN	LGA	LQFP/QFN
Code flash memory	256 KB			
Data flash memory	4 KB			
SRAM	24 KB			
	Parity	8 KB		
	ECC	16 KB		
System	CPU clock	32 MHz		
	ICU	Yes		
	KINT	8	5	4
Event control	ELC	Yes		
DMA	DTC	Yes		
Timers	GPT32	1		
	GPT16H	3	3	2
	GPT16	3	3	1
	AGT	2		
	RTC	Yes		
	WDT/IWDT	Yes		
Communication	SCI	3		
	DALI	Yes		
	IIC	2	2	1
	SPI	2	2	1
	CAN	Yes		
	USBFS	Yes		
Analog	ADC14	21	15	10
	DAC8	3		
	ACMPHS	3		
	ACMPLP	2		
	OPAMP	4	3	2
	TSN	Yes		
HMI	CTSU	28	21	9
Data processing	CRC	Yes		
	DOC	Yes		
Security	AES and TRNG			

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description	
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1- μ F capacitor. The capacitor should be placed close to the pin.	
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.	
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).	
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.	
	EXTAL	Input		
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.	
	XCOUT	Output		
	CLKOUT	Output		Clock output pin
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state.	
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.	
CAC	CACREF	Input	Measurement reference clock input pin	
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin	
	SWCLK	Input	Serial wire clock pin	
Interrupt	NMI	Input	Non-maskable interrupt request pin	
	IRQ0 to IRQ7	Input	Maskable interrupt request pins	
GPT	GTETRGA, GTETRGB	Input	External trigger input pin	
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	Input capture, output compare, or PWM output pin	
	GTIU	Input	Hall sensor input pin U	
	GTIV	Input	Hall sensor input pin V	
	GTIW	Input	Hall sensor input pin W	
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)	
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)	
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)	
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)	
	GTOUWP	Output	3-phase PWM output for BLDC motor control (positive W phase)	
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)	
	AGT	AGTEE0, AGTEE1	Input	External event input enable
		AGTIO0, AGTIO1	I/O	External event input and pulse output
AGTO0, AGTO1		Output	Pulse output	
AGTOA0, AGTOA1		Output	Output compare match A output	
AGTOB0, AGTOB1		Output	Output compare match B output	
RTC	RTCCOUT	Output	Output pin for 1-Hz/64-Hz clock	

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0, SCL1, SCL9	I/O	Input/output pins for the IIC clock (simple IIC)
	SDA0, SDA1, SDA9	I/O	Input/output pins for the IIC data (simple IIC)
	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (simple SPI)
	MISO0, MISO1, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI)
	MOSI0, MOSI1, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI)
DALI	SS0, SS1, SS9	Input	Chip-select input pins (simple SPI), active-low
	DRX0	Input	Input pin for DALI received data
IIC	DTX0	Output	Output pin for DALI transmitted data
	SCL0, SCL1	I/O	Input/output pins for clock
SPI	SDA0, SDA1	I/O	Input/output pins for data
	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VSS_USB	Input	Ground pins
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.
Analog power supply	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
ADC14	AN000 to AN013, AN016 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low
DAC8	DA0 to DA2	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator output	VCOUT	Output	Comparator output pin
ACMPHS	IVREF0 to IVREF2	Input	Reference voltage input pin
	IVCMP0 to IVCMP2	Input	Analog voltage input pin
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
OPAMP	AMP0+ to AMP3+	Input	Analog voltage input pins
	AMP0- to AMP3-	Input	Analog voltage input pins
	AMP0O to AMP3O	Output	Analog voltage output pins
CTSU	TS00 to TS22, TS25 to TS29	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
KINT	KR00 to KR07	Input	Key interrupt input pins
I/O ports	P000 to P004, P010 to P015	I/O	General-purpose input/output pins
	P100 to P113	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.8 show the pin assignments.

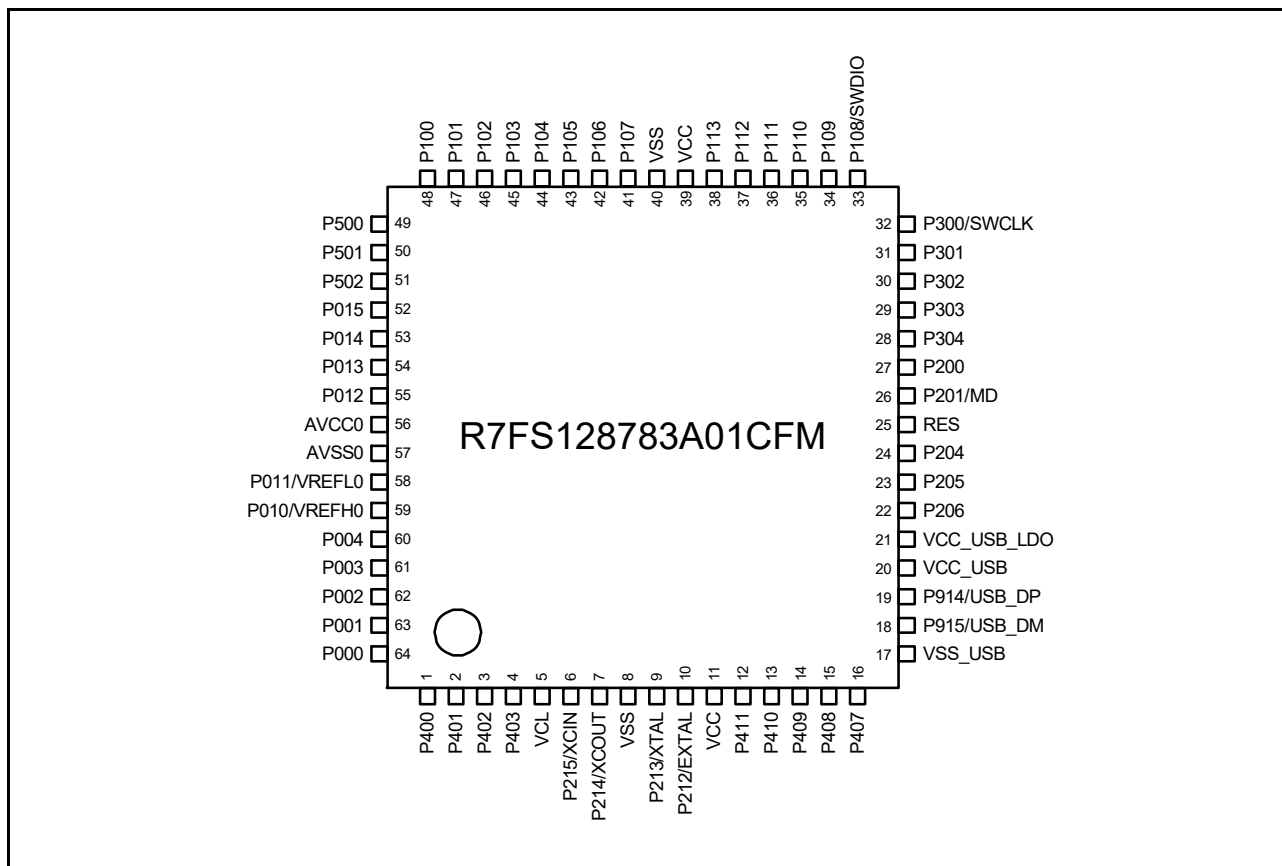


Figure 1.3 Pin assignment for LQFP 64-pin

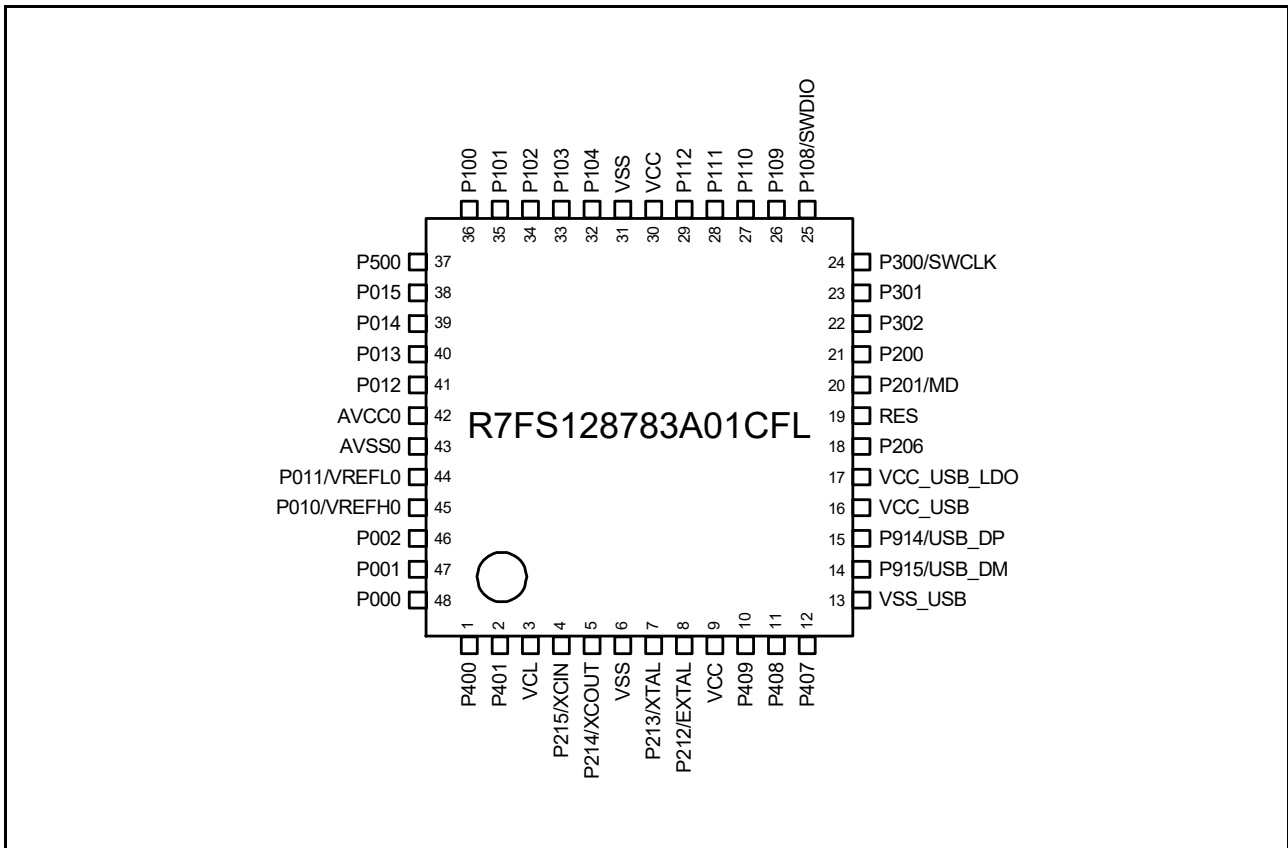


Figure 1.4 Pin assignment for LQFP 48-pin

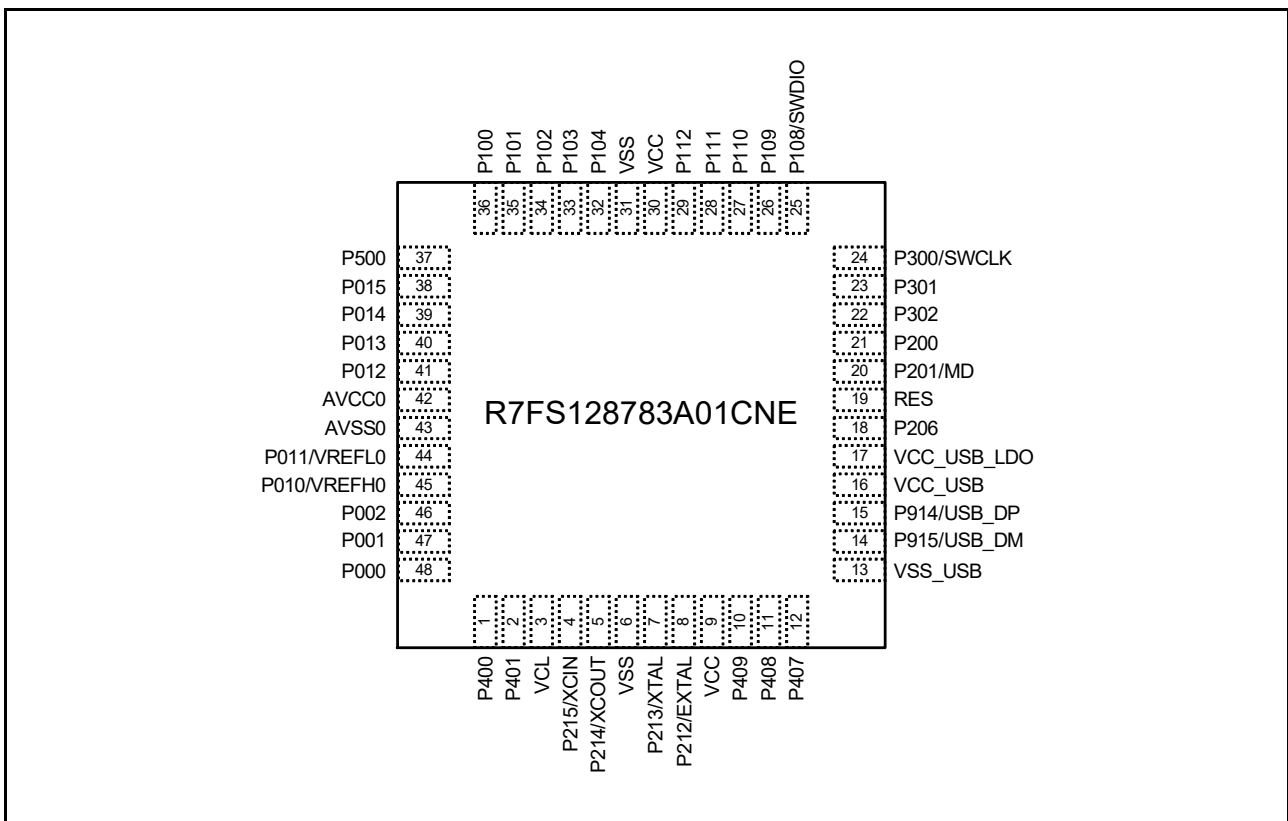


Figure 1.5 Pin assignment for QFN 48-pin

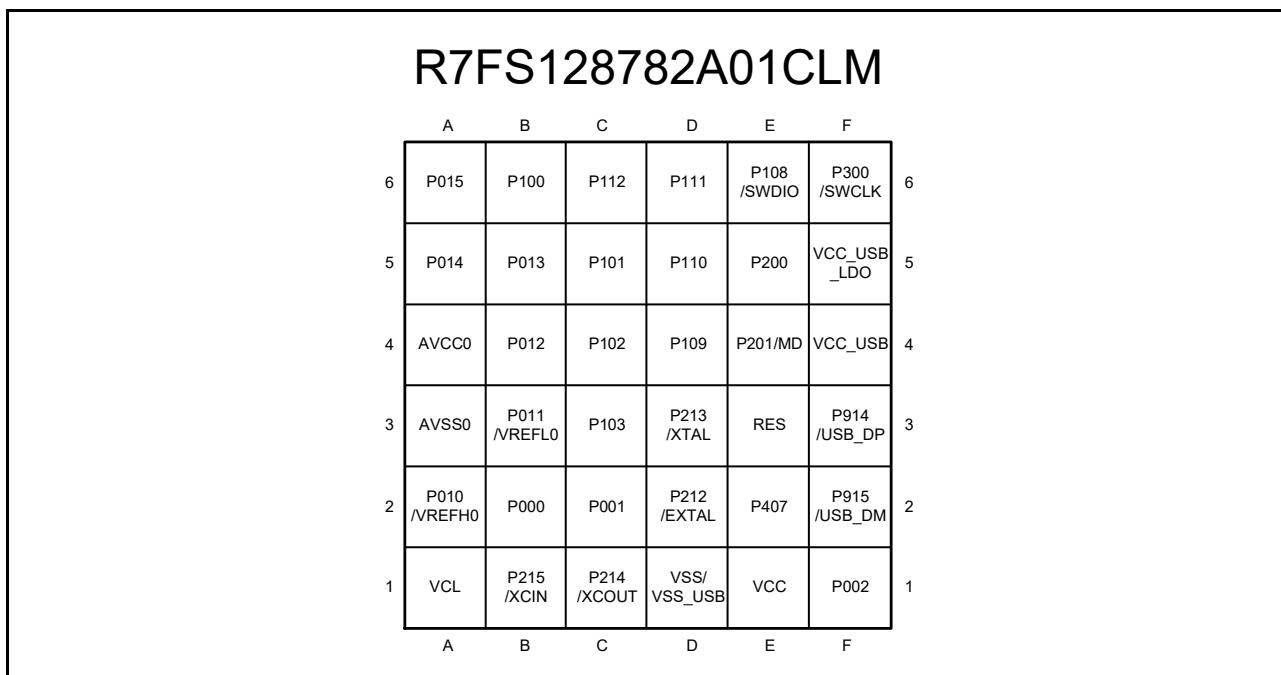


Figure 1.6 Pin assignment for LGA 36-pin (top view, pad side down)

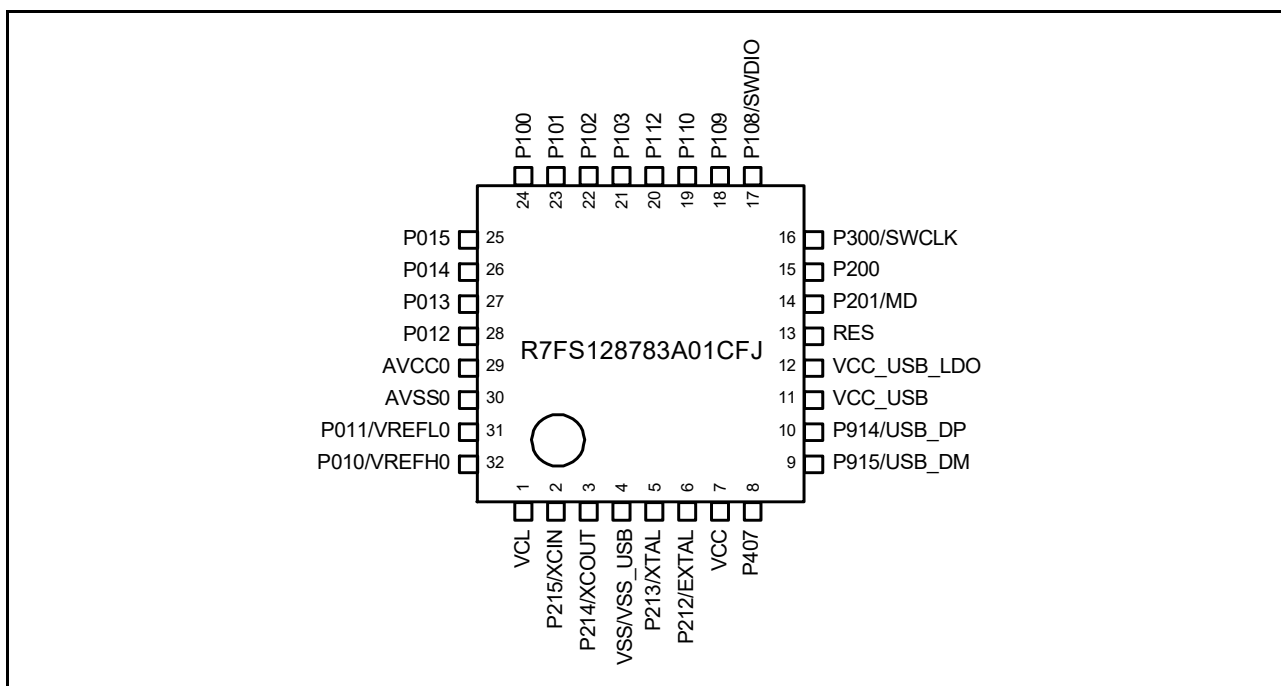


Figure 1.7 Pin assignment for LQFP 32-pin

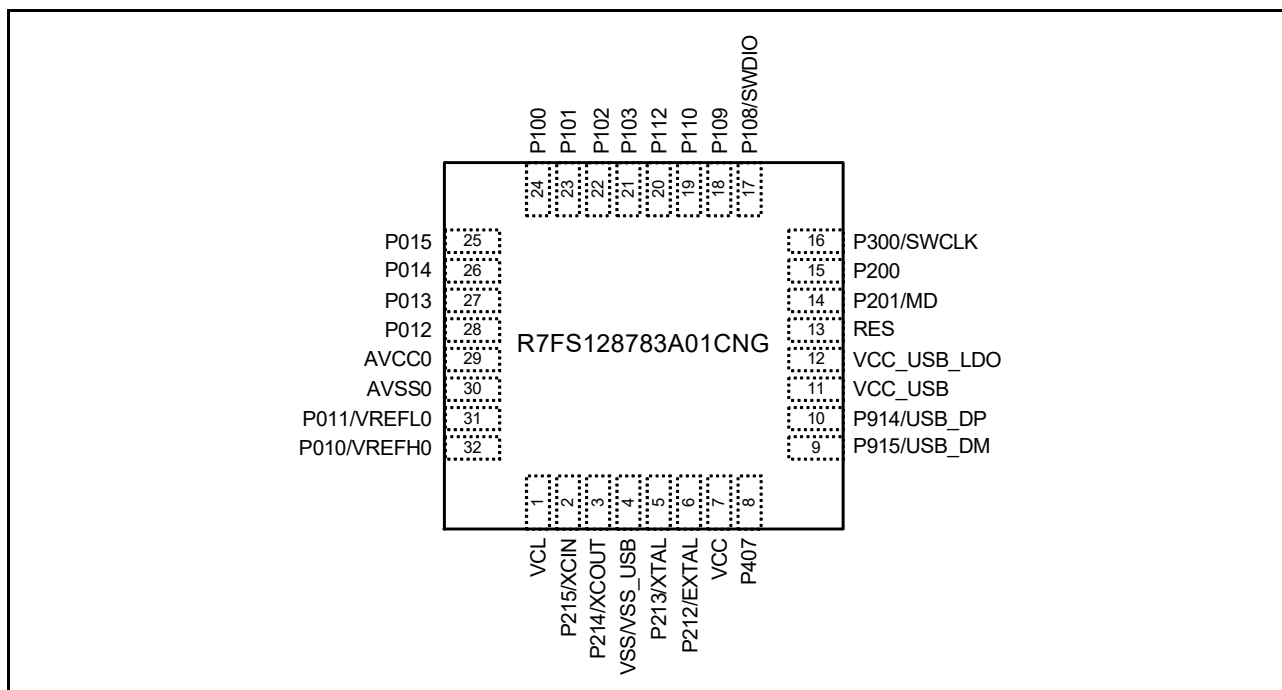


Figure 1.8 Pin assignment for QFN 32-pin

1.7 Pin Lists

Pin number						Power, System, Clock, Debug, CAC	IO ports	Timers				Communication Interfaces				Analog				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32			AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN, DALI	SCI	IIC	SPI	ADC14	DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
1	1	1	-	-	-	CACREF_C	P400	AGTIO1_D		GTIOC6A_A			SCK0_B/ SCK1_B	SCL0_A					TS20	IRQ0	
2	2	2	-	-	-		P401		GTETRGA_B	GTIOC6B_A			CTX0_B	CTS0_RTS0_B/SS0_B/ TXD1_B/ MOSI1_B/ SDA1_B	SDA0_A				TS19	IRQ5	
3	-	-	-	-	-		P402			GTIOC3B_B			CRX0_B	RXD1_B/ MISO1_B/ SCL1_B					TS18	IRQ4	
4	-	-	-	-	-		P403			GTIOC3A_B				CTS1_RTS1_B/SS1_B					TS17		
5	3	3	A1	1	1	VCL															
6	4	4	B1	2	2	XCIN	P215														
7	5	5	C1	3	3	XCOUT	P214														
8	6	6	D1	4	4	VSS															
9	7	7	D3	5	5	XTAL	P213		GTETRGA_D	GTIOC0A_D				TXD1_A/ MOSI1_A/ SDA1_A						IRQ2	
10	8	8	D2	6	6	EXTAL	P212	AGTEE1	GTETRGA_D	GTIOC0B_D				RXD1_A/ MISO1_A/ SCL1_A						IRQ3	
11	9	9	E1	7	7	VCC															
12	-	-	-	-	-		P411	AGTOA1	GTOVUP_B	GTIOC6A_B				TXD0_B/ MOSI0_B/ SDA0_B			MOSIA_B		TS07	IRQ4	
13	-	-	-	-	-		P410	AGTOB1	GTOVLO_B	GTIOC6B_B				RXD0_B/ MISO0_B/ SCL0_B			MISOA_B		TS06	IRQ5	
14	10	10	-	-	-		P409		GTOVUP_B	GTIOC5A_B				TXD0_E/ MOSI0_E/ SDA0_E/ TXD9_A/ MOSI9_A/ SDA9_A				TS05	IRQ6		
15	11	11	-	-	-		P408		GTOVLO_B	GTIOC5B_B				RXD9_A/ MISO9_A/ SCL9_A	SCL0_C				TS04	IRQ7	
16	12	12	E2	8	8		P407	AGTIO0_C		GTIOC0A_E	RTC OUT	USB_VBUS	CTS0_RTS0_D/SS0_D	SDA0_B	SSLB3_A	ADTRG0_B			TS03		
17	13	13	D1	4	4	VSS_USB															
18	14	14	F2	9	9		P915						USB_DM								
19	15	15	F3	10	10		P914						USB_DP								
20	16	16	F4	11	11	VCC_USB															
21	17	17	F5	12	12	VCC_USB_LDO															
22	18	18	-	-	-		P206		GTIU_A					RXD0_D/ MISO0_D/ SCL0_D	SDA1_A	SSLB1_A			TS01	IRQ0	
23	-	-	-	-	-	CLKOUT_A	P205	AGTO1	GTIV_A	GTIOC4A_B				TXD0_D/ MOSI0_D/ SDA0_D/ CTS9_RTS9_A/SS9_A	SCL1_A	SSLB0_A			TSCAP_A	IRQ1	
24	-	-	-	-	-	CACREF_A	P204	AGTIO1_A	GTIV_A	GTIOC4B_B				SCK0_D/ SCK9_A	SCL0_B	RSPCKB_A			TS00		
25	19	19	E3	13	13	RES															
26	20	20	E4	14	14	MD	P201														
27	21	21	E5	15	15		P200													NMI	
28	-	-	-	-	-		P304			GTIOC1A_B											
29	-	-	-	-	-		P303			GTIOC1B_B									TS02		
30	22	22	-	-	-		P302		GTOUUP_A	GTIOC4A_A					SSLB3_B				TS08	IRQ5	
31	23	23	-	-	-		P301	AGTIO0_D	GTOULO_A	GTIOC4B_A				CTS9_RTS9_D/SS9_D		SSLB2_B			TS09	IRQ6	
32	24	24	F6	16	16	SWCLK	P300		GTOUUP_C	GTIOC0A_A					SSLB1_B						
33	25	25	E6	17	17	SWDIO	P108		GTOULO_C	GTIOC0B_A				CTS9_RTS9_B/SS9_B		SSLB0_B					
34	26	26	D4	18	18	CLKOUT_B	P109		GTOVUP_A	GTIOC1A_A			CTX0_A	SCK1_E/ TXD9_B/ MOSI9_B/ SDA9_B		MOSIB_B			TS10		

Pin number						Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analog				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32			AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN, DALI	SCI	IC	BPI	ADC14	DAC8	ACMPHS, ACMPPL	OPAMP	TSU	Interrupt
35	27	27	D5	19	19		P110	GTOVLO_A	GTIOC1B_A		CRX0_A	CTS0_RTS0_C/ SS0_C/ RXD0_B/ MISO0_B/ SCL9_B		MISOB_B		VCCOUT		TS11	IRQ3		
36	28	28	D6	-	-		P111	AGTOA0	GTIOC3A_A					RSPCKB_B				TS12	IRQ4		
37	29	29	C6	20	20		P112	AGTOB0	GTIOC3B_A					SSLB0_C				TSCAP_C			
38	-	-	-	-	-		P113		GTIOC2A_C												
39	30	30	-	-	-	VCC															
40	31	31	-	-	-	VSS															
41	-	-	-	-	-		P107		GTIOC0A_B										KR07		
42	-	-	-	-	-		P106		GTIOC0B_B					SSLA3_A	AN016				KR06		
43	-	-	-	-	-		P105	GTETRG_A_C	GTIOC1A_C					SSLA2_A	AN017				KR05/ IRQ0		
44	32	32	-	-	-		P104	GTETRGB_B	GTIOC1B_C			RXD0_C/ MISO0_C/ SCL0_C		SSLA1_A	AN018			TS13	KR04/ IRQ1		
45	33	33	C3	21	21		P103	GTOWUP_A	GTIOC2A_A		CTX0_C	CTS0_RTS0_A/ SS0_A		SSLA0_A	AN019	CMPREF1		TS14	KR03		
46	34	34	C4	22	22		P102	AGTO0	GTOWLO_A	GTIOC2B_A	CRX0_C	SCK0_A		RSPCKA_A	AN020/ ADTRG0_A	CMPIN1		TS15	KR02		
47	35	35	C5	23	23		P101	AGTEE0	GTETRGB_A	GTIOC5A_A	DTX0	TXD0_A/ MOSI0_A/ SDA0_A/ CTS1_RTS1_A/ SS1_A	SDA1_B	MOSIA_A	AN021	CMPREF0		TS16	KR01/ IRQ1		
48	36	36	B6	24	24		P100	AGTIO0_A	GTETRG_A_A	GTIOC5B_A	DRX0	RXD0_A/ MISO0_A/ SCL0_A/ SCK1_A	SCL1_B	MISOA_A	AN022	CMPIN0		TS26	KR00/ IRQ2		
49	37	37	-	-	-		P500								AN013	DA1_B		TS27			
50	-	-	-	-	-		P501								AN012			AMP3+			
51	-	-	-	-	-		P502								AN011			AMP3-			
52	38	38	A6	25	25		P015							AN010	DA1_A	IVCMP1	AMP2+	TS28	IRQ7		
53	39	39	A5	26	26		P014							AN009	DA0	IVREF1	AMP2-	TS29			
54	40	40	B5	27	27		P013							AN008		IVCMP0	AMP1+				
55	41	41	B4	28	28		P012							AN007		IVREF0	AMP1-				
56	42	42	A4	29	29	AVCC0															
57	43	43	A3	30	30	AVSS0															
58	44	44	B3	31	31	VREFL0	P011							AN006	DA2_A		AMP20				
59	45	45	A2	32	32	VREFH0	P010							AN005			AMP10				
60	-	-	-	-	-		P004							AN004	DA2_B			TS25	IRQ3		
61	-	-	-	-	-		P003							AN003			AMP30				
62	46	46	F1	-	-		P002							AN002			AMP00		IRQ2		
63	47	47	C2	-	-		P001							AN001		IVREF2	AMP0-	TS22	IRQ7		
64	48	48	B2	-	-		P000							AN000		IVCMP2	AMP0+	TS21	IRQ6		

Note: Several pin names have the added suffix of _A, _B, _C, _D and _E. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

$V_{CC}^{*1} = AVCC0 = VCC_USB^{*2} = VCC_USB_LDO^{*2} = 1.6$ to $5.5V$, $VREFH0 = 1.6$ to $AVCC0$,

$VSS = AVSS0 = VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Note 1. The typical condition is set to $VCC = 3.3V$.

Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

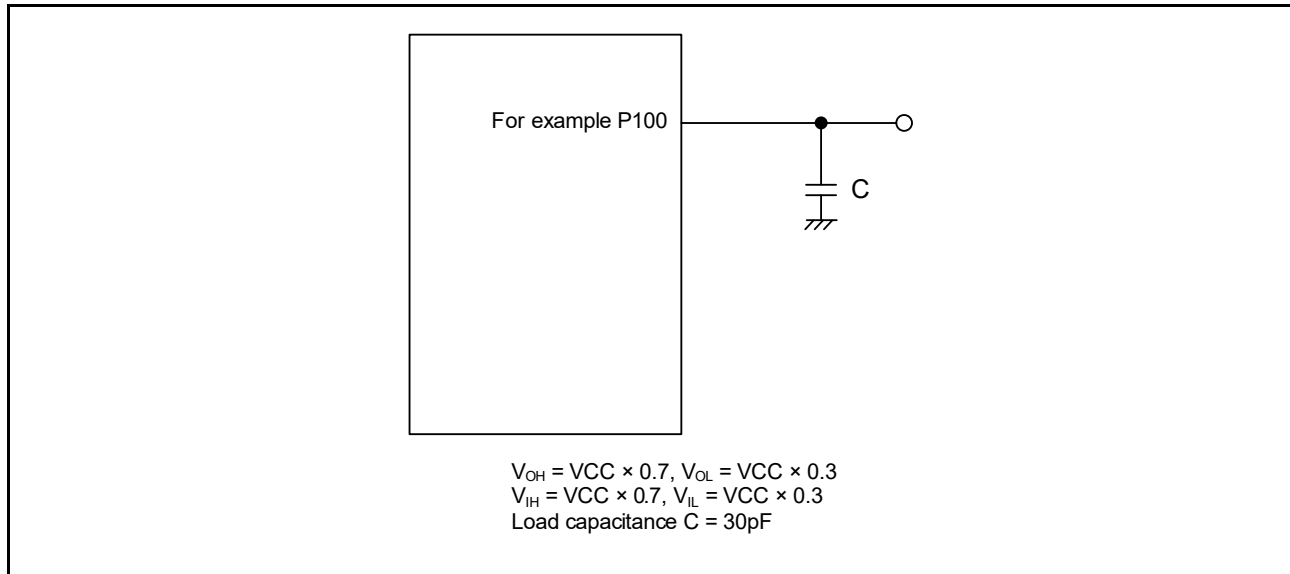


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	-0.5 to +6.5	V
Input voltage	5 V tolerant ports*1	V_{in}	-0.3 to +6.5
	P000 to P004 P010 to P015 P500 to P502	V_{in}	-0.3 to AVCC0 + 0.3
	Others	V_{in}	-0.3 to VCC + 0.3
Reference power supply voltage	VREFH0	-0.3 to +6.5	V
Analog power supply voltage	AVCC0	-0.5 to +6.5	V
USB power supply voltage	VCC_USB	-0.5 to +6.5	V
	VCC_USB_LDO	-0.5 to +6.5	V
Analog input voltage	V_{AN}	When AN000 to AN013 are used	-0.3 to AVCC0 + 0.3
		When AN016 to AN022 are used	-0.3 to VCC + 0.3
Operating temperature*2 *3	T_{opr}	-40 to +85 -40 to +105	°C
Storage temperature	T_{stg}	-55 to +125	°C

Note: Contact Renesas Electronics sales office for information on derating operation under $T_a = +85^{\circ}\text{C}$ to $+105^{\circ}\text{C}$. Derating is the systematic reduction of load for improved reliability.

Note 1. Ports P205, P206, P400, P401, and P407 are 5V-tolerant.

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

Note 2. See [section 2.2.1, Tj/Ta Definition](#).

Note 3. The upper limit of the operating temperature is 85°C or 105°C , depending on the product. For details, see [section 1.3, Part Numbering](#).

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded. To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, and between the VREFH0 and VREFL0 pins. Place capacitors of about $0.1\ \mu\text{F}$ as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance. Connect the VCL pin to a VSS pin by a $4.7\text{-}\mu\text{F}$ capacitor. The capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.6	-	5.5	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
		When USBFS is used USB Regulator Enable	VCC_USB _LDO	-	5.5	V
	VSS	-	0	-	V	
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable	-	VCC	-	V
		When USBFS is used USB Regulator Enable	3.8	-	5.5	V
	VSS_USB	-	0	-	V	
Analog power supply voltages	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	VREFH0	When used as ADC14 Reference	1.6	-	AVCC0	V
	VREFL0		-	0	-	V

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when $VCC \geq 2.2\text{ V}$ and $AVCC0 \geq 2.2\text{ V}$.

$AVCC0 = VCC$ when $VCC < 2.2\text{ V}$ or $AVCC0 < 2.2\text{ V}$.

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T_a) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T _j	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode SubOSC-speed mode
			105*1		

Note: Make sure that $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$, where total power consumption = $(V_{CC} - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times V_{CC}$.

Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see [section 1.3, Part Numbering](#). If the part number shows an operation temperature to 85°C, then T_j max is 105°C, otherwise, it is 125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1)

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (except for SMBus)*1	V _{IH}	VCC × 0.7	-	5.8	V	-
		V _{IL}	-	-	VCC × 0.3		
		ΔV _T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V _{IH}	VCC × 0.8	-	-		
		V _{IL}	-	-	VCC × 0.2		
		ΔV _T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V _{IH}	2.2	-	-	-	VCC = 3.6 to 5.5 V
		V _{IH}	2.0	-	-		VCC = 2.7 to 3.6 V
		V _{IL}	-	-	0.8		
	5V-tolerant ports*3	V _{IH}	VCC × 0.8	-	5.8		
		V _{IL}	-	-	VCC × 0.2		
	P000 to P004 P010 to P015 P500 to P502	V _{IH}	AVCC0 × 0.8	-	-		
		V _{IL}	-	-	AVCC0 × 0.2		
	P914, P915	V _{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V _{IL}	-	-	VCC_USB × 0.2		
	EXTAL Input ports pins except for P000 to P004, P010 to P015, P500 to P502, P914, P915	V _{IH}	VCC × 0.8	-	-		
		V _{IL}	-	-	VCC × 0.2		

Note 1. SCL0_A, SDA0_A, SDA0_B, SCL1_A, SDA1_A (total 5 pins)

Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL0_C, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 9 pins)

Note 3. P205, P206, P400, P401, P407 (total 5pins)

Table 2.5 I/O V_{IH} , V_{IL} (2)Conditions: $VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6$ to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	$VCC \times 0.8$	-	-	V	-
		V_{IL}	-	-	$VCC \times 0.2$		
		ΔV_T	$VCC \times 0.01$	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*1	V_{IH}	$VCC \times 0.8$	-	5.8		
		V_{IL}	-	-	$VCC \times 0.2$		
	P000 to P004 P010 to P015 P500 to P502	V_{IH}	$AVCC0 \times 0.8$	-	-		
		V_{IL}	-	-	$AVCC0 \times 0.2$		
	P914, P915	V_{IH}	$VCC_USB \times 0.8$	-	$VCC_USB + 0.3$		
		V_{IL}	-	-	$VCC_USB \times 0.2$		
	EXTAL Input ports pins except for P000 to P004, P010 to P015, P500 to P502, P914, P915	V_{IH}	$VCC \times 0.8$	-	-		
		V_{IL}	-	-	$VCC \times 0.2$		

Note 1. P205, P206, P400, P401, P407 (total 5pins)

2.2.3 I/O I_{OH} , I_{OL} **Table 2.6** I/O I_{OH} , I_{OL} Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LDO} = 1.6$ to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	
Permissible output current (average value per pin)	Ports P000 to P004, P010 to P015, P212, P213, P500 to P502	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P408, P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P914, P915		I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pins*3	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value per pin)	Ports P000 to P004, P010 to P015, P212, P213, P500 to P502	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P408, P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P914, P915		I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pins*3	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value total pins)	Total of ports P000 to P004, P010 to P015, P500 to P502	$\Sigma I_{OH} (max)$	-	-	-30	mA	
		$\Sigma I_{OL} (max)$	-	-	30	mA	
	Total of ports P914, P915	ΣI_{OH}	-	-	-4.0	mA	
		ΣI_{OL}	-	-	4.0	mA	
	Total of all output pin	$\Sigma I_{OH} (max)$	-	-	-60	mA	
		$\Sigma I_{OL} (max)$	-	-	60	mA	

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 μ s.

Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 3. Except for Ports P200, P214, P215, which are input ports.

2.2.4 I/O V_{OH} , V_{OL} , and Other Characteristics**Table 2.7 I/O V_{OH} , V_{OL} (1)**Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LDO} = 4.0$ to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Output voltage	IIC*1, *2	V_{OL}	-	-	0.4	V	$I_{OL} = 3.0$ mA	
		V_{OL}	-	-	0.6		$I_{OL} = 6.0$ mA	
	Ports P408, P409*2, *3	V_{OH}	$V_{CC} - 1.0$	-	-		$I_{OH} = -20.0$ mA	
		V_{OL}	-	-	1.0		$I_{OL} = 20$ mA	
	Ports P000 to P004, P010 to P015, P500 to P502	Low drive	V_{OH}	$AV_{CC0} - 0.8$	-		-	$I_{OH} = -2.0$ mA
			V_{OL}	-	-		0.8	$I_{OL} = 2.0$ mA
		Middle drive	V_{OH}	$AV_{CC0} - 0.8$	-		-	$I_{OH} = -4.0$ mA
			V_{OL}	-	-		0.8	$I_{OL} = 4.0$ mA
	Ports P914, P915	V_{OH}	$V_{CC_USB} - 0.8$	-	-		$I_{OH} = -2.0$ mA	
		V_{OL}	-	-	0.8		$I_{OL} = 2.0$ mA	
	Other output pins*4	Low drive	V_{OH}	$V_{CC} - 0.8$	-		-	$I_{OH} = -2.0$ mA
			V_{OL}	-	-		0.8	$I_{OL} = 2.0$ mA
		Middle drive*5	V_{OH}	$V_{CC} - 0.8$	-		-	$I_{OH} = -4.0$ mA
			V_{OL}	-	-		0.8	$I_{OL} = 4.0$ mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL0_C, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 9 pins).

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 3. Based on characterization data, not tested in production.

Note 4. Except for Ports P200, P214, P215, which are input ports.

Note 5. Except for P212, P213.

Table 2.8 I/O V_{OH} , V_{OL} (2)Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LDO} = 2.7$ to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Output voltage	IIC*1, *2	V_{OL}	-	-	0.4	V	$I_{OL} = 3.0$ mA	
		V_{OL}	-	-	0.6		$I_{OL} = 6.0$ mA	
	Ports P408, P409*2, *3	V_{OH}	$V_{CC} - 1.0$	-	-		$I_{OH} = -20.0$ mA $V_{CC} = 3.3$ V	
		V_{OL}	-	-	1.0		$I_{OL} = 20$ mA $V_{CC} = 3.3$ V	
	Ports P000 to P004, P010 to P015, P500 to P502	Low drive	V_{OH}	$AV_{CC0} - 0.5$	-		-	$I_{OH} = -1.0$ mA
			V_{OL}	-	-		0.5	$I_{OL} = 1.0$ mA
		Middle drive	V_{OH}	$AV_{CC0} - 0.5$	-		-	$I_{OH} = -2.0$ mA
			V_{OL}	-	-		0.5	$I_{OL} = 2.0$ mA
	Ports P914, P915	V_{OH}	$V_{CC_USB} - 0.5$	-	-		$I_{OH} = -1.0$ mA	
		V_{OL}	-	-	0.5		$I_{OL} = 1.0$ mA	
	Other output pins*4	Low drive	V_{OH}	$V_{CC} - 0.5$	-		-	$I_{OH} = -1.0$ mA
			V_{OL}	-	-		0.5	$I_{OL} = 1.0$ mA
		Middle drive*5	V_{OH}	$V_{CC} - 0.5$	-		-	$I_{OH} = -2.0$ mA
			V_{OL}	-	-		0.5	$I_{OL} = 2.0$ mA

Note 1. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL0_C, SCL1_A, SDA1_A, SCL1_B, SDA1_B (total 9 pins).

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.

Note 3. Based on characterization data, not tested in production.

Note 4. Except for Ports P200, P214, P215, which are input ports.

Note 5. Except for P212, P213.

Table 2.9 I/O V_{OH} , V_{OL} (3)

Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LDO} = 1.6$ to 2.7 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010 to P015, P500 to P502	Low drive	V_{OH}	$AV_{CC0} - 0.3$	-	-	V	$I_{OH} = -0.5$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 0.5$ mA
		Middle drive	V_{OH}	$AV_{CC0} - 0.3$	-	-		$I_{OH} = -1.0$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 1.0$ mA
	Ports P914, P915		V_{OH}	$V_{CC_USB} - 0.3$	-	-		$I_{OH} = -0.5$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 0.5$ mA
	Other output pins*1	Low drive	V_{OH}	$V_{CC} - 0.3$	-	-		$I_{OH} = -0.5$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 0.5$ mA
		Middle drive*2	V_{OH}	$V_{CC} - 0.3$	-	-		$I_{OH} = -1.0$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 1.0$ mA

Note 1. Except for Ports P200, P214, P215, which are input ports.

Note 2. Except for P212, P213.

Table 2.10 I/O other characteristicsConditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LDO} = 1.6$ to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, Ports P200, P214, P215	$ I_{in} $	-	-	1.0	μA $V_{in} = 0$ V $V_{in} = V_{CC}$
Three-state leakage current (off state)	5V-tolerant ports	$ I_{TS1} $	-	-	1.0	μA $V_{in} = 0$ V $V_{in} = 5.8$ V
	Other ports		-	-	1.0	
Input pull-up resistor	All ports (except for P200, P214, P215, P914, P915)	R_U	10	20	50	$k\Omega$ $V_{in} = 0$ V
Input capacitance	USB_DP, USB_DM, P200	C_{in}	-	-	30	pF $V_{in} = 0$ V $f = 1$ MHz $T_a = 25^\circ C$
	Other input pins		-	-	15	

2.2.5 Output Characteristics for I/O Pins (Low Drive Capacity)

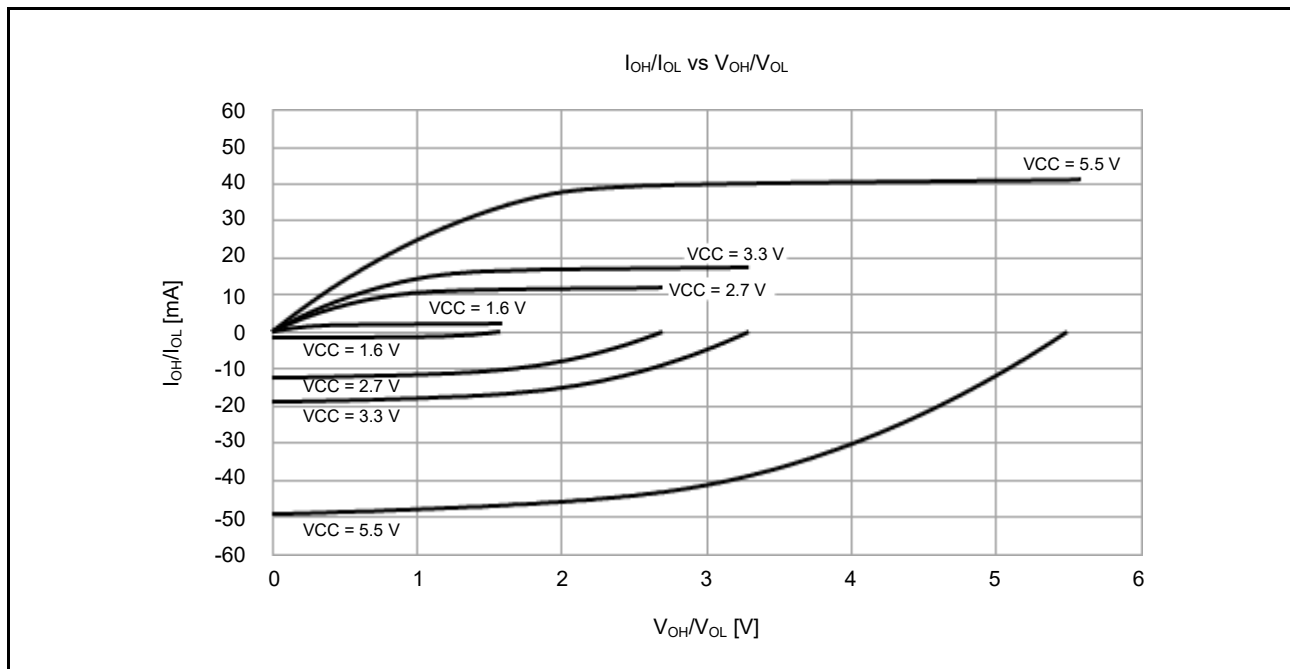


Figure 2.2 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at $T_a = 25^\circ C$ when low drive output is selected (reference data, except for P914 and P915)

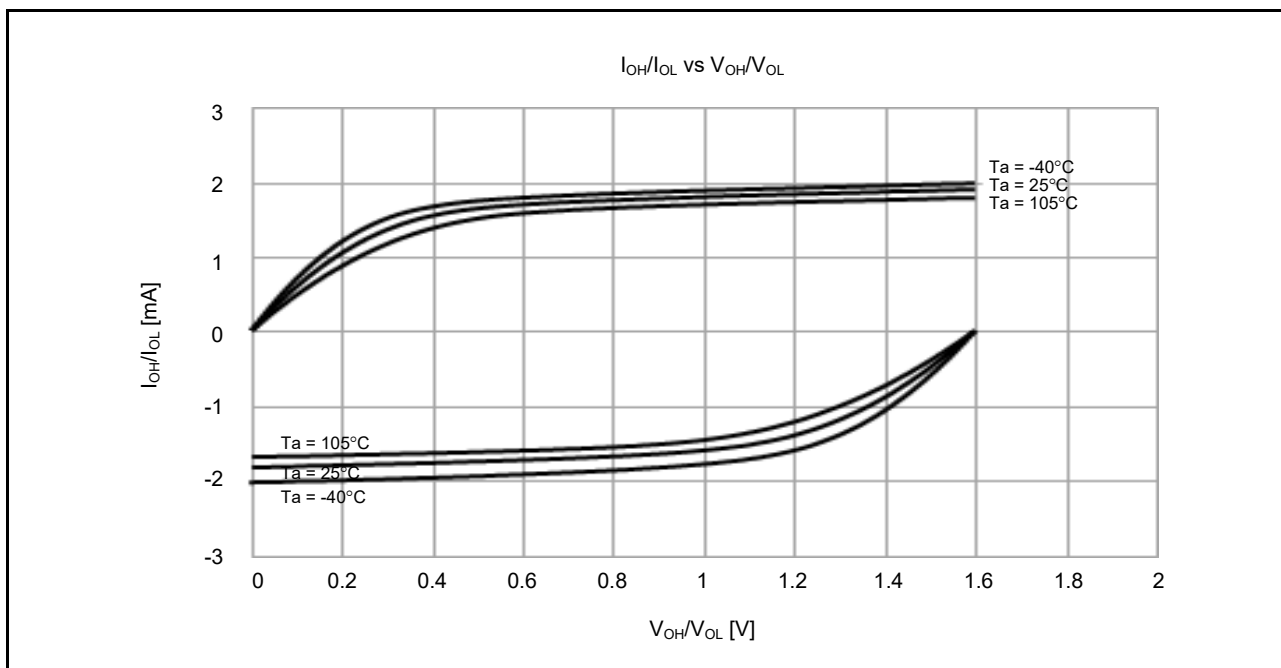


Figure 2.3 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 1.6$ V when low drive output is selected (reference data, except for P914 and P915)

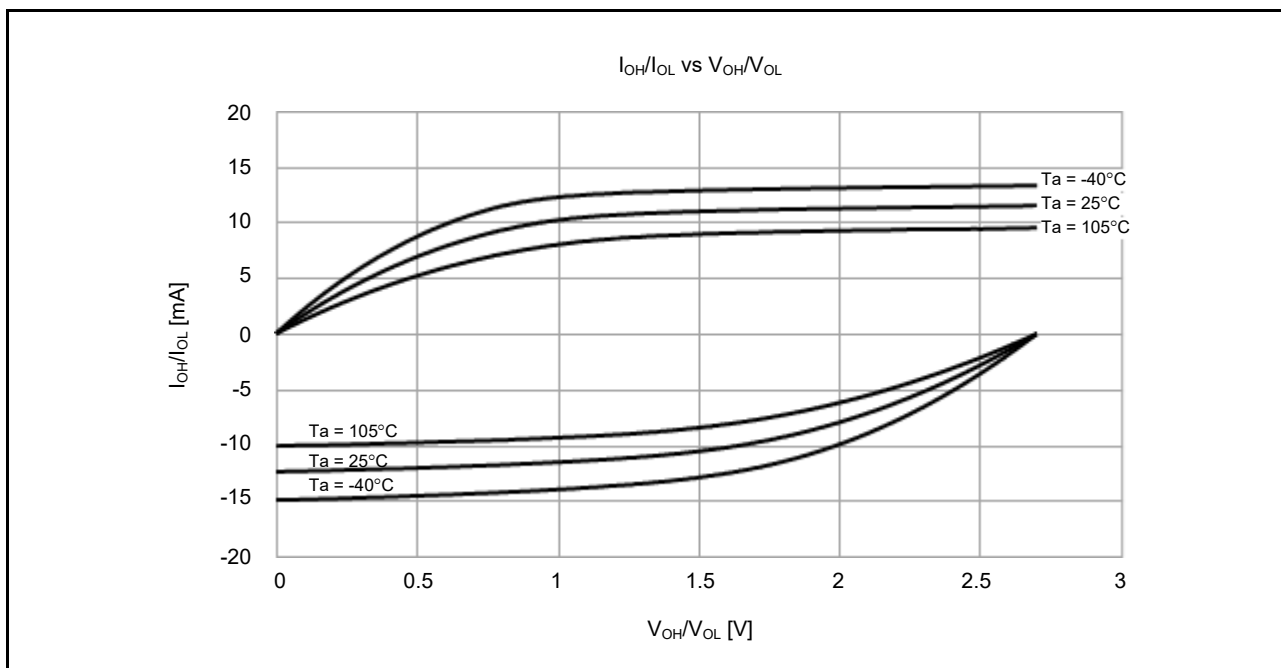


Figure 2.4 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 2.7$ V when low drive output is selected (reference data, except for P914 and P915)

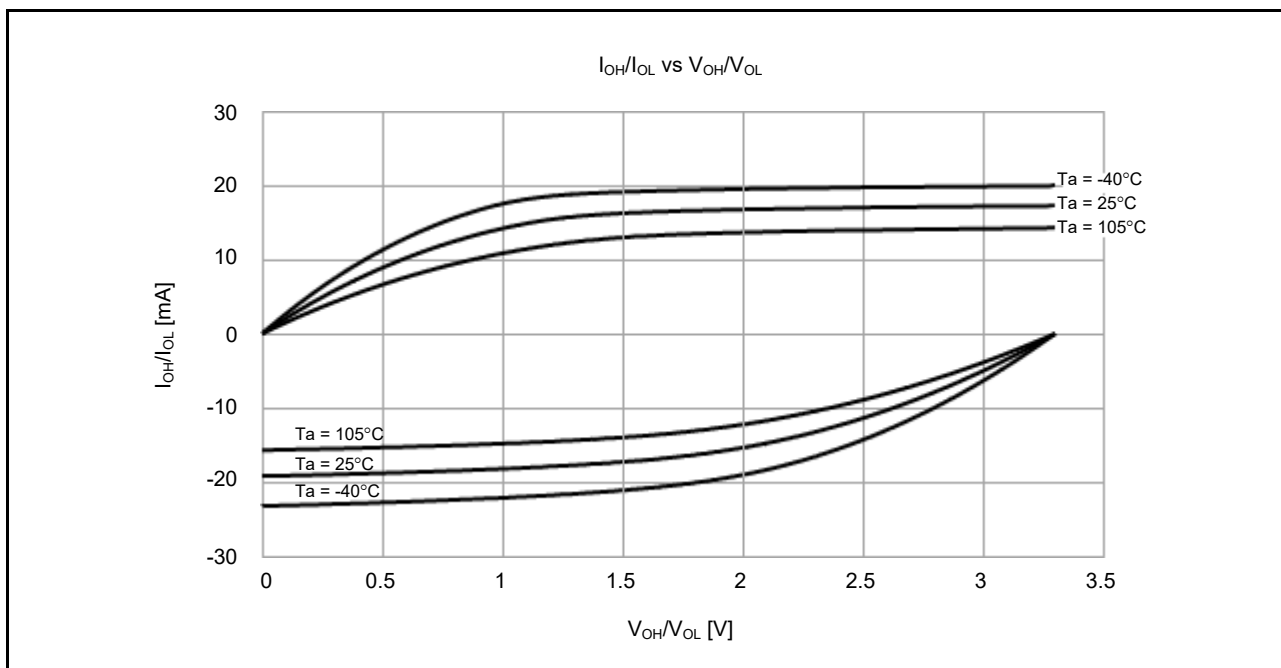


Figure 2.5 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 3.3$ V when low drive output is selected (reference data, except for P914 and P915)

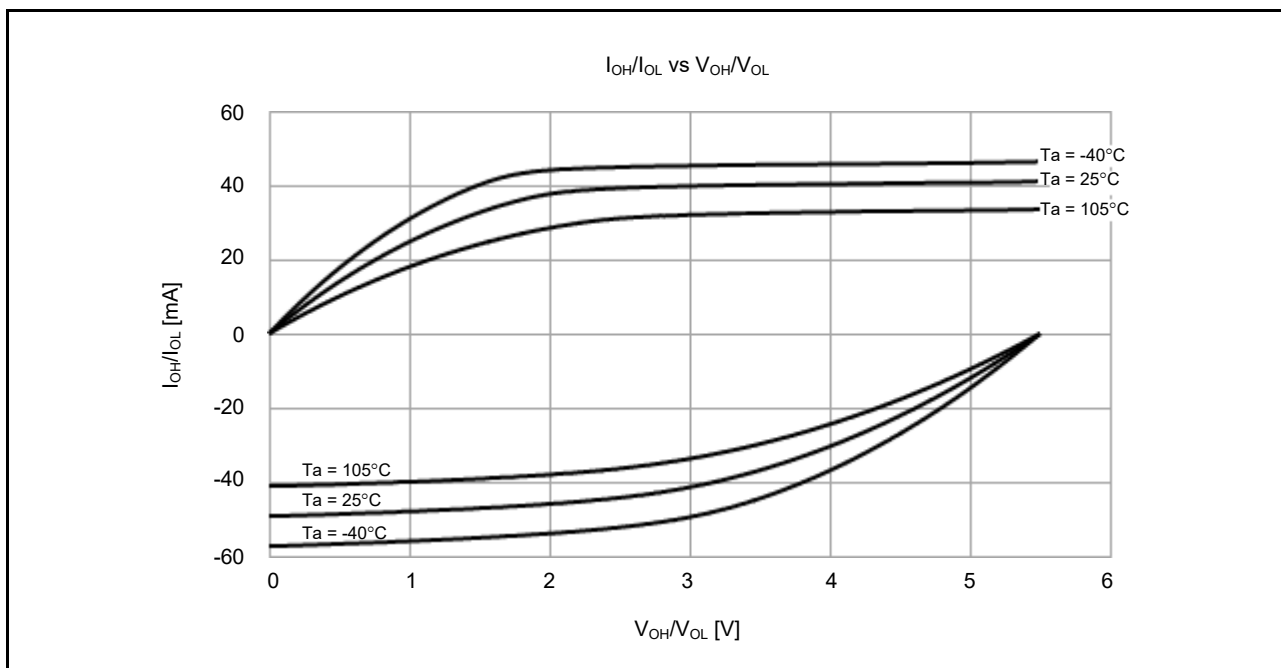


Figure 2.6 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 5.5$ V when low drive output is selected (reference data, except for P914 and P915)

2.2.6 Output Characteristics for I/O Pins (Middle Drive Capacity)

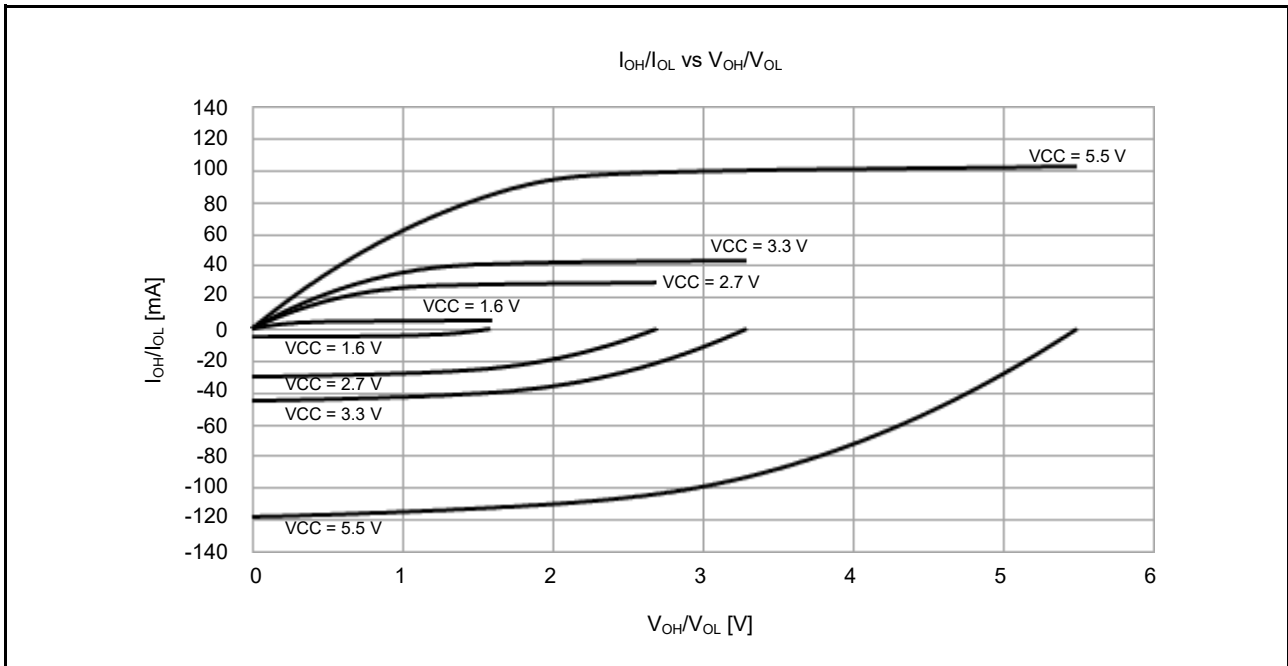


Figure 2.7 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at $T_a = 25^\circ\text{C}$ when middle drive output is selected (reference data, except for P914 and P915)

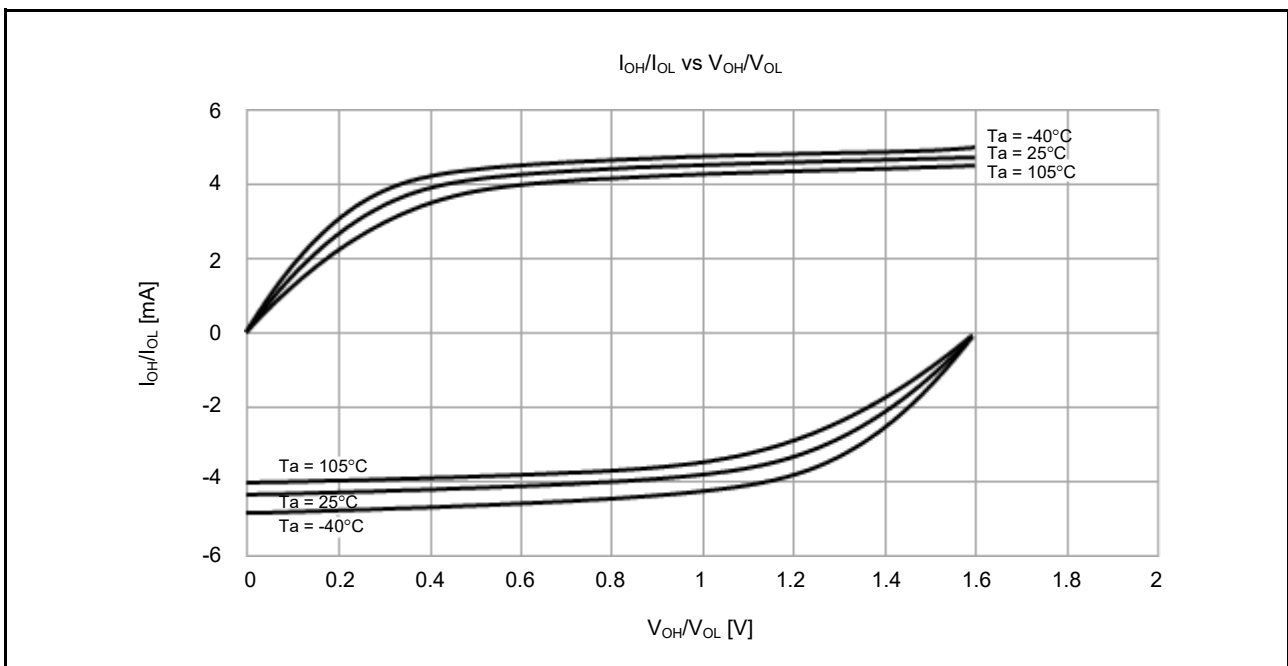


Figure 2.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 1.6\text{ V}$ when middle drive output is selected (reference data, except for P914 and P915)

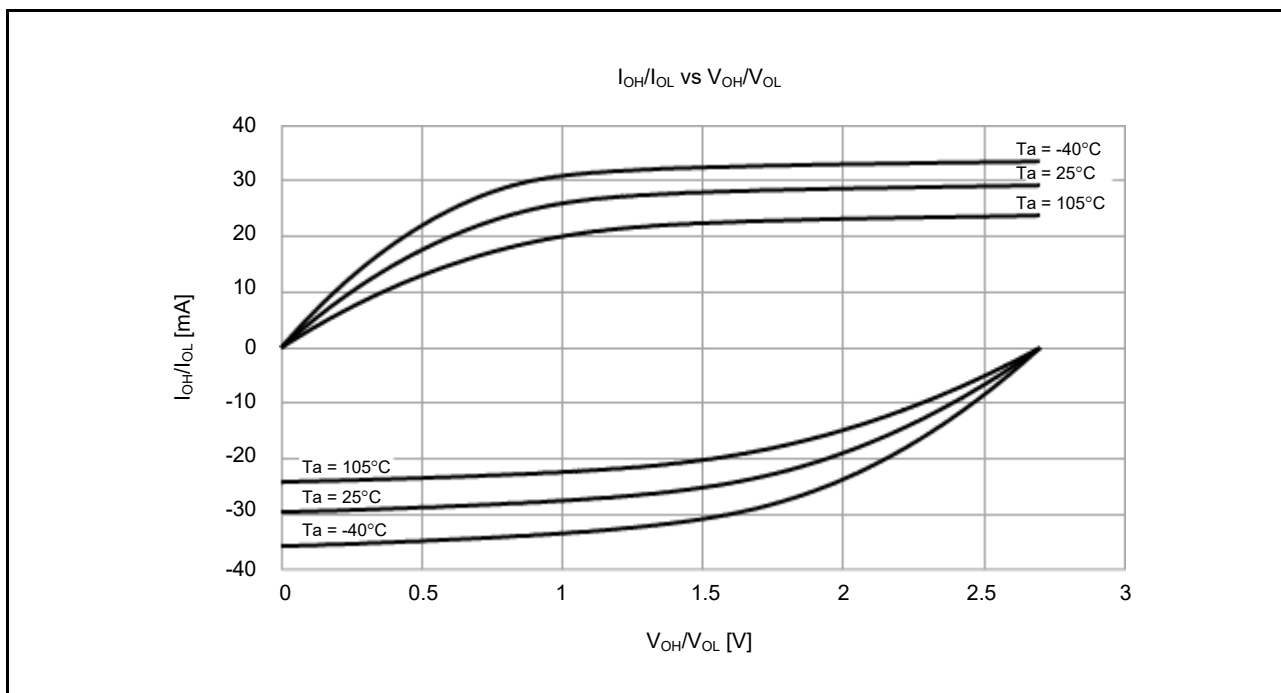


Figure 2.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 2.7$ V when middle drive output is selected (reference data, except for P914 and P915)

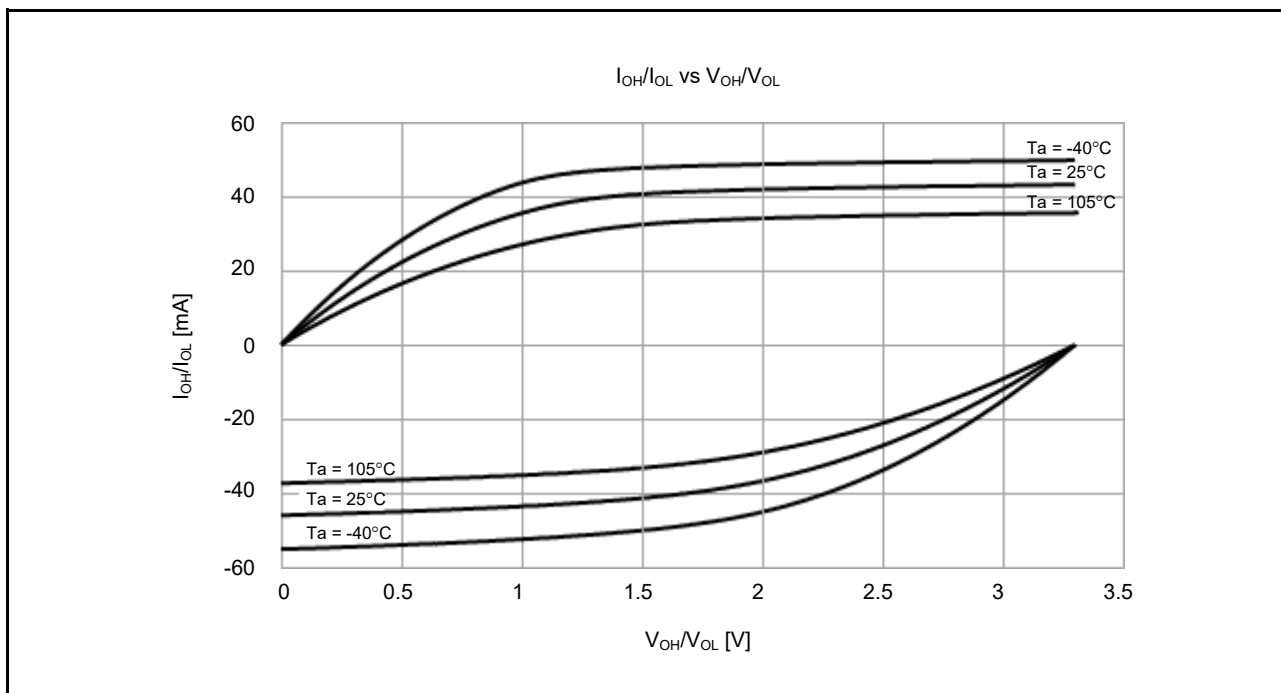


Figure 2.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 3.3$ V when middle drive output is selected (reference data, except for P914 and P915)

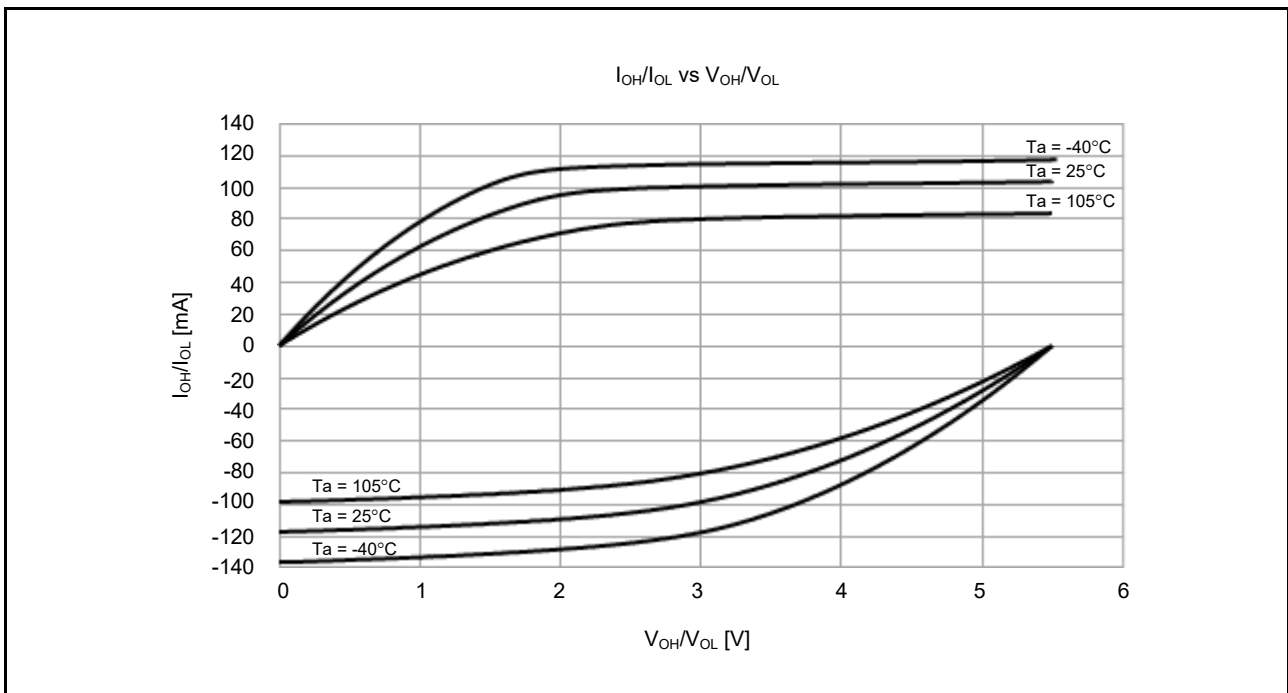


Figure 2.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 5.5$ V when middle drive output is selected (reference data, except for P914 and P915)

2.2.7 Output Characteristics for P408 and P409 I/O Pins (Middle Drive Capacity)

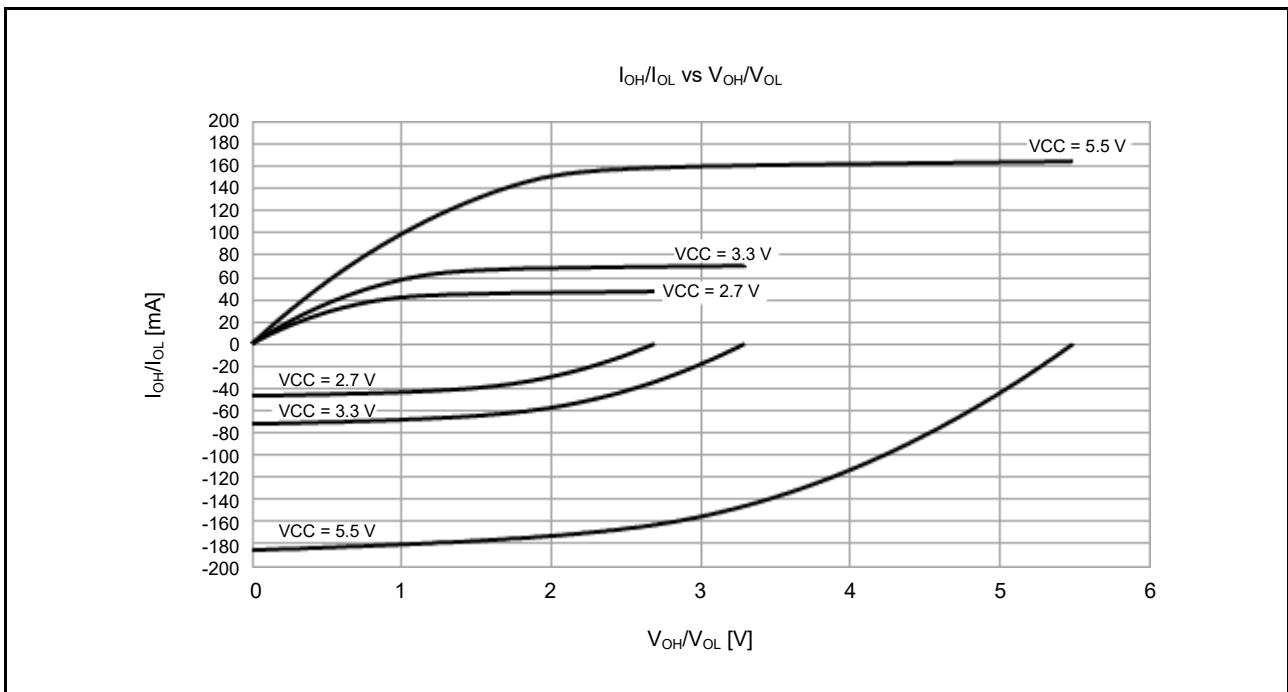


Figure 2.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at $T_a = 25^\circ\text{C}$ when middle drive output is selected (reference data)

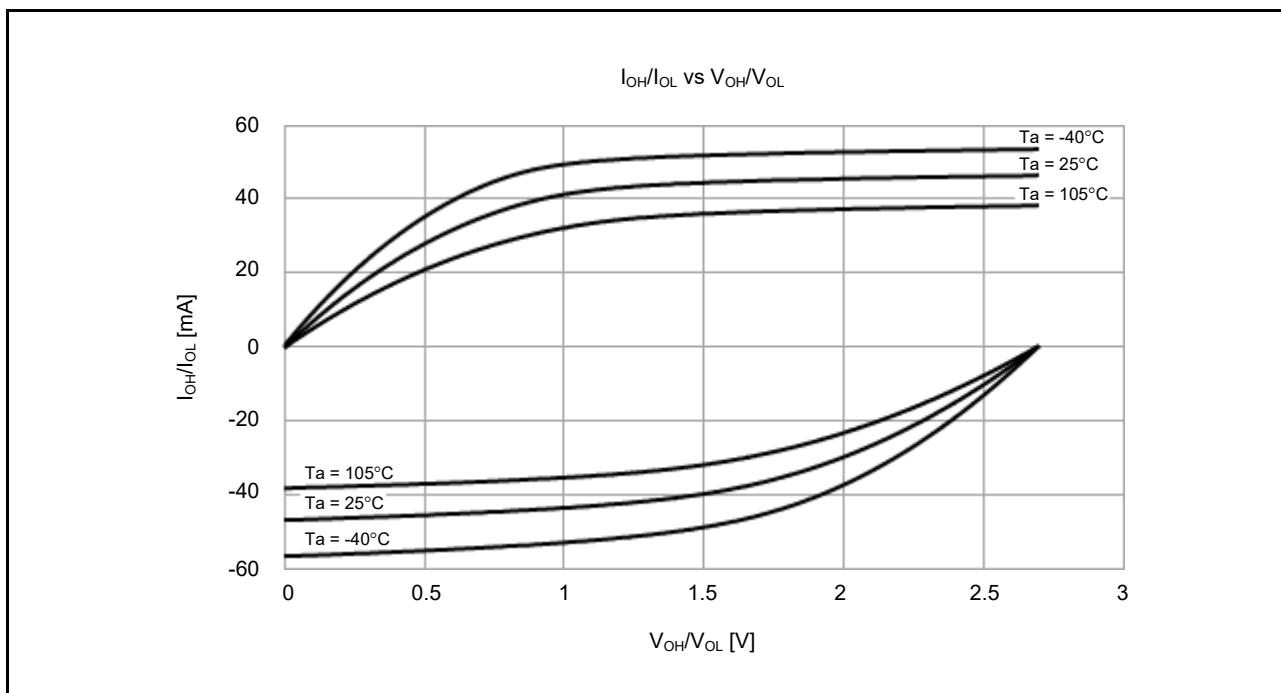


Figure 2.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 2.7$ V when middle drive output is selected (reference data)

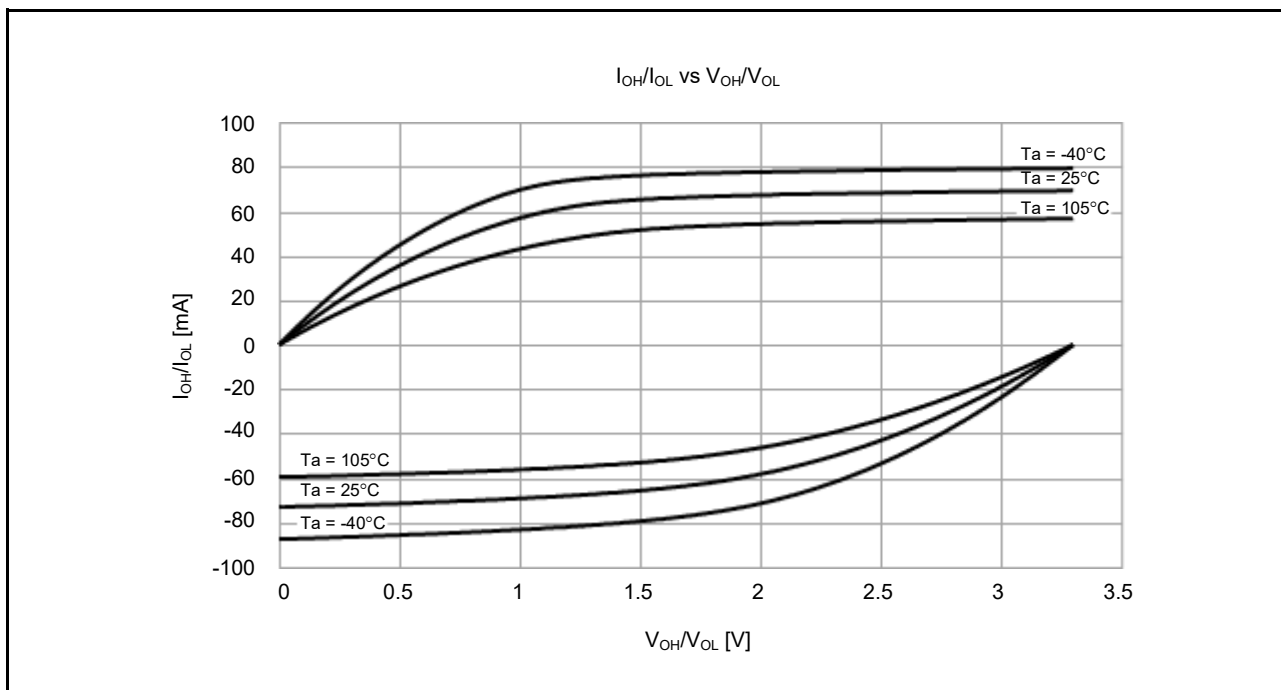


Figure 2.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 3.3$ V when middle drive output is selected (reference data)

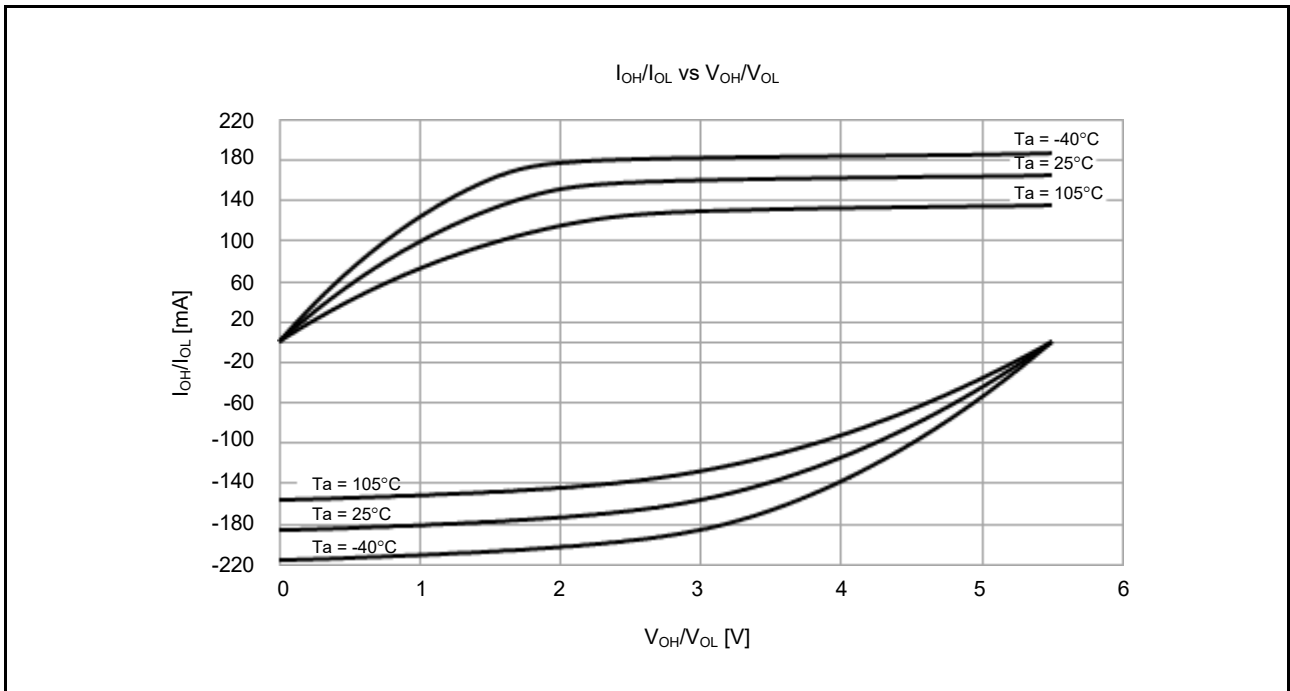


Figure 2.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 5.5$ V when middle drive output is selected (reference data)

2.2.8 Output Characteristics for IIC I/O Pins

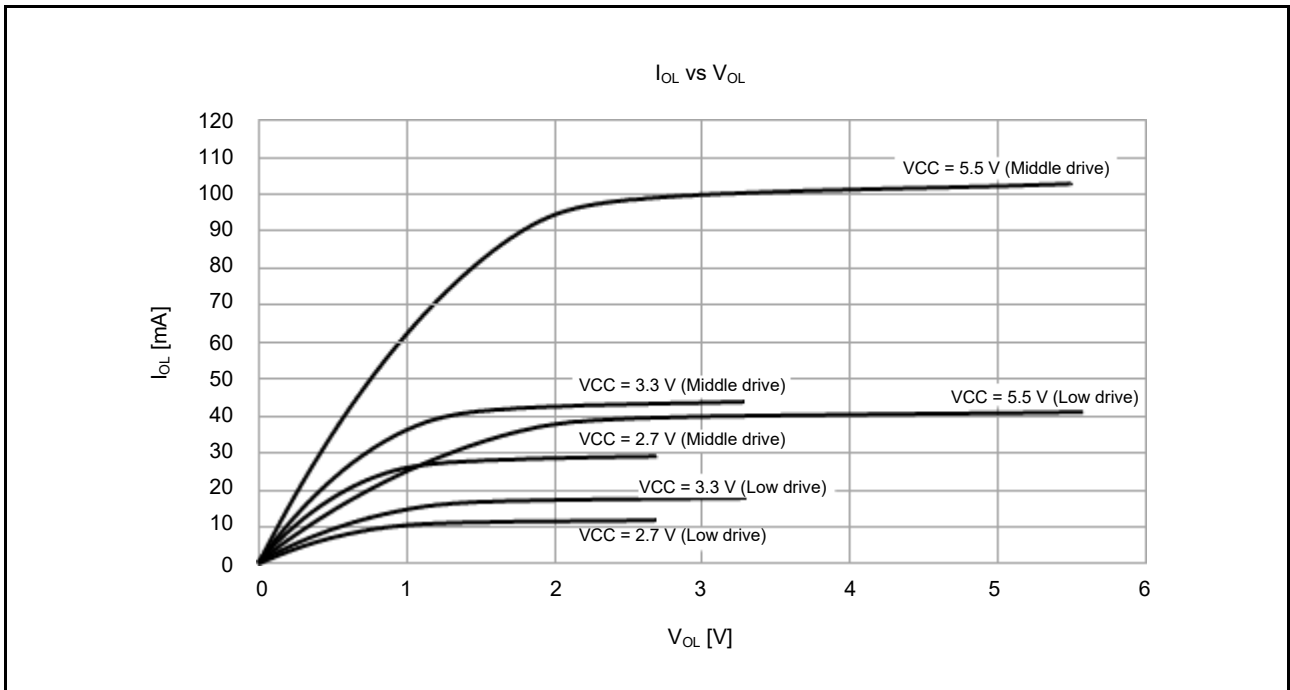


Figure 2.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at $T_a = 25^\circ\text{C}$

2.2.9 Operating and Standby Current

Table 2.11 Operating and standby current (1) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*9	Max	Unit	Test Conditions	
Supply current*1	High-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32 MHz	I _{CC}	4.2	-	mA	*7	
				ICLK = 16 MHz		2.6	-			
				ICLK = 8 MHz		1.8	-			
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 32 MHz		6.2	-			
				ICLK = 16 MHz		3.6	-			
				ICLK = 8 MHz		2.4	-			
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32 MHz		10.5	-			
				ICLK = 16 MHz		5.8	-			
				ICLK = 8 MHz		3.4	-			
		All peripheral clock enabled, code executing from flash*5	ICLK = 32 MHz	-	22.1					
		Sleep mode	All peripheral clock disabled*5	ICLK = 32 MHz	1.6	-	*7			
				ICLK = 16 MHz	1.2	-				
				ICLK = 8 MHz	0.9	-				
	All peripheral clock enabled*5		ICLK = 32 MHz	7.5	-	*8				
			ICLK = 16 MHz	4.1	-					
			ICLK = 8 MHz	2.4	-					
	Increase during BGO operation*6						2.5	-	-	
	Middle-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 12 MHz	I _{CC}	1.9	-	mA	*7	
				ICLK = 8 MHz		1.6	-			
ICLK = 12 MHz				2.7		-				
All peripheral clock disabled, CoreMark code executing from flash*5			ICLK = 8 MHz	2.1		-				
			ICLK = 12 MHz	4.3		-				
			ICLK = 8 MHz	3.1		-				
All peripheral clock enabled, while (1) code executing from flash*5			ICLK = 12 MHz	-		8.1				
Sleep mode		All peripheral clock disabled*5	ICLK = 12 MHz	0.8	-	*7				
			ICLK = 8 MHz	0.8	-					
		All peripheral clock enabled*5	ICLK = 12 MHz	3.0	-	*8				
			ICLK = 8 MHz	2.2	-					
Increase during BGO operation*6						2.5	-		-	
Low-speed mode*3		Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 1 MHz	I _{CC}	0.3	-		mA	*7
	ICLK = 1 MHz			0.4		-				
	ICLK = 1 MHz			0.5		-				
	All peripheral clock disabled, CoreMark code executing from flash*5		ICLK = 1 MHz	-		2.0				
	Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz	0.2	-	*7				
		All peripheral clock enabled*5	ICLK = 1 MHz	0.4	-	*8				

Table 2.11 Operating and standby current (1) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*9	Max	Unit	Test Conditions
Supply current*1	Low-voltage mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 4 MHz	I _{CC}	1.5	-	mA	*7
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		1.7	-		
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 4 MHz		2.3	-		*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 4 MHz		-	4.0		
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz		0.9	-		*7
			All peripheral clock enabled*5	ICLK = 4 MHz		1.7	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz	I _{CC}	5.9	-	μA	*7
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz		13.0	-		*8
			All peripheral clock enabled, code executing from flash*5	ICLK = 32.768 kHz		128.3 (17.8)*10	163.7		
		Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		3.2	-		*7
All peripheral clock enabled*5			ICLK = 32.768 kHz	10.0		-	*8		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The clock source is HOCO.

Note 3. The clock source is MOCO.

Note 4. The clock source is the sub-clock oscillator.

Note 5. This does not include BGO operation.

Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.

Note 7. PCLKB and PCLKD are set to divided by 64.

Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.

Note 9. VCC = 3.3 V.

Note 10. MOCO and DAC is stopped.

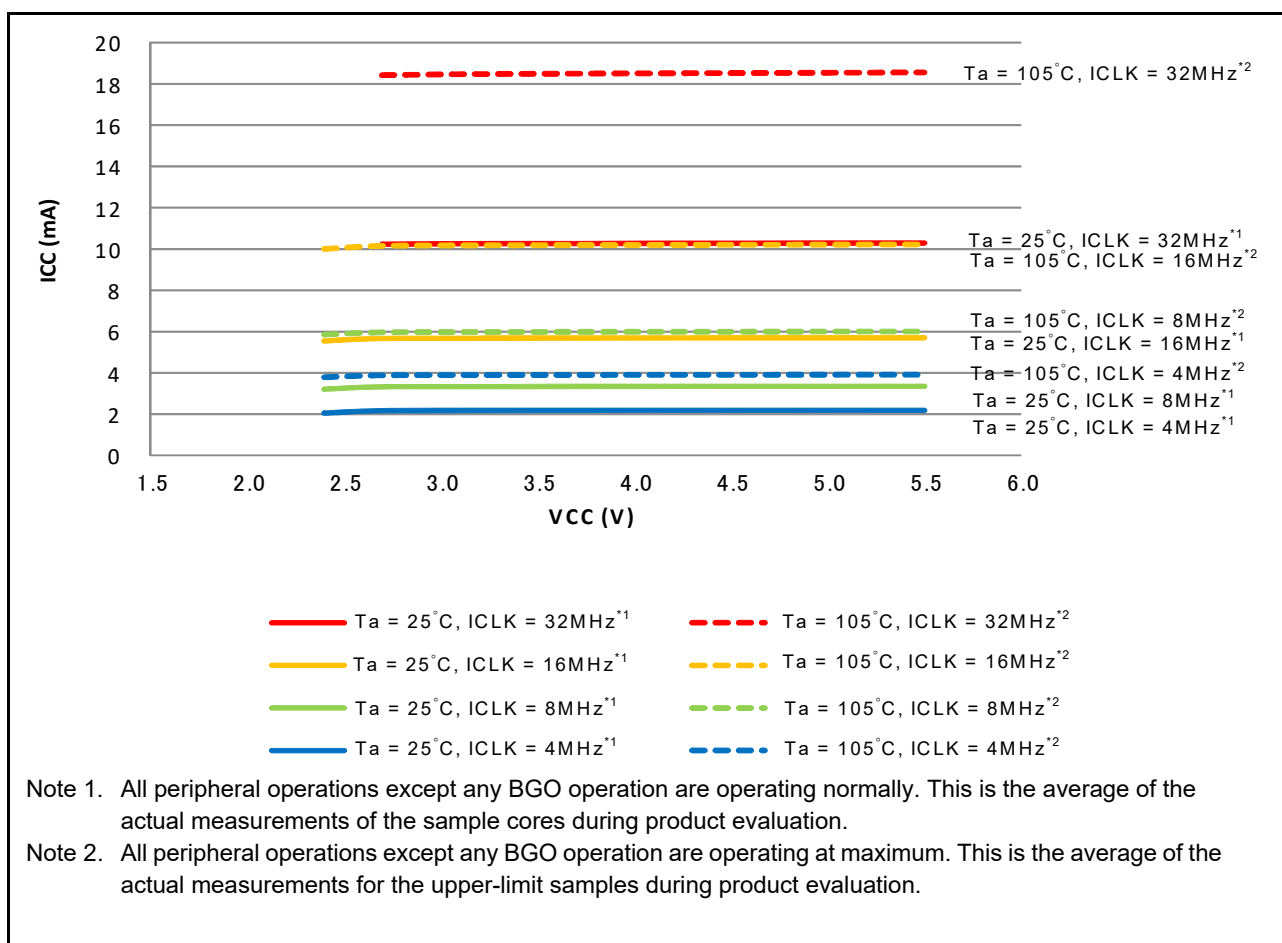


Figure 2.17 Voltage dependency in high-speed mode (reference data)

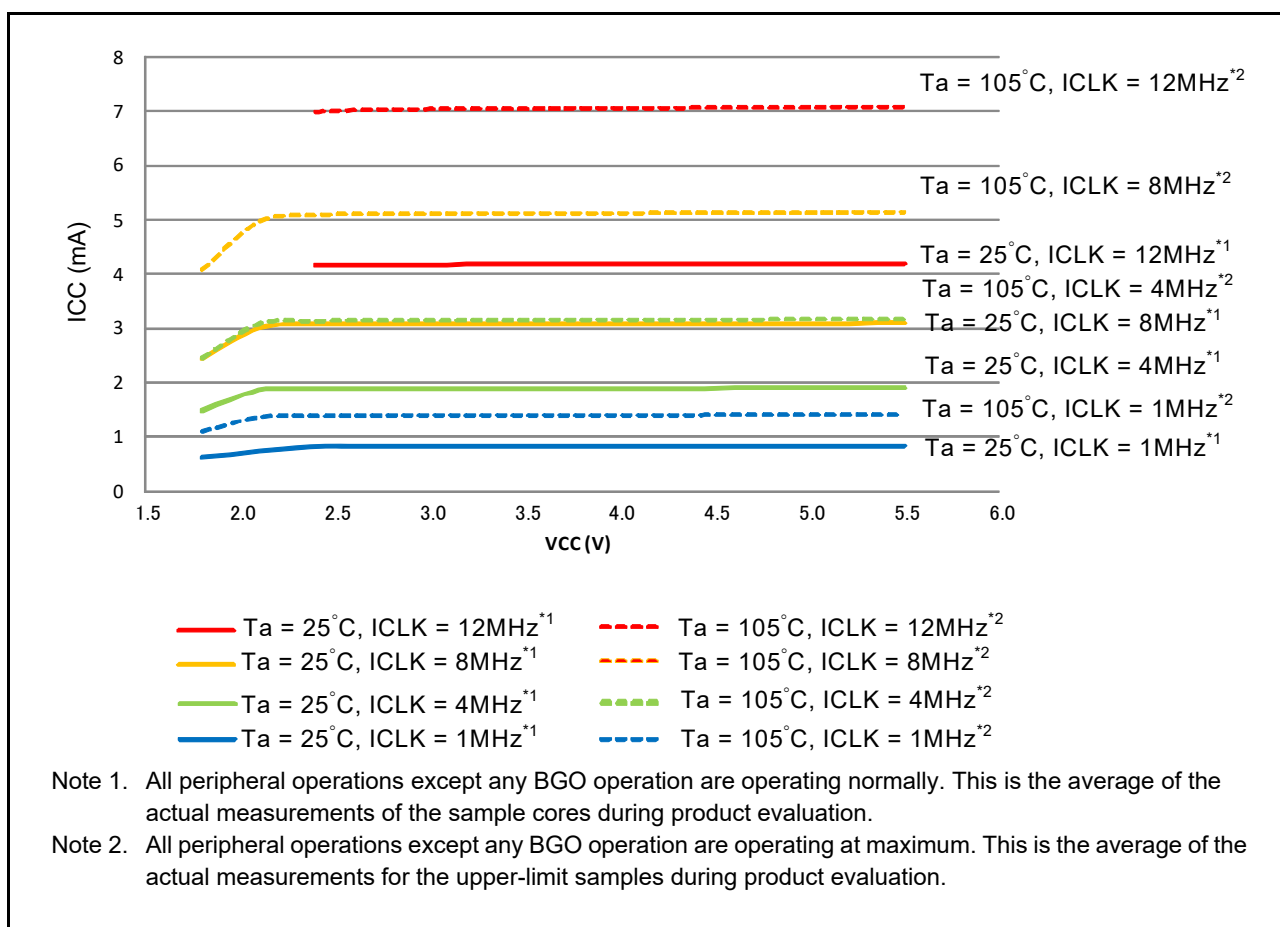


Figure 2.18 Voltage dependency in middle-speed mode (reference data)

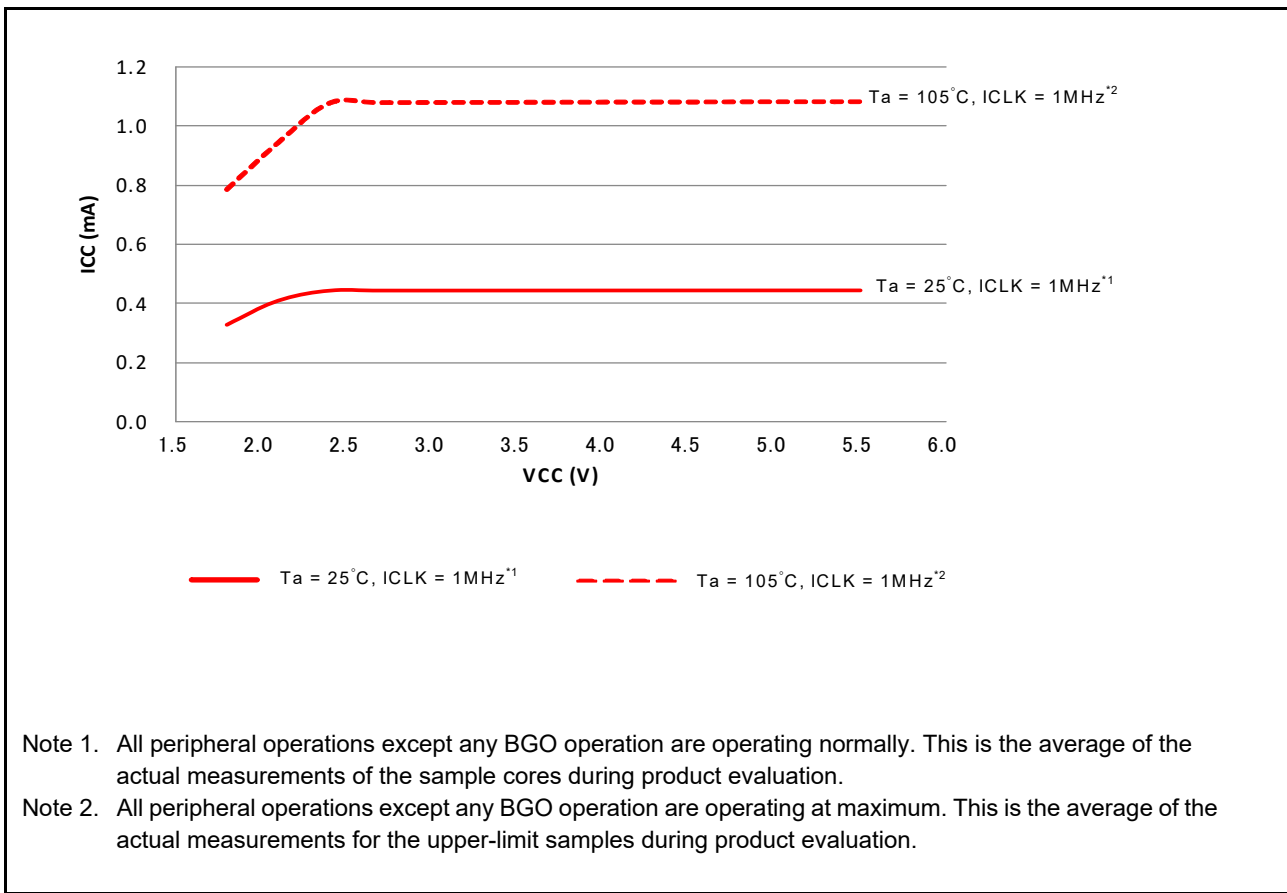


Figure 2.19 Voltage dependency in low-speed mode (reference data)

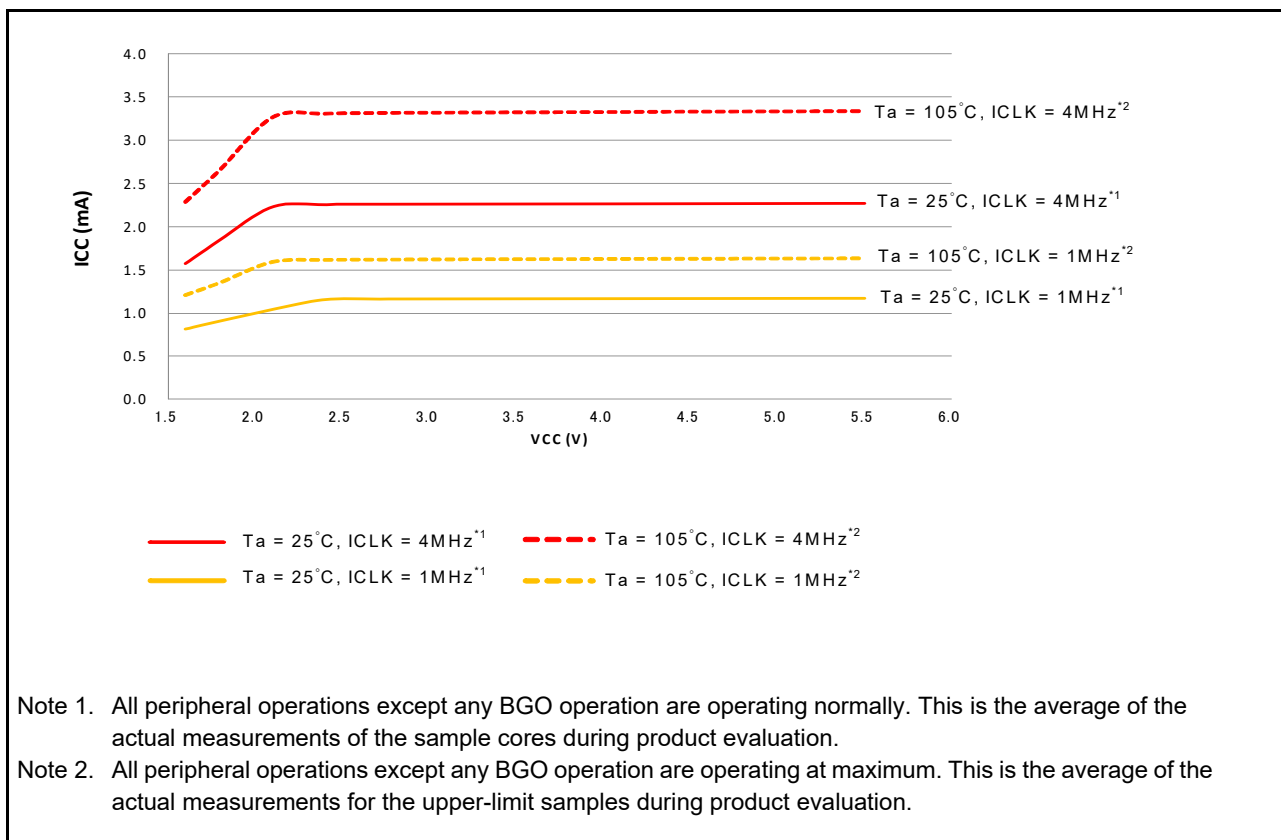


Figure 2.20 Voltage dependency in low-voltage mode (reference data)

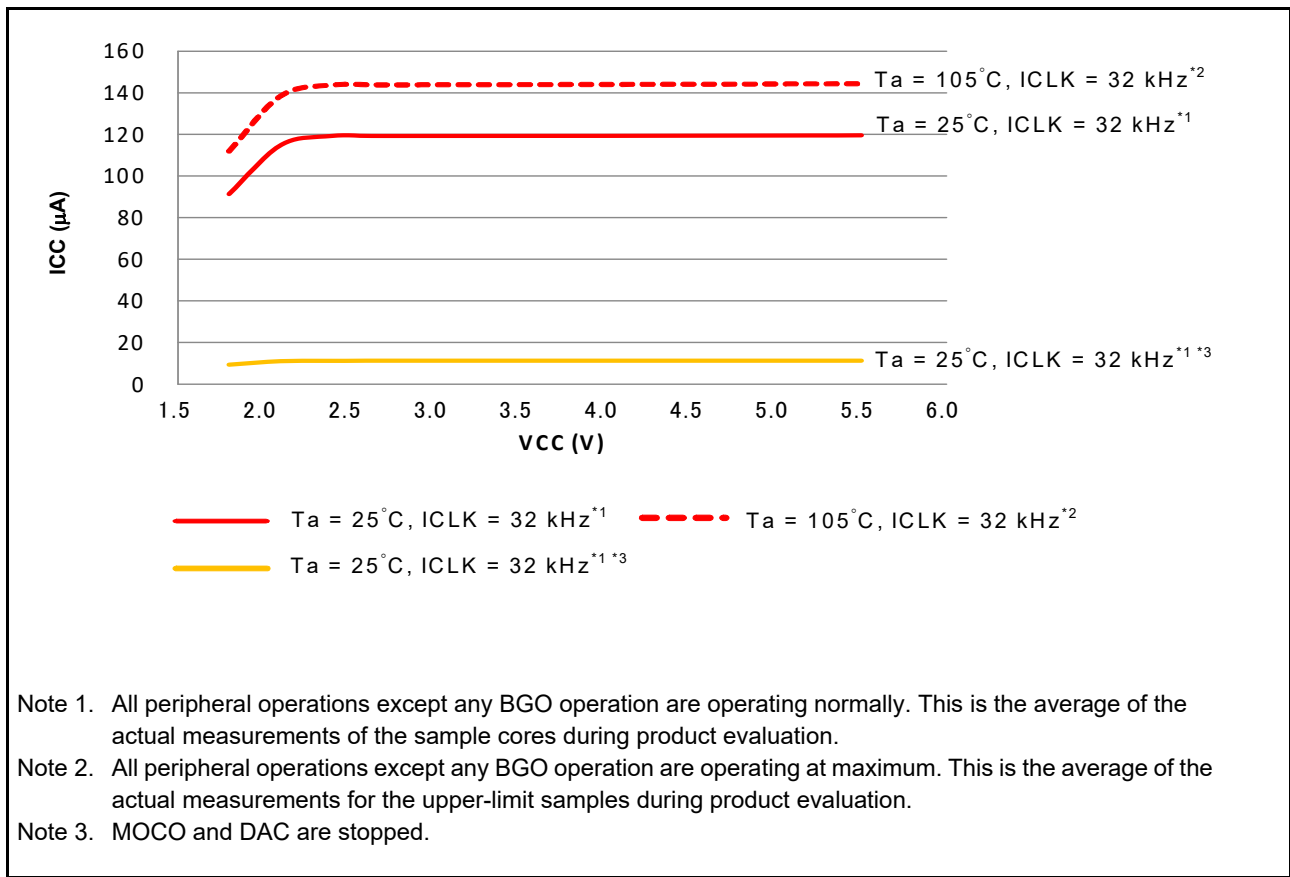


Figure 2.21 Voltage dependency in subosc-speed mode (reference data)

Table 2.12 Operating and standby current (2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Typ ^{*3}	Max	Unit	Test conditions	
Supply current ^{*1}	Software Standby mode ^{*2}	I _{CC}	T _a = 25°C	0.5	2.0	µA	-
			T _a = 55°C	0.8	7.0		
			T _a = 85°C	2.9	12.0		
			T _a = 105°C	6.3	42.0		
	Increment for RTC operation with low-speed on-chip oscillator ^{*4}			0.4	-		-
	Increment for RTC operation with sub-clock oscillator ^{*4}			0.5	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)
				1.6	-		SOMCR.SODRV[1:0] are 00b (normal mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state.

Note 2. The IWDT and LVD are not operating.

Note 3. VCC = 3.3 V.

Note 4. Includes the current of low-speed on-chip oscillator or sub-oscillation circuit.

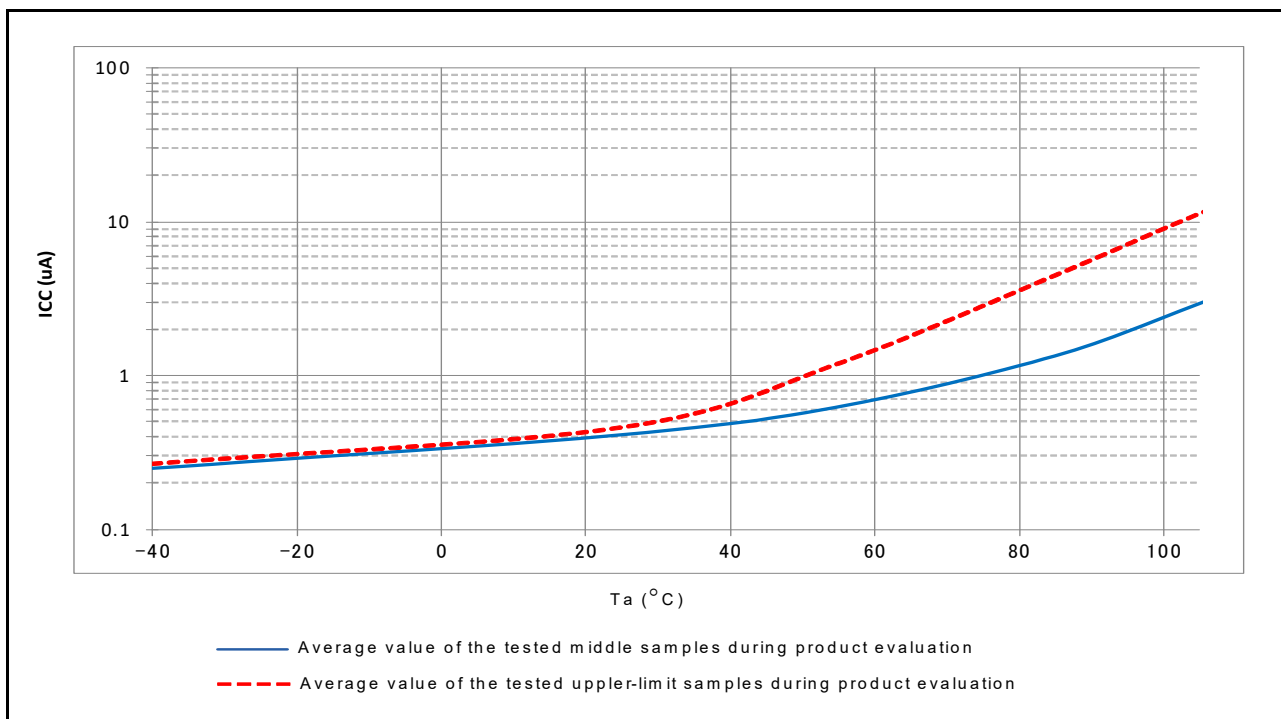
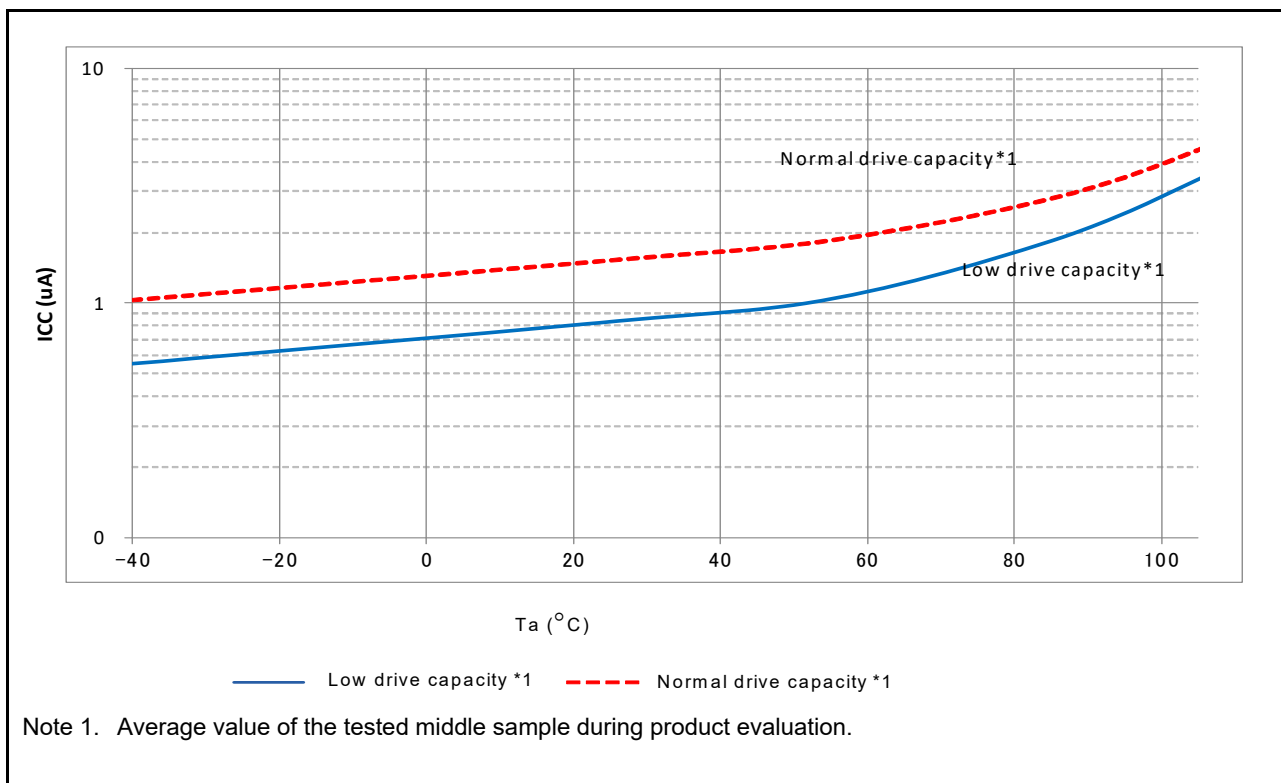


Figure 2.22 Temperature dependency in Software Standby mode (reference data)



Note 1. Average value of the tested middle sample during product evaluation.

Figure 2.23 Temperature dependency of RTC operation (reference data)

Table 2.13 Operating and standby current (3)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Analog power supply current	During A/D conversion (at high-speed conversion)	I _{AVCC}	-	-	3.0	mA	-	
	During A/D conversion (at low-power conversion)		-	-	1.0	mA	-	
	During D/A conversion *1 (per channel)		-	-	1.6	mA	-	
	Waiting for A/D and D/A conversion (all units)*5		-	-	1.0	μA	-	
Reference power supply current	During A/D conversion	I _{REFH0}	-	-	150	μA	-	
	Waiting for A/D conversion (all units)		-	-	60	nA	-	
Temperature sensor		I _{TNS}	-	75	-	μA	-	
Low-power analog comparator (ACMPLP) operating current	Window comparator (high-speed mode)	I _{CMPLP}	-	15	-	μA	-	
	Window comparator (low-speed mode)		-	3	-	μA	-	
	Comparator (high-speed mode)		-	10	-	μA	-	
	Comparator (low-speed mode)		-	2	-	μA	-	
High-speed analog comparator (ACMPHS) operating current		I _{CMPHS}	-	70	100	μA	AVCC0 ≥ 2.7V	
Operational Amplifier operating current	Low power mode	I _{AMP}	1-unit operating	-	1.0	2.0	μA	-
			2-unit operating	-	1.5	3.0	μA	-
			3-unit operating	-	2.0	3.5	μA	-
			4-unit operating	-	2.5	4.5	μA	-
	High speed mode		1-unit operating	-	200	280	μA	-
			2-unit operating	-	320	450	μA	-
			3-unit operating	-	440	620	μA	-
			4-unit operating	-	560	790	μA	-
USB operating current	During USB communication under the following settings and conditions: <ul style="list-style-type: none"> Function controller is in Full-Speed mode and <ul style="list-style-type: none"> Bulk OUT transfer is (64 bytes) × 1 Bulk IN transfer is (64 bytes) × 1 Host device is connected by a 1-meter USB cable from the USB port. 	I _{USBF} *2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-	
	During suspended state under the following setting and conditions: <ul style="list-style-type: none"> Function controller is in Full-Speed mode (the USB_DP pin is pulled up) Software Standby mode Host device is connected by a 1-meter USB cable from the USB port. 		I _{SUSP} *3	-	0.35 (VCC) 170 (VCC_USB)*4	-	μA	-
PWM Delay Generation Circuit current	PCLKD = 64 MHz, DLL Mode = 5-bit mode	I _{CC}	-	3.3	4.6	mA	-	
	PCLKD = 64 MHz, DLL Mode = 4-bit mode		-	3.0	4.2	mA	-	
	PCLKD = 32 MHz, DLL Mode = 5-bit mode		-	2.0	2.8	mA	-	

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Note 2. Current is consumed only by the USBFS.

Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU in the suspended state.

Note 4. When VCC = VCC_USB = 3.3 V.

Note 5. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC140 module-stop bit) is in the module-stop state.

2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.14 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	-	2	ms/V	-
	Voltage monitor 0 reset enabled at startup*1, *2				-		
	SCI boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.

Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.15 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).

When the VCC change exceeds VCC $\pm 10\%$, the allowable voltage change rising and falling gradient $dt/dVCC$ must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	-	-	10	kHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 2.24 $V_{r(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	$dt/dVCC$	1.0	-	-	ms/V	When VCC change exceeds VCC $\pm 10\%$

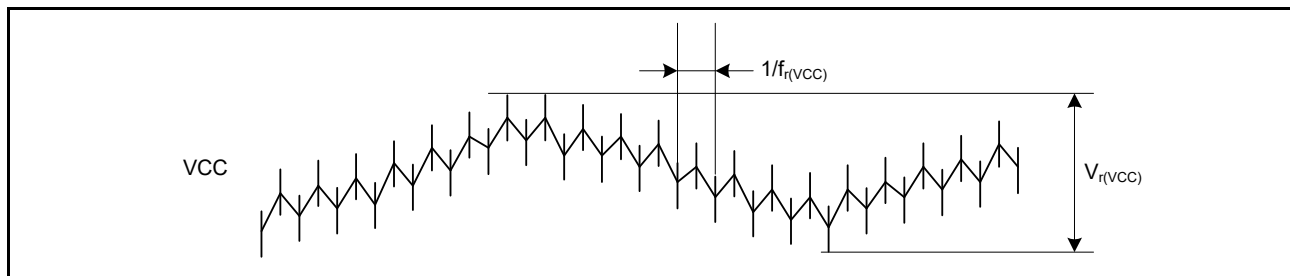


Figure 2.24 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.16 Operation frequency in high-speed operating mode

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter		Symbol	Min	Typ	Max*5	Unit	
Operation frequency	System clock (ICLK)*1, *2, *4	f	2.7 to 5.5 V	0.032768	-	32	MHz
			2.4 to 2.7 V	0.032768	-	16	
	Peripheral module clock (PCLKB)*4		2.7 to 5.5 V	-	-	32	
			2.4 to 2.7 V	-	-	16	
	Peripheral module clock (PCLKD)*3, *4		2.7 to 5.5 V	-	-	64	
			2.4 to 2.7 V	-	-	16	

- Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note 2. The frequency accuracy of ICLK must be $\pm 3.5\%$ during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
- Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
- Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
- Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see [Table 2.21, Clock timing](#).

Table 2.17 Operation frequency in middle-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Symbol	Min	Typ	Max*5	Unit	
Operation frequency	System clock (ICLK)*1, *2, *4	f	2.7 to 5.5 V	0.032768	-	12	MHz
			2.4 to 2.7 V	0.032768	-	12	
			1.8 to 2.4 V	0.032768	-	8	
	Peripheral module clock (PCLKB)*4		2.7 to 5.5 V	-	-	12	
			2.4 to 2.7 V	-	-	12	
			1.8 to 2.4 V	-	-	8	
	Peripheral module clock (PCLKD)*3, *4		2.7 to 5.5 V	-	-	12	
			2.4 to 2.7 V	-	-	12	
			1.8 to 2.4 V	-	-	8	

- Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note 2. The frequency accuracy of ICLK must be $\pm 3.5\%$ during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
- Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
- Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.
- Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see [Table 2.21, Clock timing](#).

Table 2.18 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.8 to 5.5 V	f	0.032768	-	1	MHz
	Peripheral module clock (PCLKB)*4	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3, *4	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.

Note 2. The frequency accuracy of ICLK must be $\pm 3.5\%$ during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 1 MHz when the A/D converter is in use.

Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.

Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see [Table 2.21, Clock timing](#).

Table 2.19 Operation frequency in low-voltage mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*1, *2, *4	1.6 to 5.5 V	f	0.032768	-	4	MHz
	Peripheral module clock (PCLKB)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*3, *4	1.6 to 5.5 V		-	-	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of ICLK must be $\pm 3.5\%$ during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKD is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.

Note 4. See section 8, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, and PCLKD.

Note 5. The maximum value of operation frequency does not include internal oscillator errors. For details on the range of guaranteed operation, see [Table 2.21, Clock timing](#).

Table 2.20 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1, *3	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*2, *3	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.

Note 2. The 14-bit A/D converter cannot be used.

Note 3. See section 8, Clock Generation Circuit in User's Manual for the relationship between ICLK, PCLKB, and PCLKD frequencies.

2.3.2 Clock Timing

Table 2.21 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	-	-	ns	Figure 2.25
EXTAL external clock input high pulse width	t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width	t_{XL}	20	-	-	ns	
EXTAL external clock rising time	t_{Xr}	-	-	5	ns	
EXTAL external clock falling time	t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	-	-	μ s	-
EXTAL external clock input frequency	f_{EXTAL}	-	-	20	MHz	$2.4 \leq VCC \leq 5.5$
		-	-	8		$1.8 \leq VCC < 2.4$
		-	-	1		$1.6 \leq VCC < 1.8$
Main clock oscillator oscillation frequency	f_{MAIN}	1	-	20	MHz	$2.4 \leq VCC \leq 5.5$
		1	-	8		$1.8 \leq VCC < 2.4$
		1	-	4		$1.6 \leq VCC < 1.8$
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time	t_{LOCO}	-	-	100	μ s	Figure 2.26
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time	t_{MOCO}	-	-	1	μ s	-
HOCO clock oscillation frequency	f_{HOCO24}	23.64	24	24.36	MHz	$T_a = -40$ to -20°C $1.8 \leq VCC \leq 5.5$
		22.68	24	25.32		$T_a = -40$ to 85°C $1.6 \leq VCC < 1.8$
		23.76	24	24.24		$T_a = -20$ to 85°C $1.8 \leq VCC \leq 5.5$
		23.52	24	24.48		$T_a = 85$ to 105°C $2.4 \leq VCC \leq 5.5$
	f_{HOCO32}	31.52	32	32.48		$T_a = -40$ to -20°C $1.8 \leq VCC \leq 5.5$
		30.24	32	33.76		$T_a = -40$ to 85°C $1.6 \leq VCC < 1.8$
		31.68	32	32.32		$T_a = -20$ to 85°C $1.8 \leq VCC \leq 5.5$
		31.36	32	32.64		$T_a = 85$ to 105°C $2.4 \leq VCC \leq 5.5$
	f_{HOCO48}^{*3}	47.28	48	48.72		$T_a = -40$ to -20°C $1.8 \leq VCC \leq 5.5$
		47.52	48	48.48		$T_a = -20$ to 85°C $1.8 \leq VCC \leq 5.5$
		47.04	48	48.96		$T_a = 85$ to 105°C $2.4 \leq VCC \leq 5.5$
	f_{HOCO64}^{*4}	63.04	64	64.96		$T_a = -40$ to -20°C $2.4 \leq VCC \leq 5.5$
63.36		64	64.64	$T_a = -20$ to 85°C $2.4 \leq VCC \leq 5.5$		
62.72		64	65.28	$T_a = 85$ to 105°C $2.4 \leq VCC \leq 5.5$		
HOCO clock oscillation stabilization time*5, *6	Except low-voltage mode	t_{HOCO24}	-	-	μ s	Figure 2.27
		t_{HOCO32}	-	-		
		t_{HOCO48}	-	-		
	t_{HOCO64}	-	-			
Low-voltage mode	t_{HOCO24}	-	-	100.9		
Sub-clock oscillator oscillation frequency	f_{SUB}	-	32.768	-	kHz	-
		-	-	-		

Table 2.21 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	-	0.5	-	s	Figure 2.28

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.

Note 3. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 5.5 V.

Note 4. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 5.5 V.

Note 5. This is a characteristic when the HOCOCCR.HCSTP bit is cleared to 0 (oscillation) in the MOCO stop state. When the HOCOCCR.HCSTP bit is cleared to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 μ s.

Note 6. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

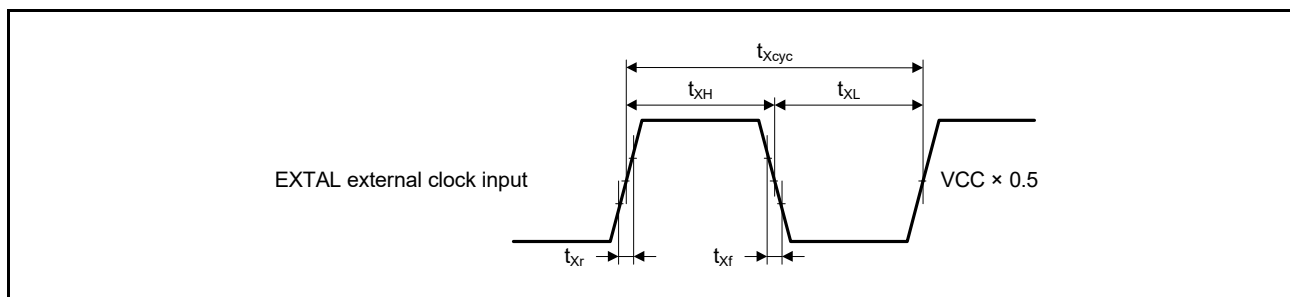


Figure 2.25 EXTAL external clock input timing

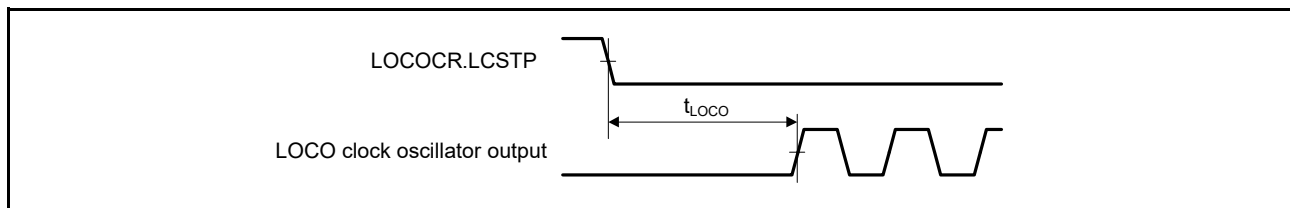


Figure 2.26 LOCO clock oscillator start timing

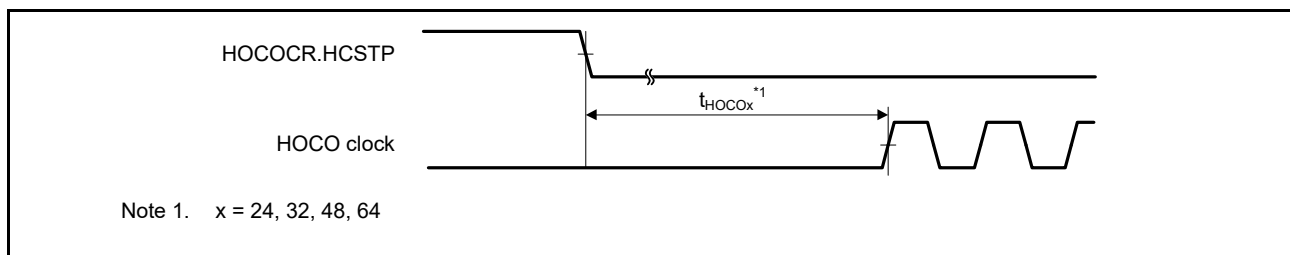


Figure 2.27 HOCO clock oscillator start timing (started by setting the HOCOCCR.HCSTP bit)

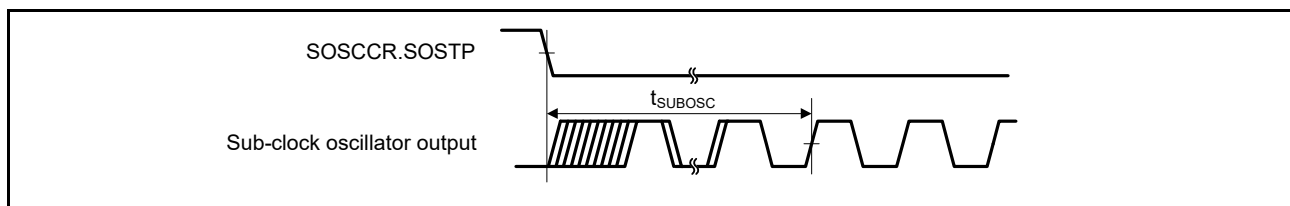


Figure 2.28 Sub-clock oscillator start timing

2.3.3 Reset Timing

Table 2.22 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	3	-	-	ms	Figure 2.29
	Not at power-on	t_{RESW}	30	-	-	μ s	Figure 2.30
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	-	0.7	-	ms	Figure 2.29
	LVD0 disabled*2		-	0.3	-		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	-	0.5	-	ms	Figure 2.30
	LVD0 disabled*2		-	0.05	-		
Wait time after internal reset cancellation (watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	t_{RESWT3}	-	0.6	-	ms	
	LVD0 disabled*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.

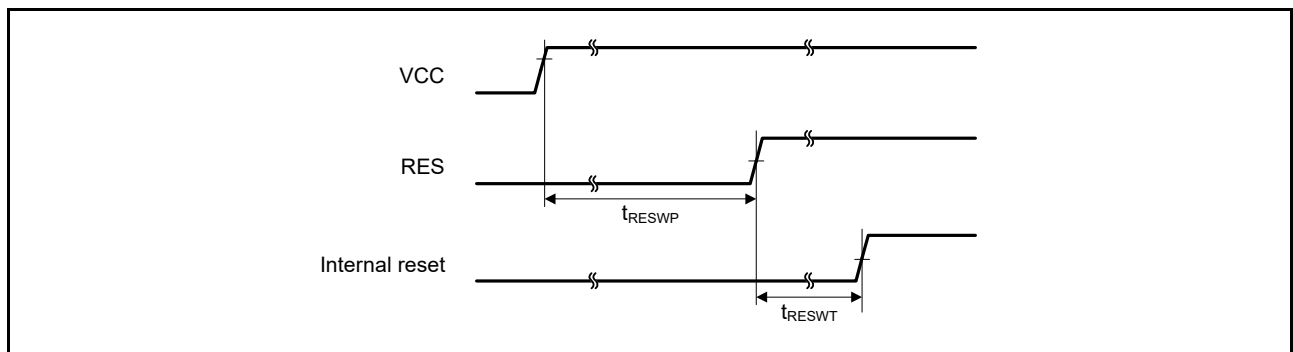


Figure 2.29 Reset input timing at power-on

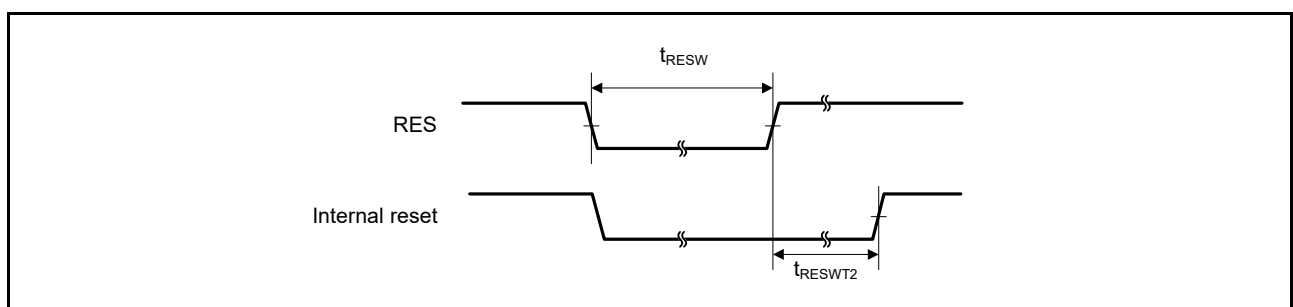


Figure 2.30 Reset input timing

2.3.4 Wakeup Time

Table 2.23 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t _{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t _{SBYEX}	-	14	25	μs	
		System clock source is HOCO*4 (HOCO clock is 32 MHz)		t _{SBYHO}	-	43	52	μs	
		System clock source is HOCO*4 (HOCO clock is 48 MHz)		t _{SBYHO}	-	44	52	μs	
		System clock source is HOCO*5 (HOCO clock is 64 MHz)		t _{SBYHO}	-	82	110	μs	
		System clock source is MOCO		t _{SBYMO}	-	16	25	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Note 4. The HOCO clock wait control register (HOCOWTCR) is set to 05h.

Note 5. The HOCO clock wait control register (HOCOWTCR) is set to 06h.

Table 2.24 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (12 MHz)*2	t _{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (12 MHz)*3	t _{SBYEX}	-	2.9	10	μs	
		System clock source is HOCO*4		t _{SBYHO}	-	38	50	μs	
		System clock source is MOCO (8 MHz)		t _{SBYMO}	-	3.5	5.5	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Note 4. The system clock is 12 MHz.

Table 2.25 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (1 MHz)*2	t _{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (1 MHz)*3	t _{SBYEX}	-	28	50	μs	
		System clock source is MOCO (1 MHz)		t _{SBYMO}	-	25	35	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.26 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-voltage mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (4 MHz)*2	t _{SBYMC}	-	2	3	ms	Figure 2.31
		External clock input to main clock oscillator	System clock source is main clock oscillator (4 MHz)*3	t _{SBYEX}	-	108	130	μs	
		System clock source is HOCO (4 MHz)		t _{SBYHO}	-	108	130	μs	

Note 1. The division ratio of ICK and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.27 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	SubOSC-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t _{SBYSC}	-	0.85	1	ms	Figure 2.31
		System clock source is LOCO (32.768 kHz)	t _{SBYLO}	-	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

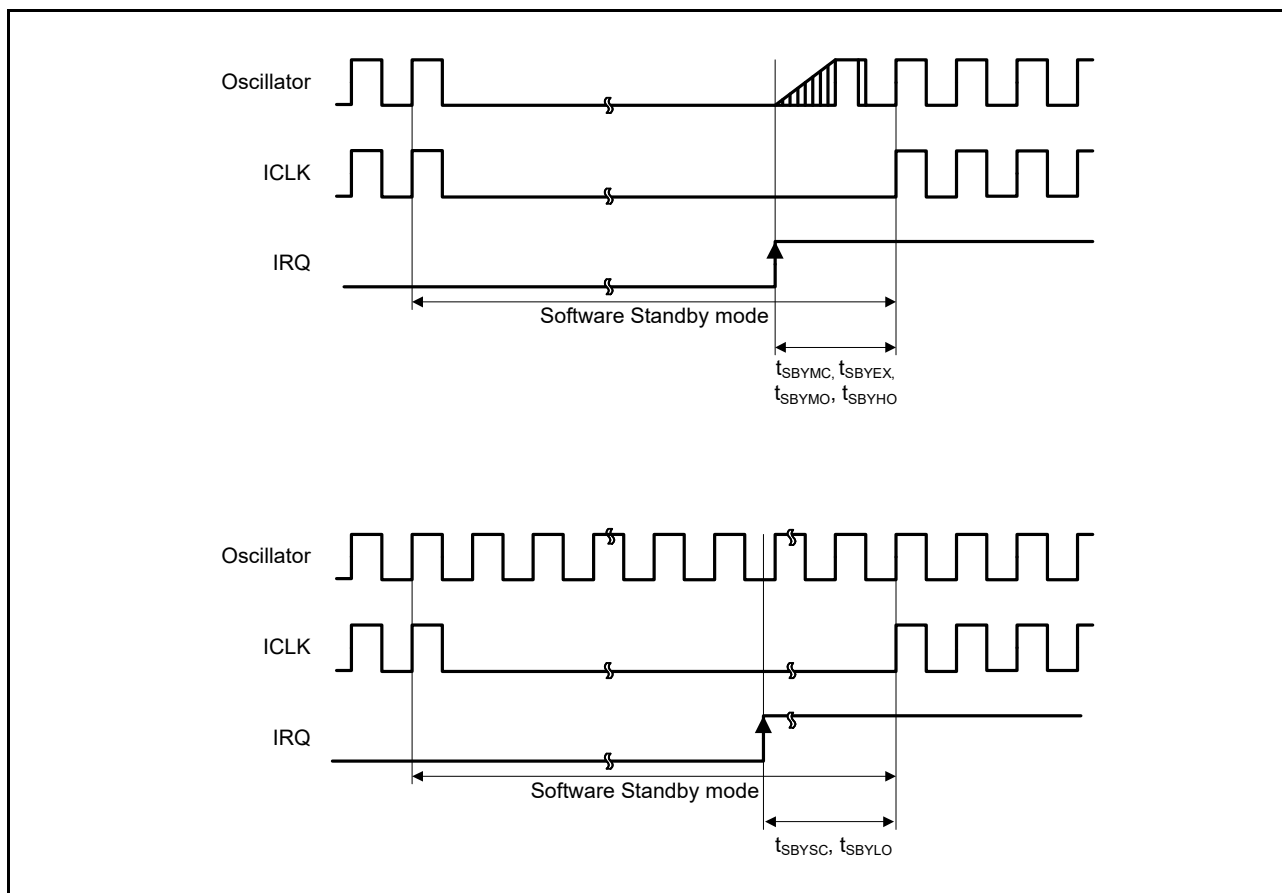


Figure 2.31 Software Standby mode cancellation timing

Table 2.28 Timing of recovery from low power modes (6)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	-	36	45	μs	Figure 2.32
	Middle-speed mode System clock source is MOCO (8 MHz)	t_{SNZ}	-	1.3	3.6	μs	
	Low-speed mode System clock source is MOCO (1 MHz)	t_{SNZ}	-	10	13	μs	
	Low-voltage mode System clock source is HOCO (4 MHz)	t_{SNZ}	-	87	110	μs	

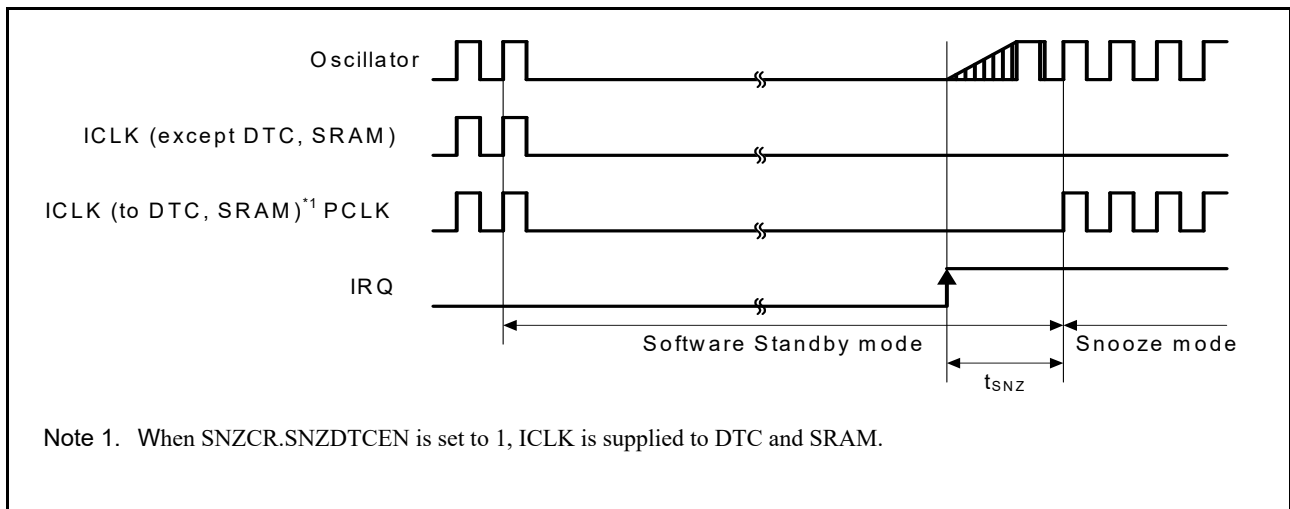


Figure 2.32 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.29 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.

Note 1. t_{Pcyc} indicates the PCLKB cycle.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQ_i digital filter sampling clock (i = 0 to 7).

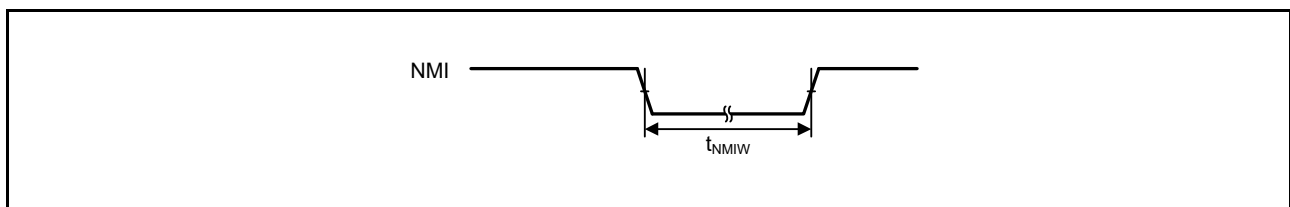


Figure 2.33 NMI interrupt input timing

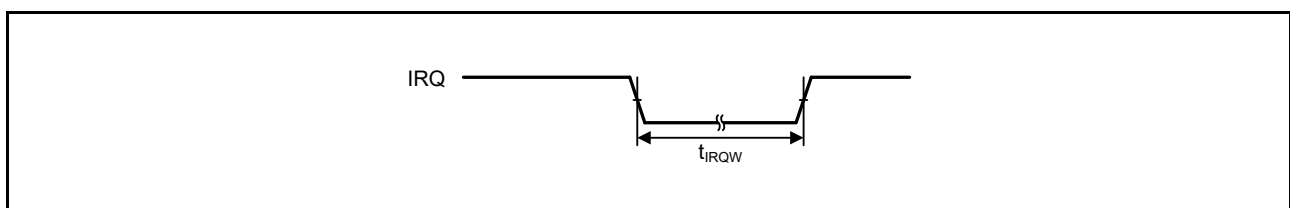


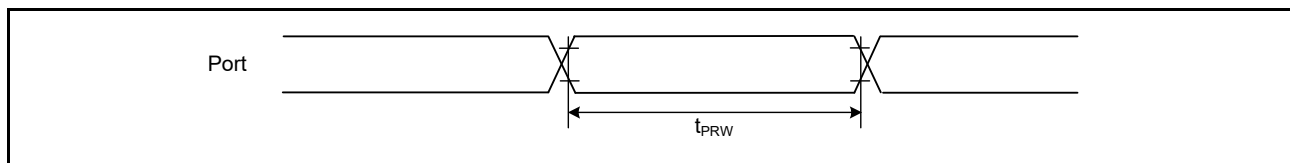
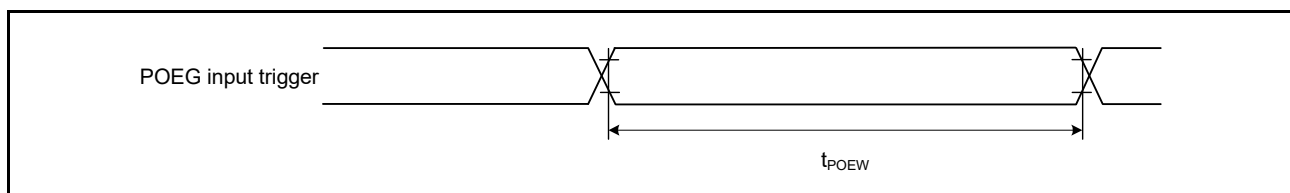
Figure 2.34 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

Table 2.30 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing

Parameter		Symbol	Min	Max	Unit	Test conditions	
I/O Ports	Input data pulse width	t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.35	
	Input/output data cycle (P002, P003, P010, P011)	t_{POcyc}	10	-	μs	-	
POEG	POEG input trigger pulse width	t_{POEW}	3	-	t_{Pcyc}	Figure 2.36	
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.37
		Dual edge		2.5	-		
AGT	AGTIO, AGTEE input cycle	$2.7 V \leq VCC \leq 5.5 V$	t_{ACYC}^{*1}	250	-	ns	Figure 2.38
		$2.4 V \leq VCC < 2.7 V$		500	-	ns	
		$1.8 V \leq VCC < 2.4 V$		1000	-	ns	
		$1.6 V \leq VCC < 1.8 V$		2000	-	ns	
	AGTIO, AGTEE input high level width, low-level width	$2.7 V \leq VCC \leq 5.5 V$	t_{ACKWH}, t_{ACKWL}	100	-	ns	
		$2.4 V \leq VCC < 2.7 V$		200	-	ns	
		$1.8 V \leq VCC < 2.4 V$		400	-	ns	
		$1.6 V \leq VCC < 1.8 V$		800	-	ns	
AGTIO, AGTO, AGTOA, AGTOB output cycle	$2.7 V \leq VCC \leq 5.5 V$	t_{ACYC2}	62.5	-	ns	Figure 2.38	
	$2.4 V \leq VCC < 2.7 V$		125	-	ns		
	$1.8 V \leq VCC < 2.4 V$		250	-	ns		
	$1.6 V \leq VCC < 1.8 V$		500	-	ns		
ADC14	14-bit A/D converter trigger input pulse width	t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.39	
KINT	KRn (n = 00 to 07) pulse width	t_{KR}	250	-	ns	Figure 2.40	

Note 1. Constraints on AGTIO input: $t_{Pcyc} \times 2 (t_{Pcyc}: PCLKB \text{ cycle}) < t_{ACYC}$.

**Figure 2.35 I/O ports input timing****Figure 2.36 POEG input trigger timing**

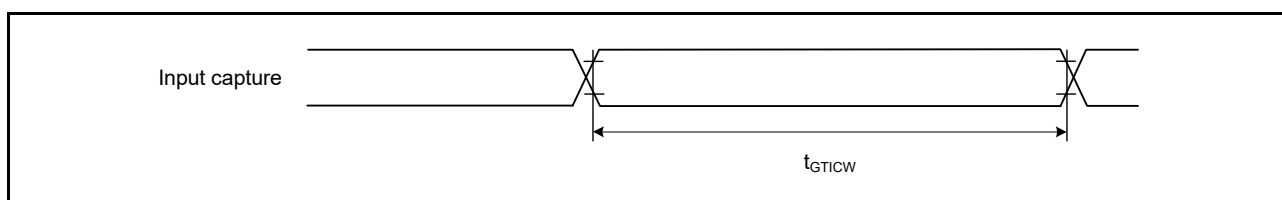


Figure 2.37 GPT input capture timing

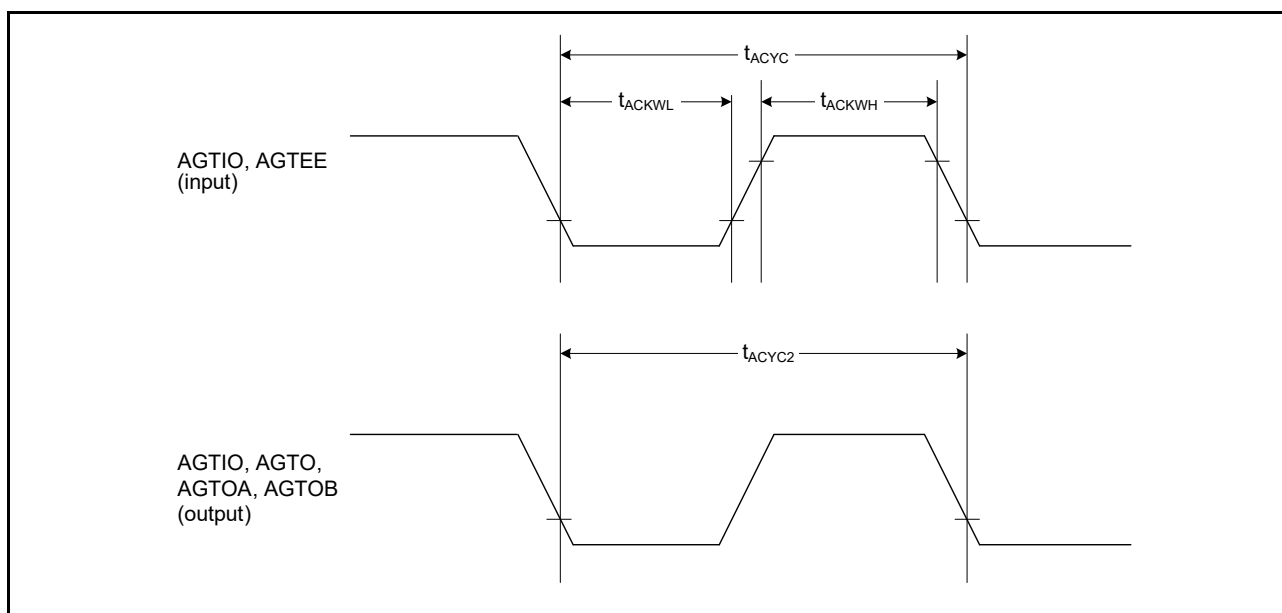


Figure 2.38 AGT I/O timing

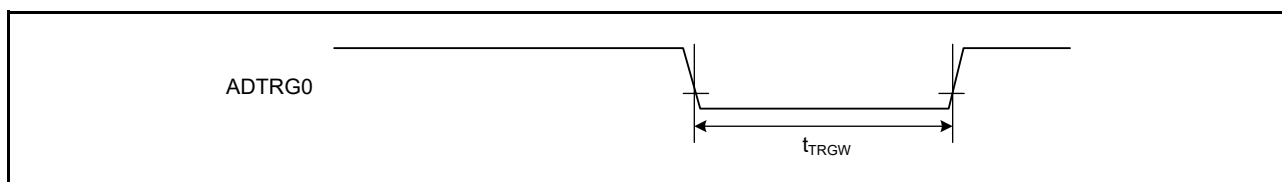


Figure 2.39 ADC14 trigger input timing

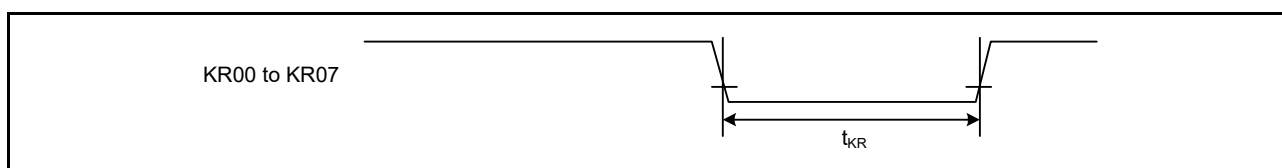


Figure 2.40 Key interrupt input timing

2.3.7 PWM Delay Generation Circuit Timing

Table 2.31 PWM delay generation circuit timing
Conditions: $V_{CC} = AV_{CC0} = 2.7$ to 5.5 V 32 MHz \leq PCLKD \leq 64 MHz

Parameter		Min	Typ	Max	Unit	Test conditions
Resolution	PCLKD = 64 MHz, DLL Mode = 5-bit mode	-	488	-	ps	-
	PCLKD = 64 MHz, DLL Mode = 4-bit mode	-	976	-	ps	-
	PCLKD = 32 MHz, DLL Mode = 5-bit mode	-	976	-	ps	-
DNL*1, *2		-	5	-	LSB	-

Note 1. The differences among lines in 1-LSB resolution are normalized by this value.

Note 2. The drive capability of the PWM delay generation circuit output port is middle drive.

2.3.8 CAC Timing

Table 2.32 CAC timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
CAC	CACREF input pulse width	$t_{Pcyc}^{*1} \leq t_{cac}^{*2}$	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{Pcyc}$	-	-	ns	-
		$t_{Pcyc}^{*1} > t_{cac}^{*2}$		$5 \times t_{cac} + 6.5 \times t_{Pcyc}$	-	-	ns	

Note 1. t_{Pcyc} : PCLKB cycle.

Note 2. t_{cac} : CAC count clock source cycle.

2.3.9 SCI Timing

Table 2.33 SCI timing (1)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter		Symbol	Min	Max	Unit ^{*1}	Test conditions	
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.41
		Clock synchronous		6	-		
Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
Input clock rise time		t_{SCKr}	-	20	ns		
Input clock fall time		t_{SCKf}	-	20	ns		
Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}		
	Clock synchronous		4	-			
Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
Output clock rise time	1.8V or above	t_{SCKr}	-	20	ns		
			1.6V or above	-			30
Output clock fall time	1.8V or above	t_{SCKf}	-	20	ns		
			1.6V or above	-			30
Transmit data delay (master)	Clock synchronous	t_{TXD}	-	40	ns	Figure 2.42	
			1.6V or above	-			45
Transmit data delay (slave)	Clock synchronous	t_{TXD}	-	55	ns		
			2.4V or above	-			60
			1.8V or above	-			100
			1.6V or above	-			125
Receive data setup time (master)	Clock synchronous	t_{RXS}	45	-	ns		
			55	-			
			90	-			
			110	-			
Receive data setup time (slave)	Clock synchronous	t_{RXS}	40	-	ns		
			45	-			
Receive data hold time (master)	Clock synchronous	t_{RXH}	5	-	ns		
Receive data hold time (slave)	Clock synchronous	t_{RXH}	40	-	ns		

Note 1. t_{Pcyc} : PCLKB cycle.

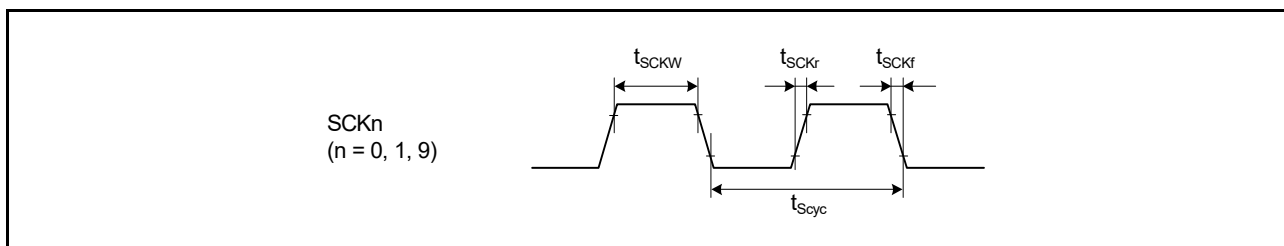


Figure 2.41 SCK clock input timing

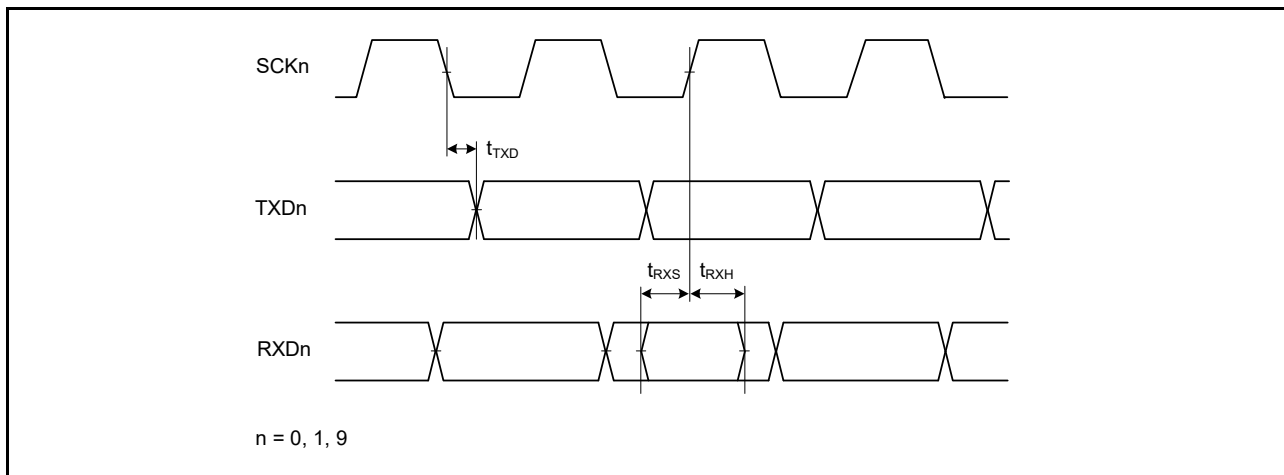


Figure 2.42 SCI input/output timing in clock synchronous mode

Table 2.34 SCI timing (2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Max	Unit*1	Test conditions		
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.43		
	SCK clock cycle input (slave)			6	65536				
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}			
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}			
	SCK clock rise and fall time		t_{SPCKr} , t_{SPCKf}	1.8V or above	-	20		ns	
				1.6V or above	-	30			
	Data input setup time	Master	2.7V or above	t_{SU}	45	-		ns	Figure 2.44 to Figure 2.47
			2.4V or above		55	-			
			1.8V or above		80	-			
			1.6V or above		110	-			
		Slave	2.7V or above		40	-			
			1.6V or above		45	-			
Data input hold time	Master		t_H	33.3	-	ns			
	Slave			40	-				
SS input setup time			t_{LEAD}	1	-	t_{SPcyc}			
SS input hold time			t_{LAG}	1	-	t_{SPcyc}			
Data output delay	Master	1.8V or above	t_{OD}	-	40	ns			
		1.6V or above		-	50				
	Slave	2.4V or above		-	65				
		1.8V or above		-	100				
		1.6V or above		-	125				
Data output hold time	Master	2.7V or above	t_{OH}	-10	-	ns			
		2.4V or above		-20	-				
		1.8V or above		-30	-				
		1.6V or above		-40	-				
	Slave			-10	-				
Data rise and fall time	Master		t_{Dr} , t_{Df}	-	20	ns			
	Slave	1.8V or above		-	20				
		1.6V or above		-	30				
Simple SPI	Slave access time		t_{SA}	-	6	t_{Pcyc}	Figure 2.47		
	Slave output release time		t_{REL}	-	6	t_{Pcyc}			

Note 1. t_{Pcyc} : PCLKB cycle.

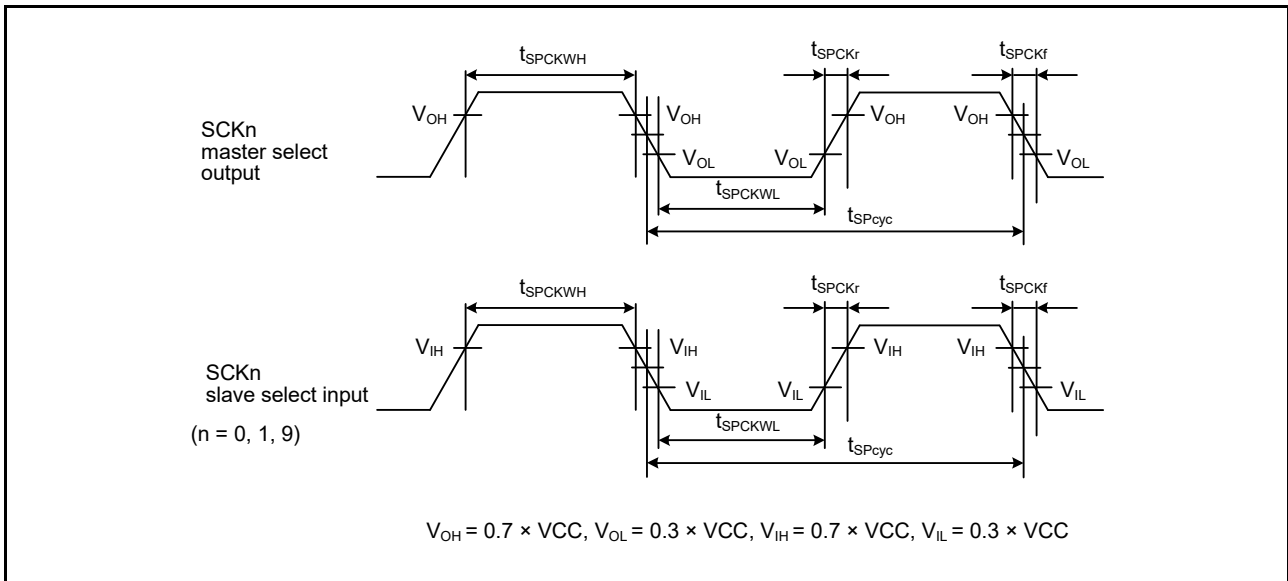


Figure 2.43 SCKn master select output and slave select input timing

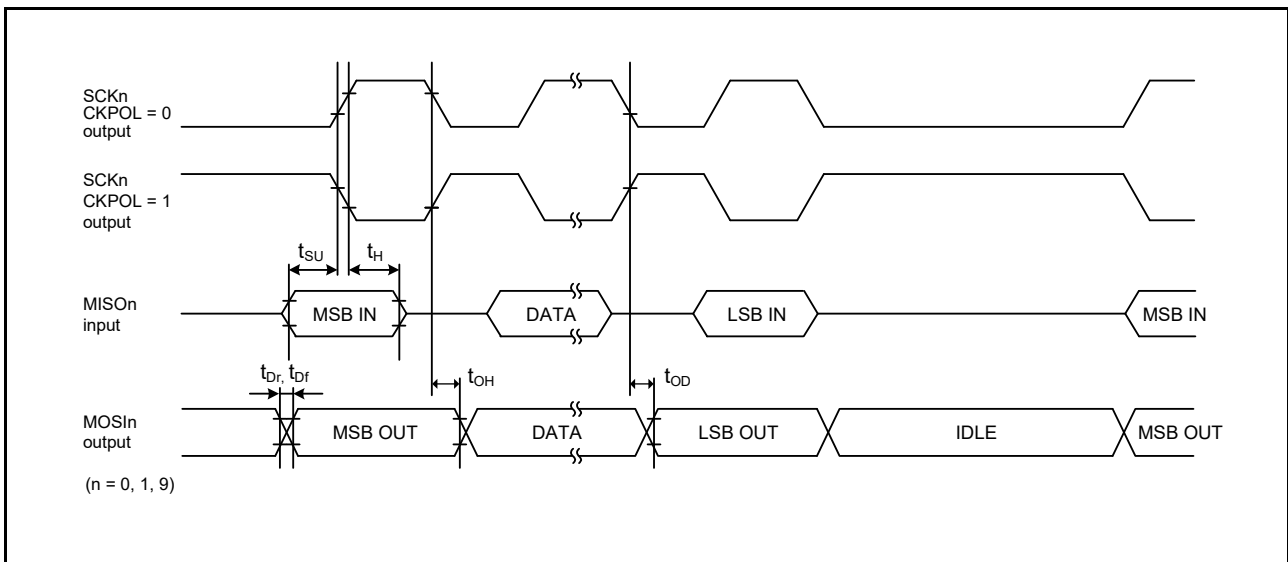


Figure 2.44 SCKn master, CKPOL = 1, MISO and MOS timing

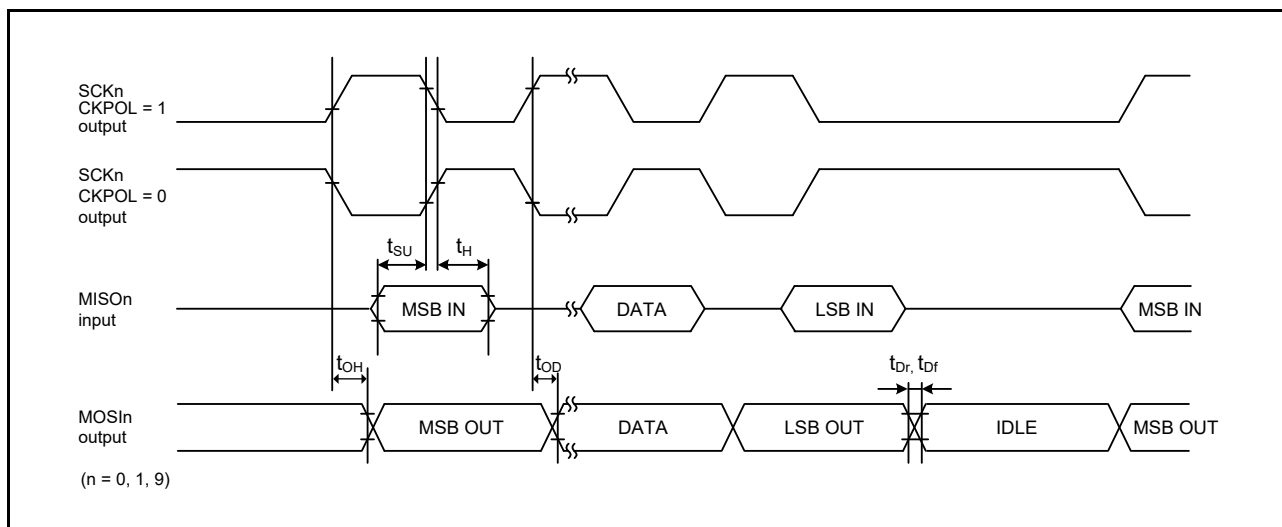


Figure 2.45 SCI simple SPI mode timing (master, CKPH = 0)

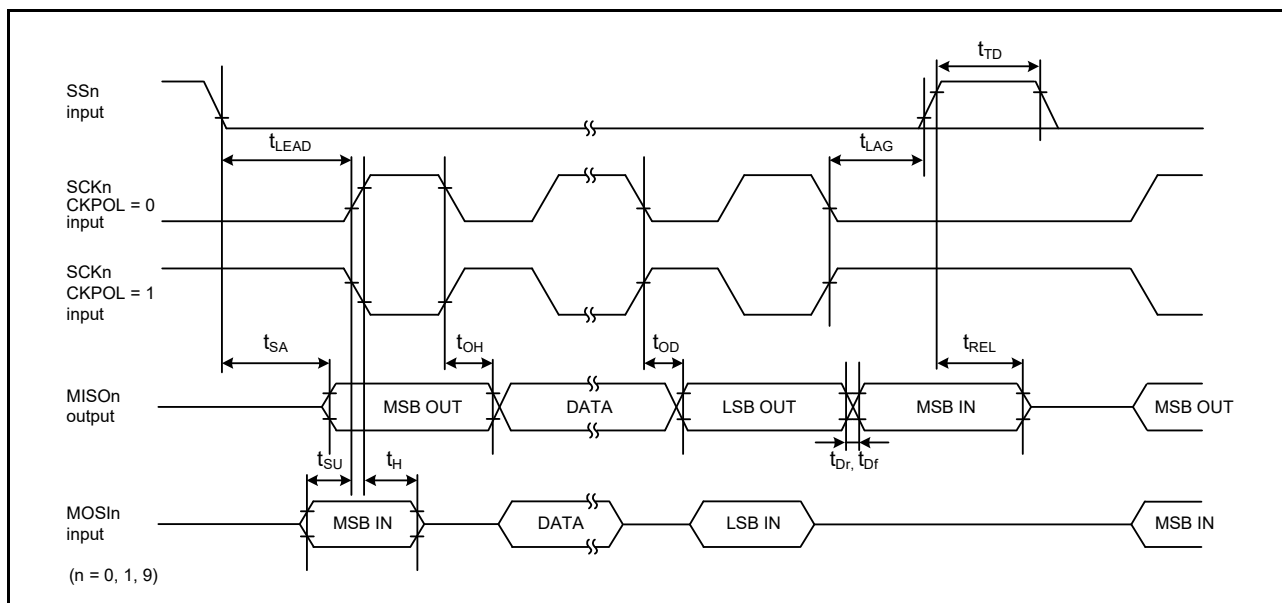


Figure 2.46 SCI simple SPI mode timing (slave, CKPH = 1)

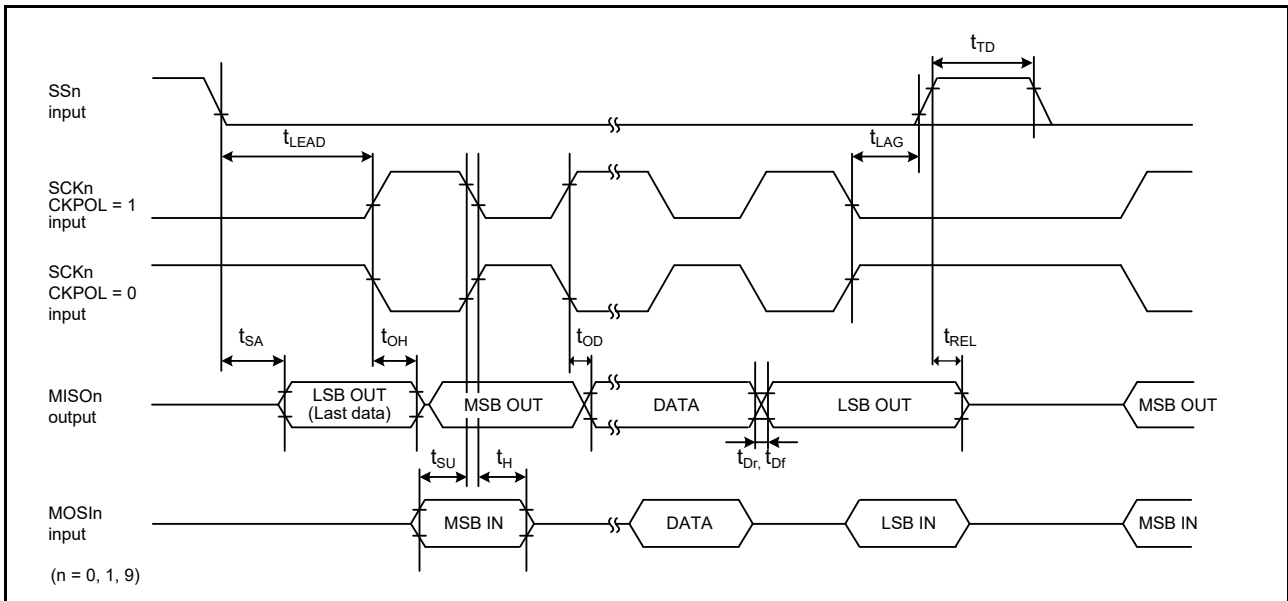


Figure 2.47 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.35 SCI timing (3)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter	Symbol	Min	Max	Unit	Test conditions	
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.48
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b^{*1}	-	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 2.48
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b^{*1}	-	400	pF	

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle.

Note 1. C_b indicates the total capacity of the bus line.

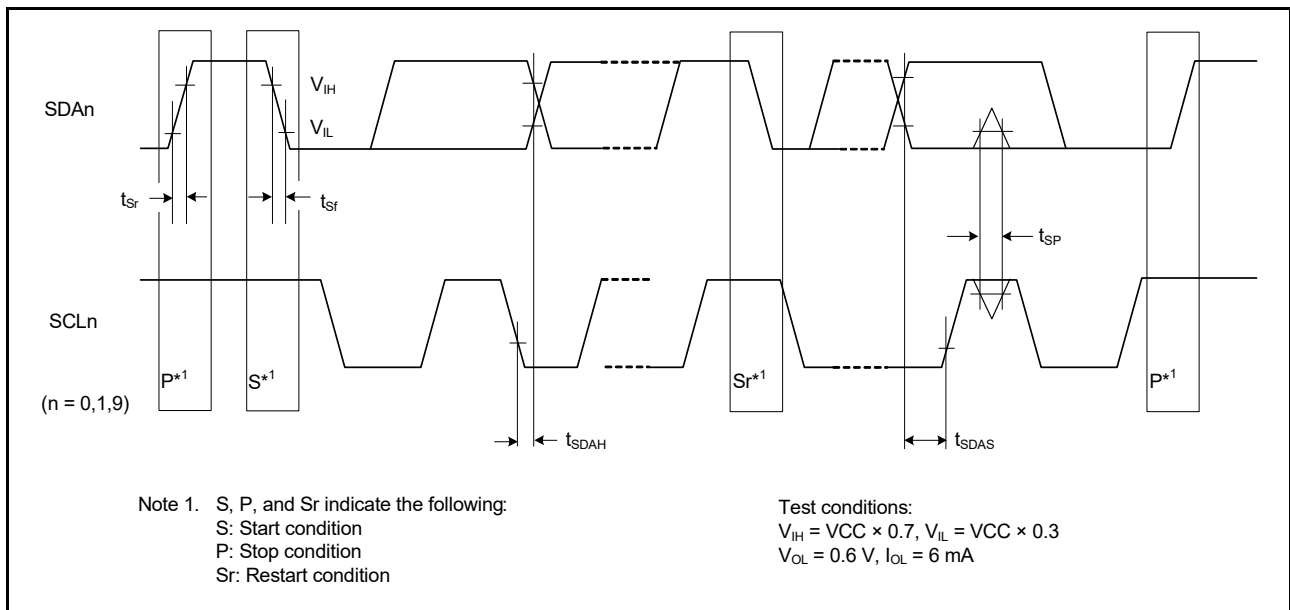


Figure 2.48 SCI simple IIC mode timing

2.3.10 SPI Timing

Table 2.36 SPI timing (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit*1	Test conditions		
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.49 C = 30pF	
		Slave		6	4096			
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$		ns		
		Slave		$3 \times t_{Pcyc}$				
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$		ns		
		Slave		$3 \times t_{Pcyc}$				
	RSPCK clock rise and fall time	Output		2.7V or above	-	10		ns
				2.4V or above	-	15		
				1.8V or above	-	20		
				1.6V or above	-	30		
		Input	-	1	μs			

Table 2.36 SPI timing (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions		
SPI	Data input setup time	Master	t_{SU}	10	-	ns	Figure 2.50 to Figure 2.55 C = 30pF		
		Slave		2.4V or above	10			-	
				1.8V or above	15			-	
				1.6V or above	20			-	
	Data input hold time	Master (RSPCK is PCLKB/2)	t_{HF}	0	-	ns			
		Master (RSPCK is not PCLKB/2)	t_H	t_{Pcyc}	-				
		Slave	t_H	20	-				
	SSL setup time	Master	t_{LEAD}	$-30 + N \times t_{SPcyc}^{*2}$	-	ns			
		Slave		$6 \times t_{Pcyc}$	-	ns			
	SSL hold time	Master	t_{LAG}	$-30 + N \times t_{SPcyc}^{*3}$	-	ns			
		Slave		$6 \times t_{Pcyc}$	-	ns			
	Data output delay	Master	2.7V or above	t_{OD}	-	14		ns	Figure 2.50 to Figure 2.55 C = 30pF
			2.4V or above		-	20			
			1.8V or above		-	25			
			1.6V or above		-	30			
		Slave	2.7V or above		-	50			
			2.4V or above		-	60			
			1.8V or above		-	85			
			1.6V or above		-	110			
	Data output hold time	Master	t_{OH}	0	-	ns			
Slave		0		-					
Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns				
	Slave		$6 \times t_{Pcyc}$	-					
MOSI and MISO rise and fall time	Output	2.7V or above	t_{Dr}, t_{Df}	-	10	ns			
		2.4V or above		-	15				
		1.8V or above		-	20				
		1.6V or above		-	30				
	Input	-		1	μs				
SSL rise and fall time	Output	2.7V or above	t_{SSLr}, t_{SSLf}	-	10	ns			
		2.4V or above		-	15				
		1.8V or above		-	20				
		1.6V or above		-	30				
	Input	-		1	μs				
Slave access time	2.4V or above	t_{SA}	-	$2 \times t_{Pcyc} + 100$	ns	Figure 2.54 and Figure 2.55 C = 30pF			
			1.8V or above	-			$2 \times t_{Pcyc} + 140$		
			1.6V or above	-			$2 \times t_{Pcyc} + 180$		
Slave output release time	2.4V or above	t_{REL}	-	$2 \times t_{Pcyc} + 100$	ns				
			1.8V or above	-			$2 \times t_{Pcyc} + 140$		
			1.6V or above	-			$2 \times t_{Pcyc} + 180$		

Note 1. t_{Pcyc} : PCLKB cycle.

Note 2. N is set as an integer from 1 to 8 by the SPCKD register.

Note 3. N is set as an integer from 1 to 8 by the SSLND register.

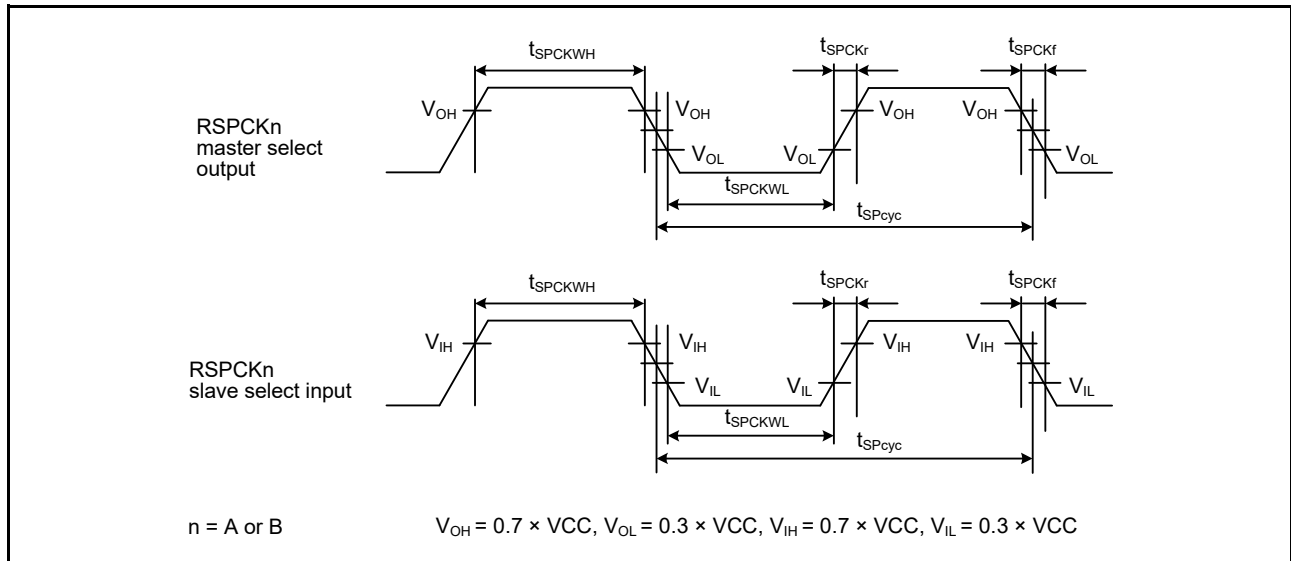


Figure 2.49 SPI clock timing

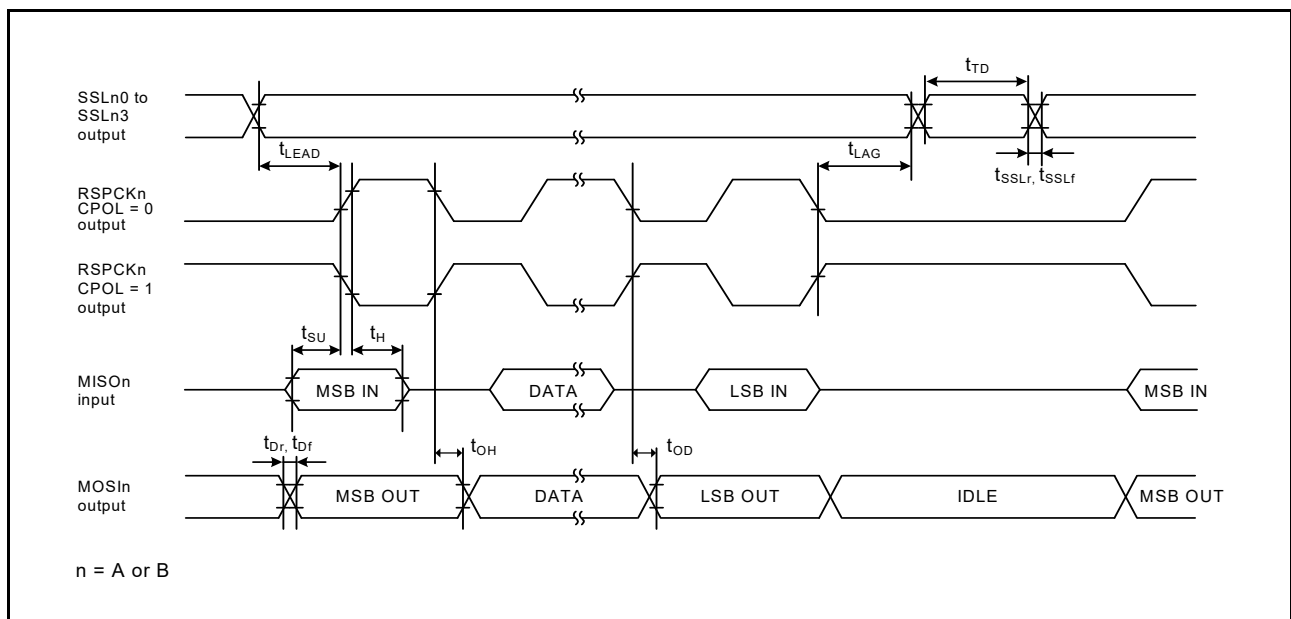


Figure 2.50 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

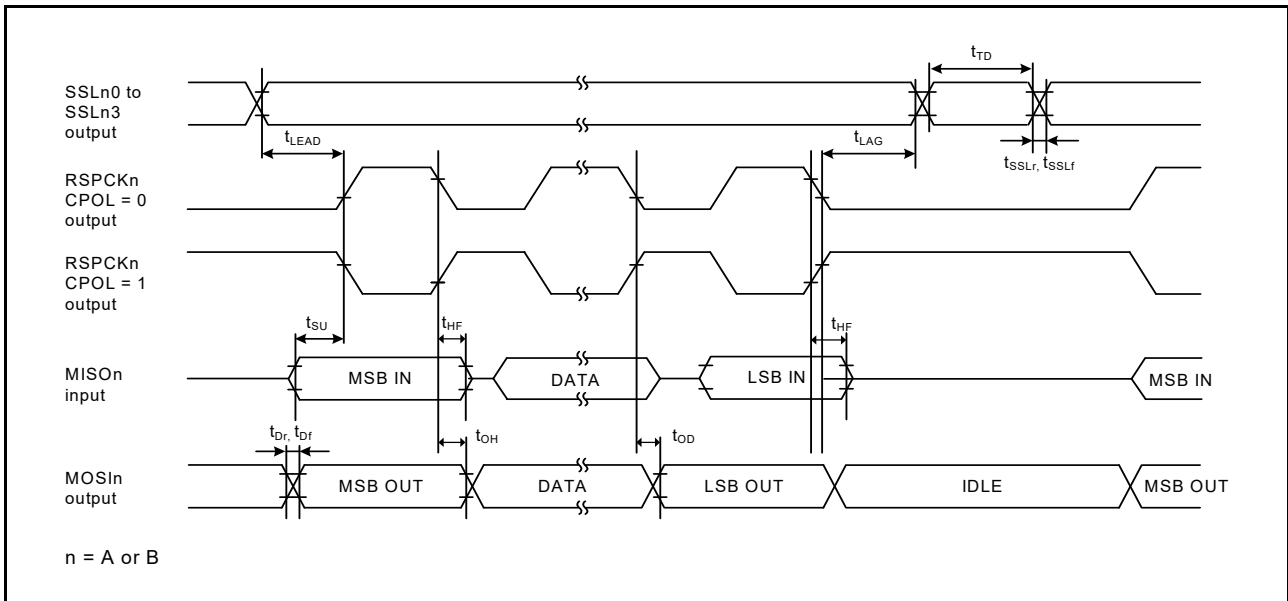


Figure 2.51 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

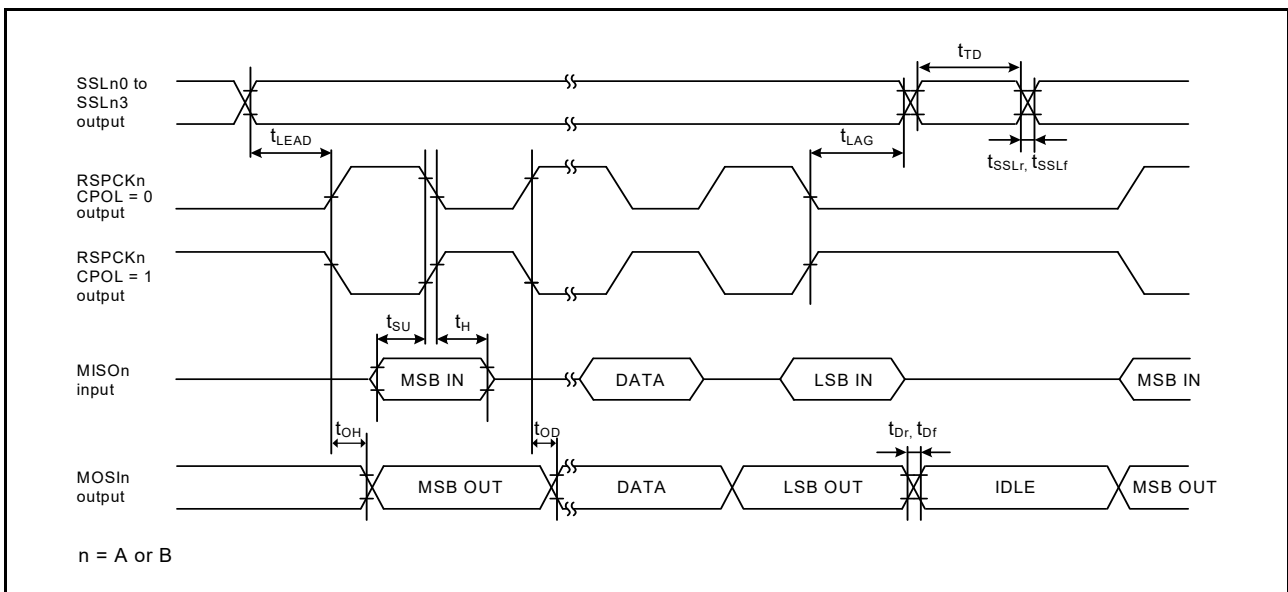


Figure 2.52 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

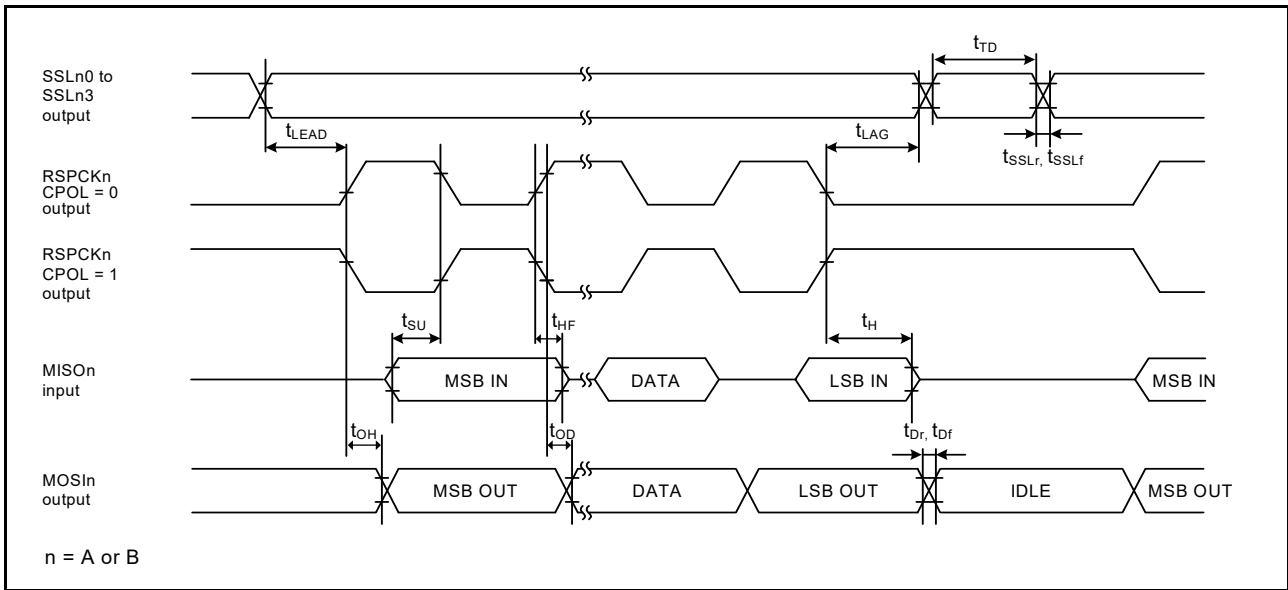


Figure 2.53 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)

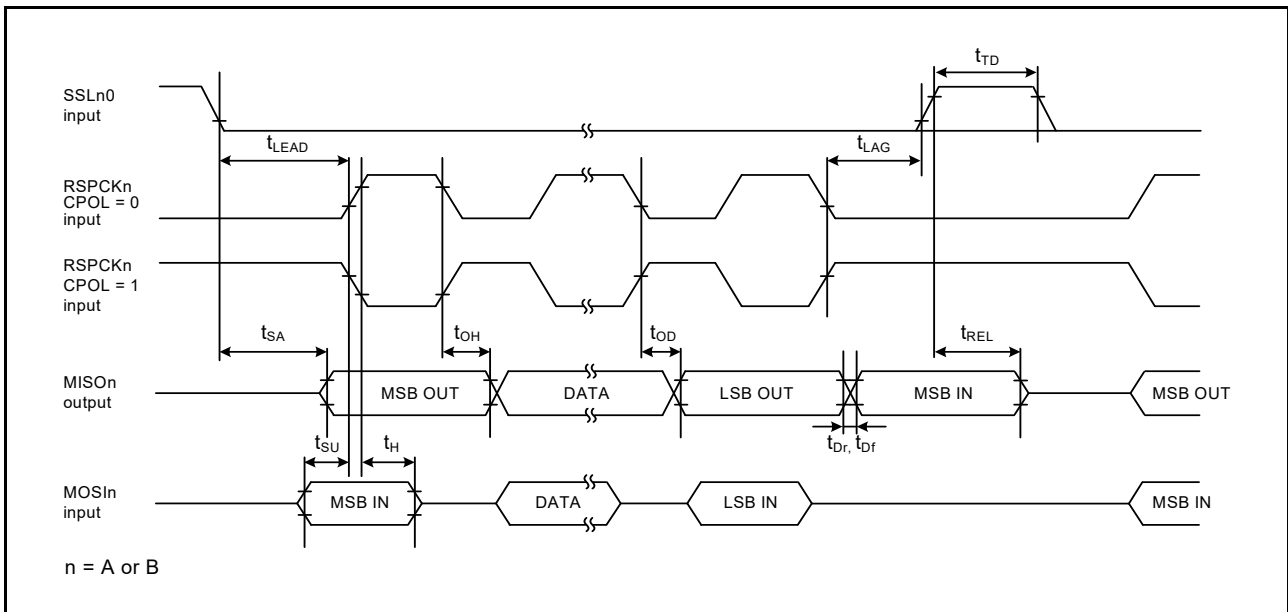


Figure 2.54 SPI timing (slave, CPHA = 0)

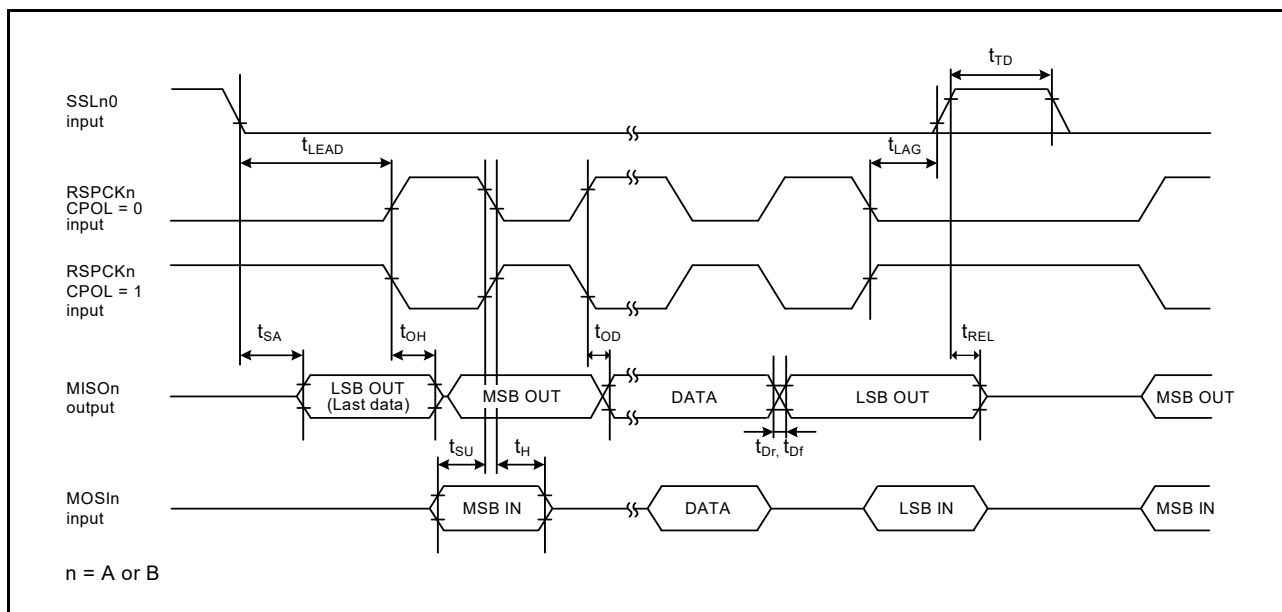


Figure 2.55 SPI timing (slave, CPHA = 1)

2.3.11 IIC Timing

Table 2.37 IIC timing

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 1300$	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
SCL, SDA capacitive load	C_b	-	400	pF		
IIC (Fast mode)	SCL input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 600$	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	300	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
SCL, SDA capacitive load	C_b	-	400	pF		

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

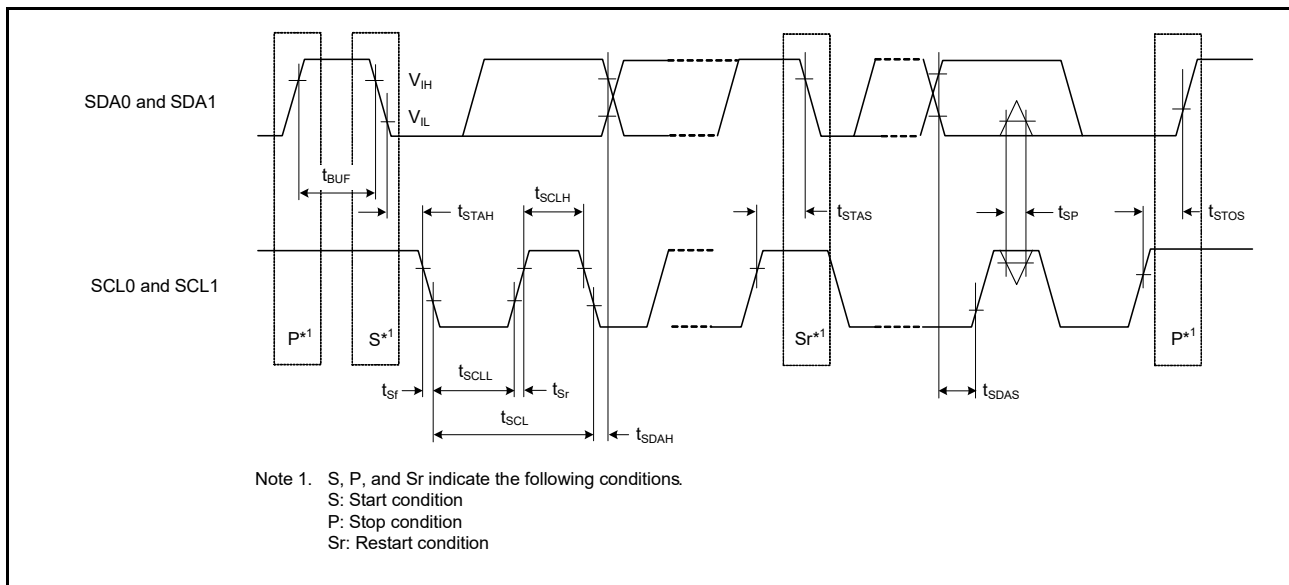


Figure 2.56 I²C bus interface input/output timing

2.3.12 CLKOUT Timing

Table 2.38 CLKOUT timing

Parameter		Symbol	Min	Max	Unit	Test conditions	
CLKOUT	CLKOUT pin output cycle*1	VCC = 2.7 V or above	t _{Cyc}	62.5	-	ns	Figure 2.57
		VCC = 1.8 V or above		125	-		
		VCC = 1.6 V or above		250	-		
CLKOUT	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t _{CH}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
CLKOUT	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t _{CL}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
CLKOUT	CLKOUT pin output rise time	VCC = 2.7 V or above	t _{Cr}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		
CLKOUT	CLKOUT pin output fall time	VCC = 2.7 V or above	t _{Cf}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		

Note 1. When the EXTAL external clock input or an oscillator divided by 1 (the CKOCR.CKOSSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) is used for output from CLKOUT, specifications in Table 2.38 should be satisfied with 45% to 55% of input duty cycle.

Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSSEL[2:0] bits are 001b), set the clock output division ratio to 2 (the CKOCR.CKODIV[2:0] bits are 001b).

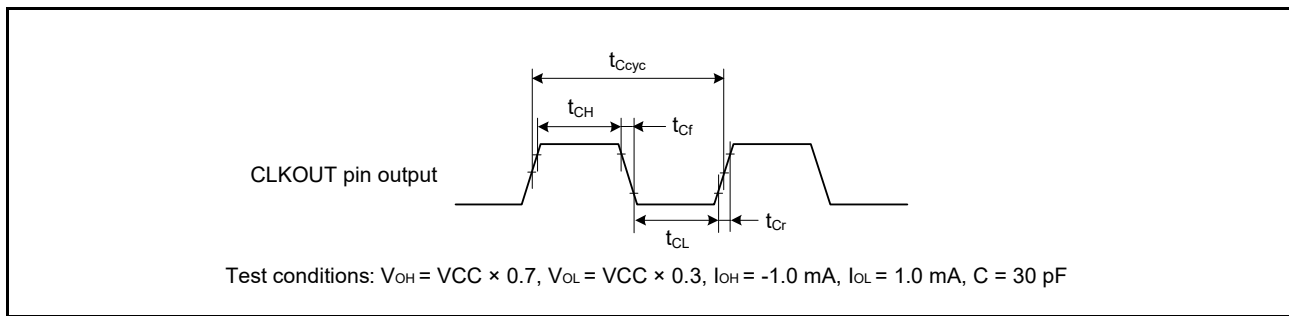


Figure 2.57 CLKOUT output timing

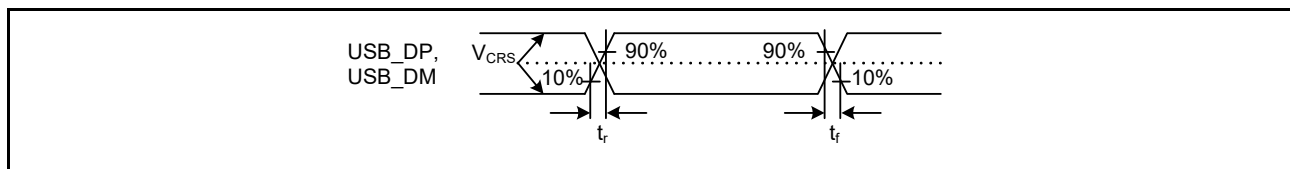
2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.39 USB characteristics

Conditions: VCC = AVCC0 = VCC_USB = 3.0 to 3.6 V, Ta = -20 to +85°C

Parameter		Symbol	Min	Max	Unit	Test conditions	
Input characteristics	Input high level voltage	V_{IH}	2.0	-	V	-	
	Input low level voltage	V_{IL}	-	0.8	V	-	
	Differential input sensitivity	V_{DI}	0.2	-	V	USB_DP - USB_DM	
	Differential common mode range	V_{CM}	0.8	2.5	V	-	
Output characteristics	Output high level voltage	V_{OH}	2.8	VCC_USB	V	$I_{OH} = -200 \mu A$	
	Output low level voltage	V_{OL}	0.0	0.3	V	$I_{OL} = 2 \text{ mA}$	
	Cross-over voltage	V_{CRS}	1.3	2.0	V	Figure 2.58, Figure 2.59, Figure 2.60	
	Rise time	FS	t_r	4	20		ns
		LS		75	300		
	Fall time	FS	t_f	4	20		ns
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11		%
LS			80	125			
Output resistance	Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not necessary.)		
VBUS characteristics	VBUS input voltage	V_{IH}	$VCC \times 0.8$	-	V	-	
		V_{IL}	-	$VCC \times 0.2$	V	-	
Pull-up, pull-down	Pull-down resistor	R_{PD}	14.25	24.80	k Ω	-	
	Pull-up resistor	R_{PUI}	0.9	1.575	k Ω	During idle state	
		R_{PUA}	1.425	3.09	k Ω	During reception	
Battery Charging Specification Ver 1.2	D + sink current	I_{DP_SINK}	25	175	μA	-	
	D - sink current	I_{DM_SINK}	25	175	μA	-	
	DCD source current	I_{DP_SRC}	7	13	μA	-	
	Data detection voltage	V_{DAT_REF}	0.25	0.4	V	-	
	D + source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA	
	D - source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA	


Figure 2.58 USB_DP and USB_DM output timing

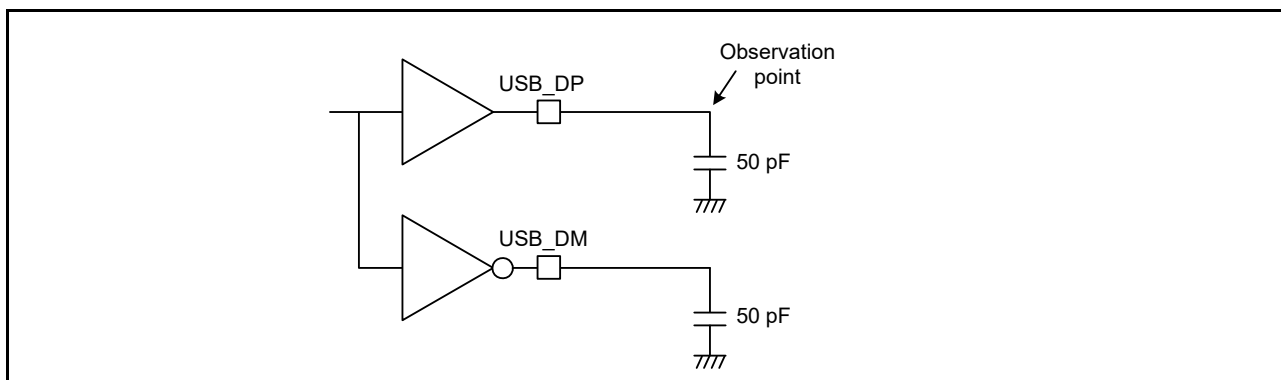


Figure 2.59 Test circuit for Full-Speed (FS) connection

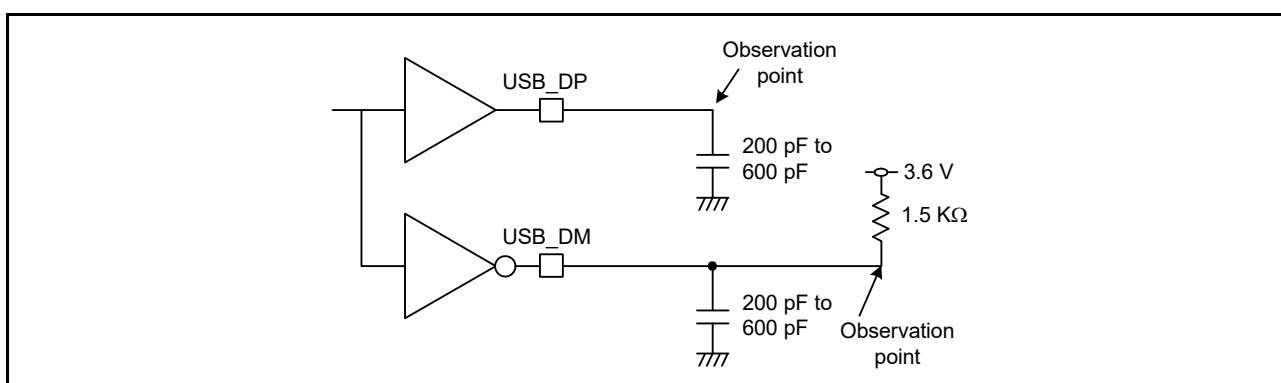


Figure 2.60 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.40 USB regulator

Parameter		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	VCC_USB_LDO ≥ 3.8V	-	-	50	mA	-
	VCC_USB_LDO ≥ 4.5V	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

2.5 ADC14 Characteristics

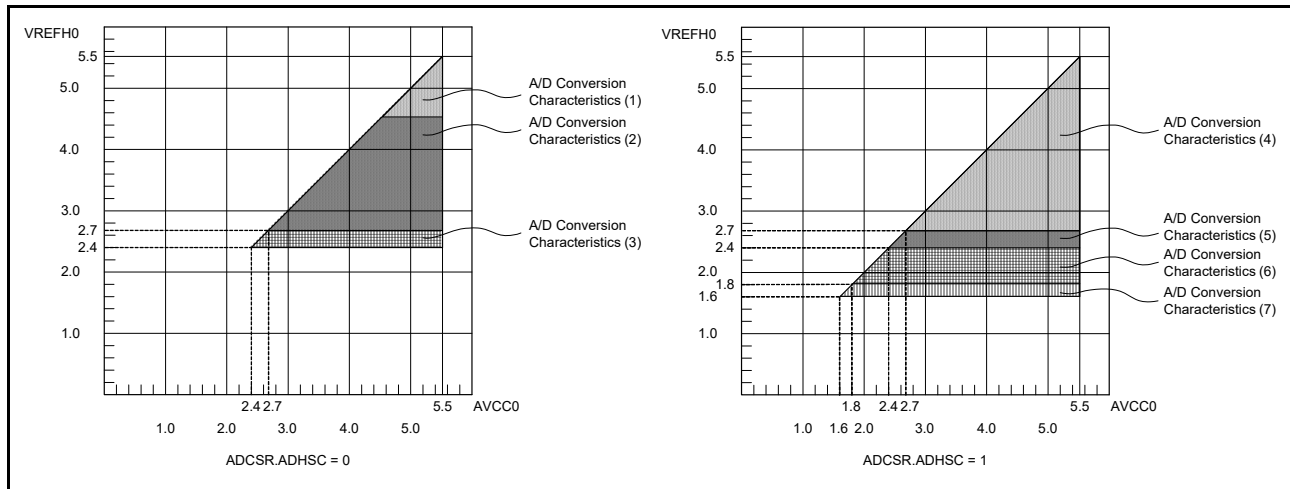


Figure 2.61 AVCC0 to VREFH0 voltage range

Table 2.41 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	64	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.13	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-

Table 2.41 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.80	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.22	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (C_{in}), see section [section 2.2.4, I/O VOH, VOL, and Other Characteristics](#).

Table 2.42 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	48	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	A _{in}	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.94	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.50	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above

Table 2.42 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test Conditions	
Quantization error	-	±0.5	-	LSB	-	
Absolute accuracy	-	±1.25	±5.0	LSB	High-precision channel	
			±8.0	LSB	Other than above	
DNL differential nonlinearity error	-	±1.0	-	LSB	-	
INL integral nonlinearity error	-	±1.0	±3.0	LSB	-	
14-bit mode						
Resolution	-	-	14	Bit	-	
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	1.06	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error	-	±2.0	±18	LSB	High-precision channel	
			±24.0	LSB	Other than above	
Full-scale error	-	±3.0	±18	LSB	High-precision channel	
			±24.0	LSB	Other than above	
Quantization error	-	±0.5	-	LSB	-	
Absolute accuracy	-	±5.0	±20	LSB	High-precision channel	
			±32.0	LSB	Other than above	
DNL differential nonlinearity error	-	±4.0	-	LSB	-	
INL integral nonlinearity error	-	±4.0	±12.0	LSB	-	

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O VOH, VOL, and Other Characteristics](#).

Table 2.43 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test Conditions	
Frequency	1	-	32	MHz	-	
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
				9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
				6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution	-	-	12	Bit	-	

Table 2.43 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.41	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.25	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.59	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.44	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O VOH, VOL, and Other Characteristics](#).

Table 2.44 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	24	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel

Table 2.44 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.25	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.38	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.50	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O VOH, VOL, and Other Characteristics](#).

Table 2.45 A/D conversion characteristics (5) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V

Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	16	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.38	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.06	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.75	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.44	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute

accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (C_{in}), see [section 2.2.4, I/O VOH, VOL, and Other Characteristics](#).

Table 2.46 A/D conversion characteristics (6) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	8	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	3.8 (reference data)	kΩ	High-precision channel
		-	-	8.2 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	6.75	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.13	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±3.0	±8.0	LSB	High-precision channel
				±12.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	7.50	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.88	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±4.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Full-scale error		-	±6.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-

Table 2.46 A/D conversion characteristics (6) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test Conditions
Absolute accuracy	-	±12.0	±32.0	LSB	High-precision channel
			±48.0	LSB	Other than above
DNL differential nonlinearity error	-	±4.0	-	LSB	-
INL integral nonlinearity error	-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O VOH, VOL, and Other Characteristics](#).

Table 2.47 A/D conversion characteristics (7) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test Conditions	
Frequency	1	-	4	MHz	-	
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
				9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	13.1 (reference data)	kΩ	High-precision channel
				14.3 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution	-	-	12	Bit	-	
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	13.5	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
					μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error	-	±1.0	-	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error	-	±1.5	-	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error	-	±0.5	-	LSB	-	
Absolute accuracy	-	±3.0	-	±8.0	LSB	High-precision channel
				±12.0	LSB	Other than above
DNL differential nonlinearity error	-	±1.0	-	LSB	-	
INL integral nonlinearity error	-	±1.0	±3.0	LSB	-	
14-bit mode						
Resolution	-	-	14	Bit	-	

Table 2.47 A/D conversion characteristics (7) in low-power A/D conversion mode (2 of 2)

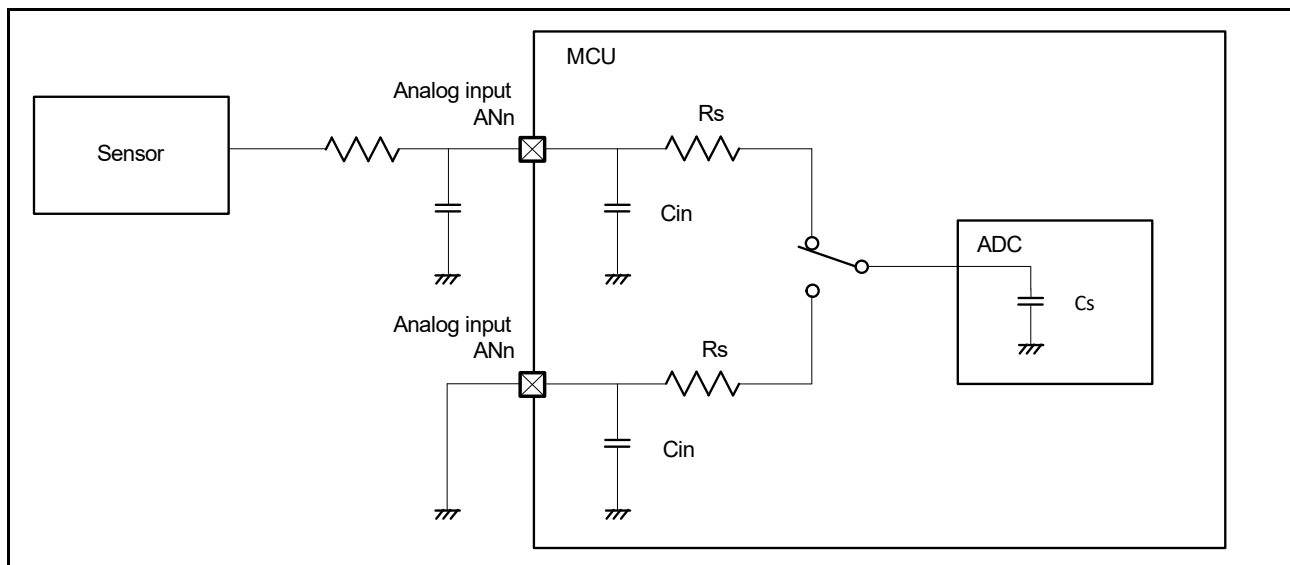
Conditions: $V_{CC} = AV_{CC0} = 1.6$ to 5.5 V ($AV_{CC0} = V_{CC}$ when $V_{CC} < 2.0$ V), $V_{REFH0} = 1.6$ to 5.5 V, $V_{SS} = AV_{SS0} = V_{REFL0} = 0$
Reference voltage range applied to the V_{REFH0} and V_{REFL0} .

Parameter		Min	Typ	Max	Unit	Test Conditions
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 k Ω	15.0	-	-	μ s	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		21.75	-	-	μ s	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	± 4.0	± 30.0	LSB	High-precision channel
				± 40.0	LSB	Other than above
Full-scale error		-	± 6.0	± 30.0	LSB	High-precision channel
				± 40.0	LSB	Other than above
Quantization error		-	± 0.5	-	LSB	-
Absolute accuracy		-	± 12.0	± 32.0	LSB	High-precision channel
				± 48.0	LSB	Other than above
DNL differential nonlinearity error		-	± 4.0	-	LSB	-
INL integral nonlinearity error		-	± 4.0	± 12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (C_{in}), see [section 2.2.4, I/O VOH, VOL, and Other Characteristics](#).

**Figure 2.62 Equivalent circuit for analog input****Table 2.48 14-bit A/D converter channel classification (1 of 2)**

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN013	$AV_{CC0} = 1.6$ to 5.5 V	Pins AN000 to AN013 cannot be used as general I/O, IRQ2 input, or for TS transmission when the A/D converter is in use.
Normal-precision channel	AN016 to AN022		-
Internal reference voltage input channel	Internal reference voltage	$AV_{CC0} = 2.0$ to 5.5 V	-

Table 2.48 14-bit A/D converter channel classification (2 of 2)

Classification	Channel	Conditions	Remarks
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	-

Table 2.49 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Frequency*3	1	-	2	MHz	-
Sampling time*4	5.0	-	-	μs	-

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.

Note 2. The 14-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 14-bit A/D converter.

Note 3. This is a parameter for ADC14 when the internal reference voltage is used as the high-potential reference voltage.

Note 4. This is a parameter for ADC14 when the internal reference voltage is selected for an analog input channel in ADC14.

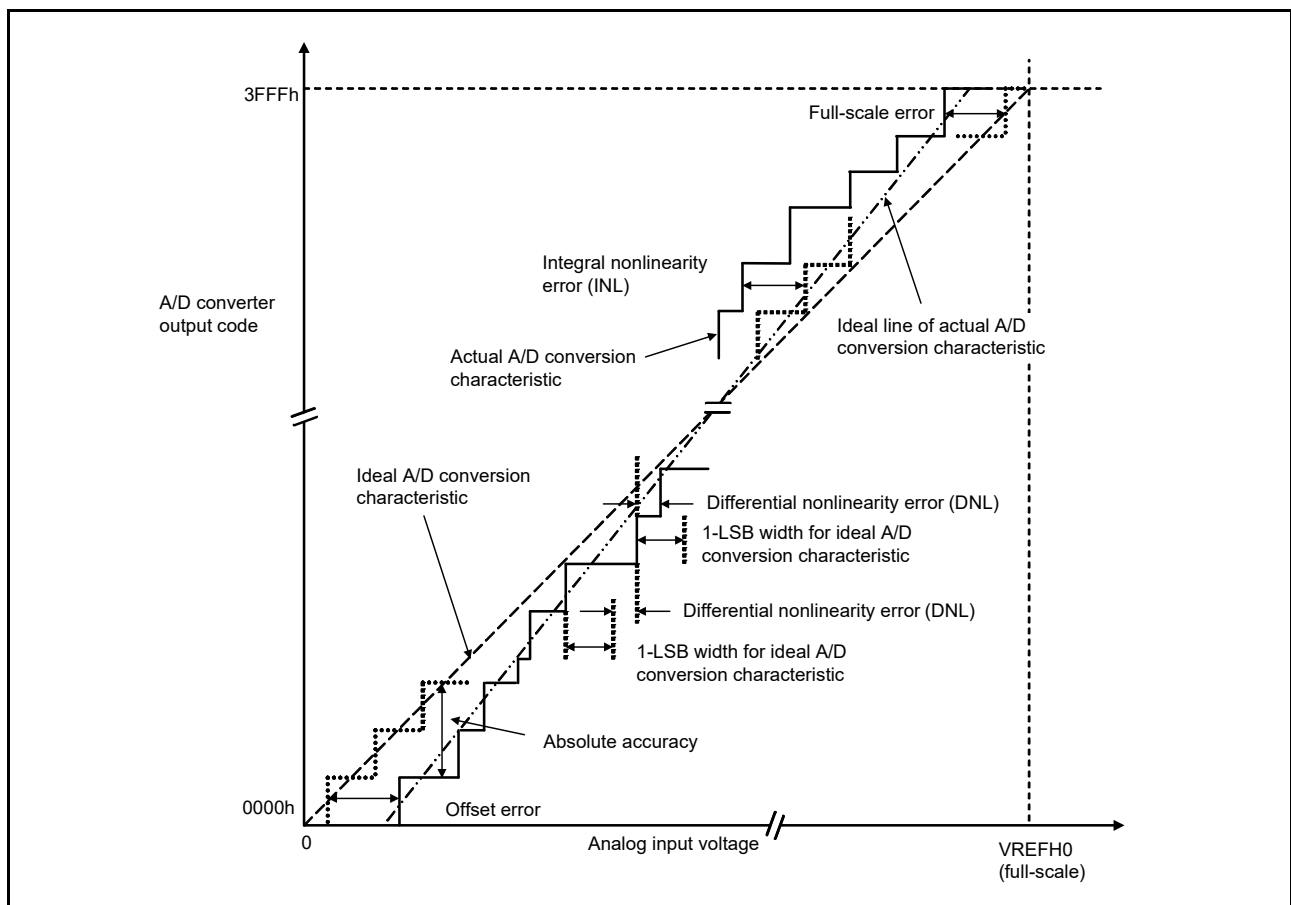


Figure 2.63 Illustration of 14-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage $V_{REFH0} = 3.072$ V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ± 5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC8 Characteristics

Table 2.50 D/A conversion characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter		Min	Typ	Max	Unit	Test conditions
Resolution		-	-	8	bit	-
Charge pump stabilization time		-	-	100	μs	-
Conversion time	VCC = 2.7 to 5.5V	-	-	3.0	μs	35-pF capacitive load
	VCC = 1.8 to 2.7V	-	-	6.0	μs	
Absolute accuracy	VCC = 2.4 to 5.5V	-	-	±3.0	LSB	2-MΩ resistive load
	VCC = 1.8 to 2.4V	-	-	±3.5		
	VCC = 2.4 to 5.5V	-	-	±2.0	LSB	4-MΩ resistive load
	VCC = 1.8 to 2.4V	-	-	±2.5		
RO output resistance		-	7.4	-	kΩ	-

2.7 TSN Characteristics

Table 2.51 TSN characteristics

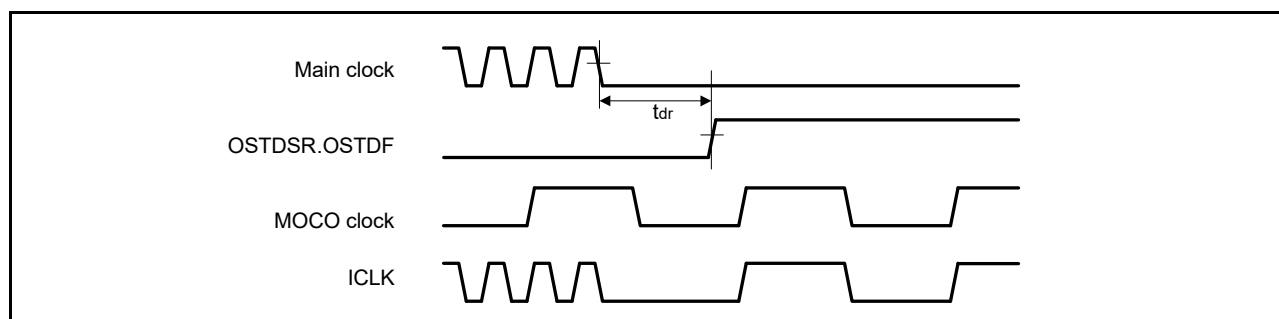
Conditions: VCC = AVCC0 = 2.0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.5	-	°C	2.4 V or above
		-	±2.0	-	°C	Below 2.4 V
Temperature slope	-	-	-3.65	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.05	-	V	VCC = 3.3 V
Temperature sensor start time	t _{START}	-	-	5	μs	-
Sampling time	-	5	-	-	μs	-

2.8 OSC Stop Detect Characteristics

Table 2.52 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t _{dr}	-	-	1	ms	Figure 2.64


Figure 2.64 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.53 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 2.65, Figure 2.66
	Voltage detection circuit (LVD0)*2	V_{det0_0}	3.68	3.85	4.00	V	Figure 2.67 At falling edge VCC
V_{det0_1}		2.68	2.85	2.96			
V_{det0_2}		2.38	2.53	2.64			
V_{det0_3}		1.78	1.90	2.02			
V_{det0_4}		1.60	1.69	1.82			
Voltage detection circuit (LVD1)*3	V_{det1_0}	4.13	4.29	4.45	V	Figure 2.68 At falling edge VCC	
	V_{det1_1}	3.98	4.16	4.30			
	V_{det1_2}	3.86	4.03	4.18			
	V_{det1_3}	3.68	3.86	4.00			
	V_{det1_4}	2.98	3.10	3.22			
	V_{det1_5}	2.89	3.00	3.11			
	V_{det1_6}	2.79	2.90	3.01			
	V_{det1_7}	2.68	2.79	2.90			
	V_{det1_8}	2.58	2.68	2.78			
	V_{det1_9}	2.48	2.58	2.68			
	V_{det1_A}	2.38	2.48	2.58			
	V_{det1_B}	2.10	2.20	2.30			
	V_{det1_C}	1.84	1.96	2.05			
	V_{det1_D}	1.74	1.86	1.95			
	V_{det1_E}	1.63	1.75	1.84			
V_{det1_F}	1.60	1.65	1.73				
Voltage detection circuit (LVD2)*4	V_{det2_0}	4.11	4.31	4.48	V	Figure 2.69 At falling edge VCC	
	V_{det2_1}	3.97	4.17	4.34			
	V_{det2_2}	3.83	4.03	4.20			
	V_{det2_3}	3.64	3.84	4.01			

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Note 2. # in the symbol $V_{det0_#}$ denotes the value of the OFS1.VDSEL1[2:0] bits.

Note 3. # in the symbol $V_{det1_#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.

Note 4. # in the symbol $V_{det2_#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.54 Power-on reset circuit and voltage detection circuit characteristics (2) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0:enable	t_{POR}	-	1.7	-	ms	-
	LVD0:disable	t_{POR}	-	1.3	-	ms	-
Wait time after voltage monitor 0,1,2 reset cancellation	LVD0:enable*1	$t_{LVD0,1,2}$	-	0.6	-	ms	-
	LVD0:disable*2	$t_{LVD1,2}$	-	0.2	-	ms	-
Response delay*3		t_{det}	-	-	350	μ s	Figure 2.65, Figure 2.66
Minimum VCC down time		t_{VOFF}	450	-	-	μ s	Figure 2.65, VCC = 1.0 V or above

Table 2.54 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset enable time	$t_{W(POR)}$	1	-	-	ms	Figure 2.66, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	$T_d(E-A)$	-	-	300	μ s	Figure 2.68, Figure 2.69
Hysteresis width (POR)	V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_F} selected.
		-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0

Note 2. When OFS1.LVDAS = 1

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.

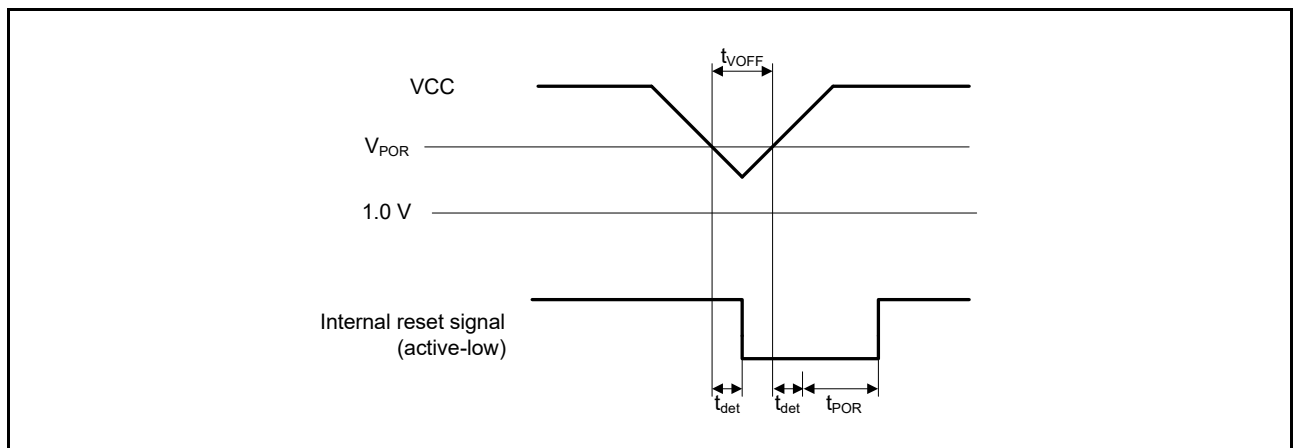


Figure 2.65 Voltage detection reset timing

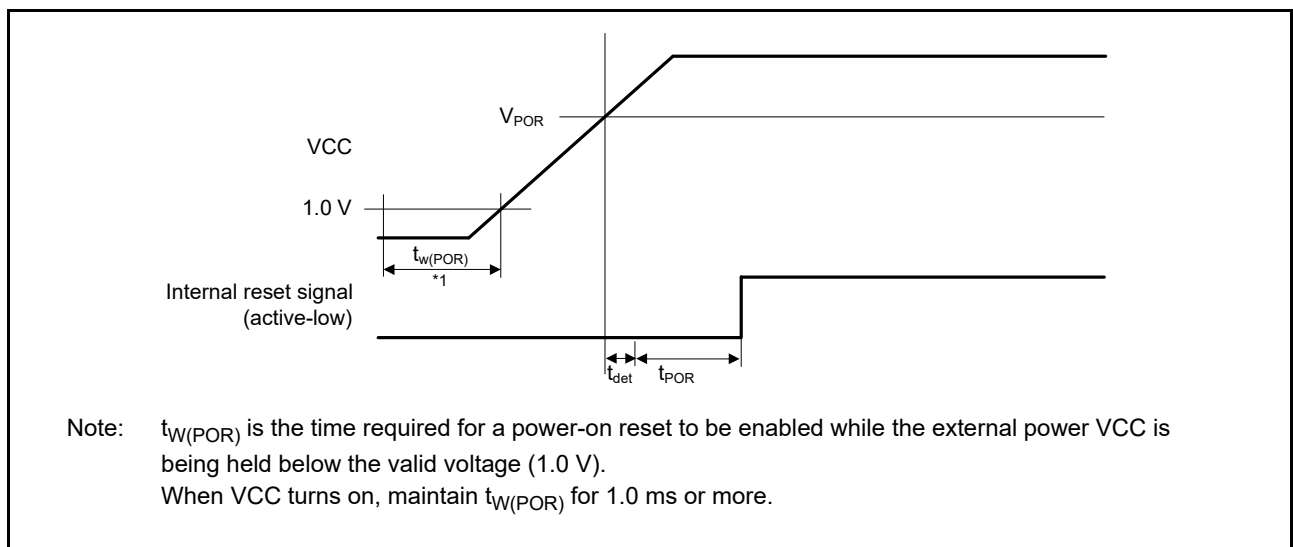


Figure 2.66 Power-on reset timing

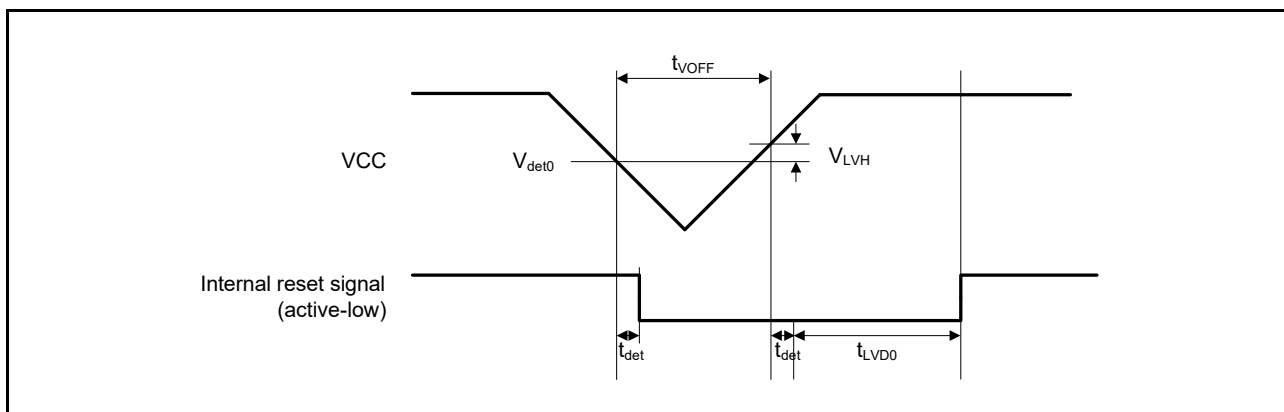


Figure 2.67 Voltage detection circuit timing (V_{det0})

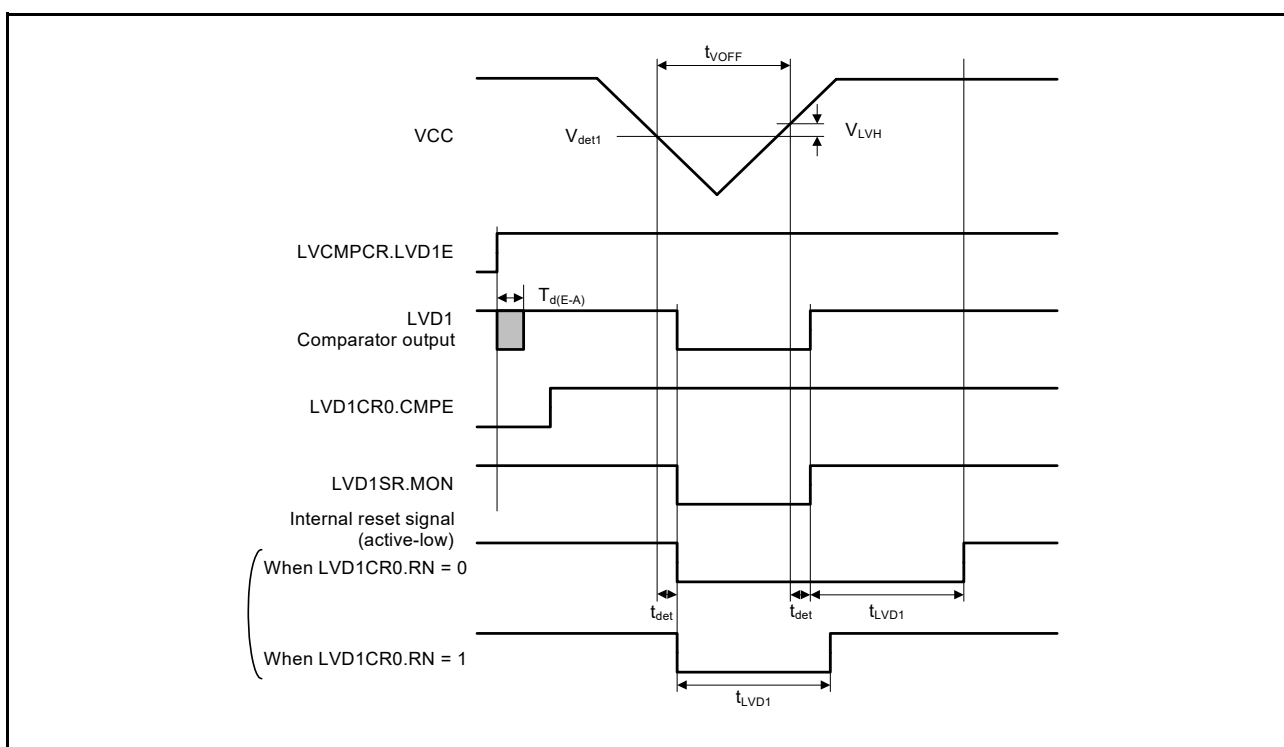


Figure 2.68 Voltage detection circuit timing (V_{det1})

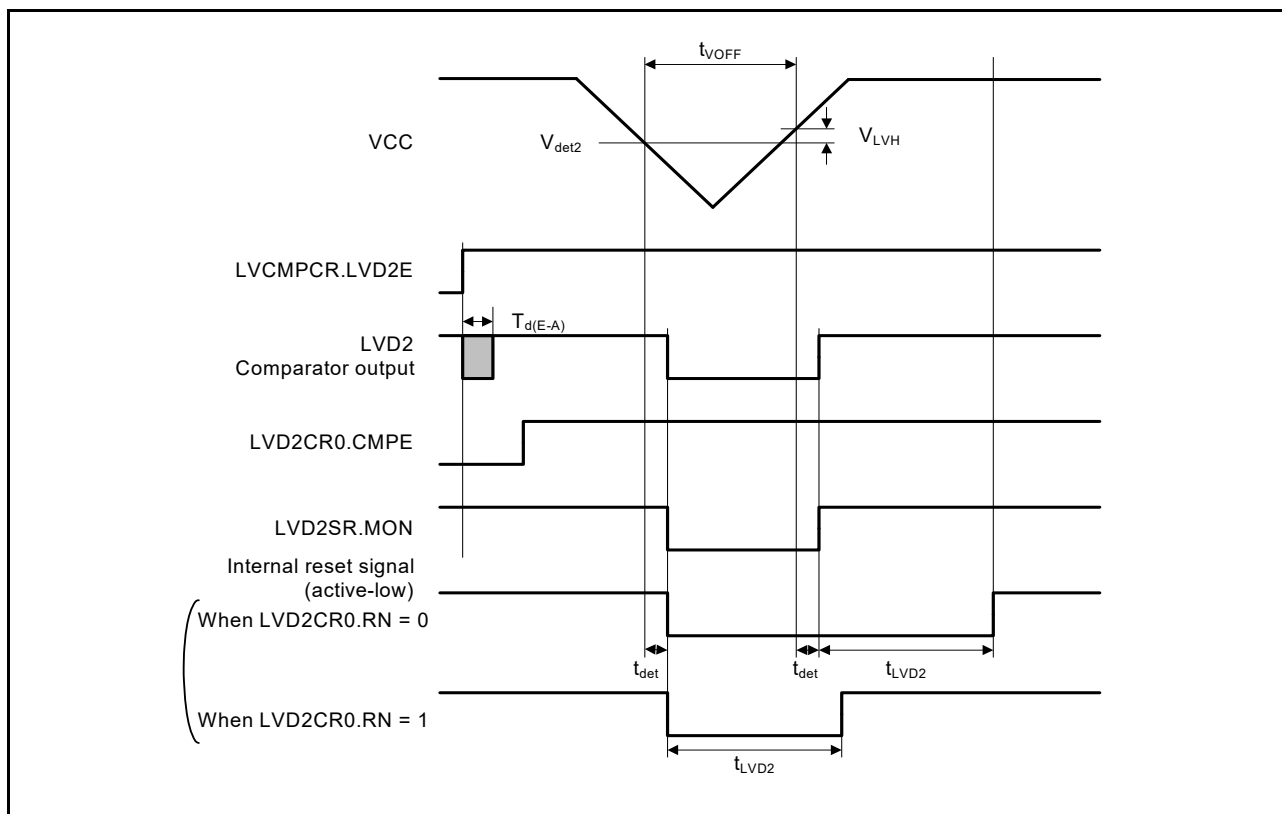


Figure 2.69 Voltage detection circuit timing (V_{det2})

2.10 CTSU Characteristics

Table 2.55 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C _{tscap}	9	10	11	nF	-
TS pin capacitive load	C _{base}	-	-	50	pF	-
Permissible output high current	ΣIoH	-	-	-24	mA	When the mutual capacitance method is applied

2.11 Comparator Characteristics

Table 2.56 ACMPHS characteristics

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V _{IOCOMP}	-	±5	±40	mV	-
Input voltage range	V _{ICPM}	0	-	AVCC0	V	-
Output delay time	T _d	-	50	100	ns	Input amplitude ±100 mV
Stabilization wait time during input channel switching*1	T _{WAIT}	300	-	-	ns	Input amplitude ±100 mV
Operation stabilization wait time*2	T _{cmp}	1	-	-	μs	3.3 V ≤ AVCC0 ≤ 5.5 V
		3	-	-	μs	2.7 V ≤ AVCC0 < 3.3 V

Note 1. Period from when the comparator input channel is switched until the switched result reflects in its output.

Note 2. Period from when comparator operation is enabled (CPMCTL.HCMPON = 1) until the comparator satisfies the DC/AC characteristics.

Table 2.57 ACMLP characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Input voltage range	IVREF0	V _{REF}	0	-	VCC - 1.4*1	V	-
	IVREF1 (Standard mode)		0	-	VCC - 1.4	V	
	IVREF1 (Window mode)		1.4*1	-	VCC	V	
	IVCMP0, IVCMP1		V _I	0	-	VCC	
Internal reference voltage	-	1.36	1.44	1.50	V	-	
Output delay	Comparator high-speed mode (Standard mode)	T _d	-	-	1.2	μs	VCC = 3.0 Slew rate of input signal > 50 mV/μs
	Comparator high-speed mode (Window mode)				2.0	μs	
	Comparator low-speed mode (Standard mode)				5.0	μs	
Offset voltage	Comparator high-speed mode (Standard mode)	-	-	-	50	mV	-
	Comparator high-speed mode (Window mode)				60	mV	
	Comparator low-speed mode (Standard mode)				40	mV	
Operation stabilization wait time	T _{cmp}	100	-	-	μs	-	

Note 1. In window mode, be sure to satisfy the following condition: IVREF1 - IVREF0 ≥ 0.2 V.

2.12 OPAMP Characteristics

Table 2.58 OPAMP characteristics (1 of 2)

Conditions: 1.8 V ≤ AVCC0 = VCC ≤ 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Common mode input range	V _{icm1}	Low-power mode	0.1	-	AVCC0 - 0.5	V
	V _{icm2}	High-speed mode	0.2	-	AVCC0 - 0.6	
Output voltage range	V _{o1}	Low-power mode	0.1	-	AVCC0 - 0.1	V
	V _{o2}	High-speed mode	0.1	-	AVCC0 - 0.1	
Input offset voltage	V _{ioff1}	Low-power mode	-7	-	7	mV
	V _{ioff2}	High-speed mode	-5	-	5	

Table 2.58 OPAMP characteristics (2 of 2)
 Conditions: $1.8\text{ V} \leq AVCC0 = VCC \leq 5.5\text{ V}$, $VSS = AVSS0 = 0\text{ V}$

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Open gain	A_V	-		80	120	-	dB
Gain-bandwidth (GB) product	GBW1	Low-power mode		-	0.012	-	MHz
	GBW2	High-speed mode		-	1.7	-	
Phase margin	PM	CL = 20 pF		50	-	-	deg
Gain margin	GM	CL = 20 pF		10	-	-	dB
Equivalent input noise	V_{noise1}	f = 10 Hz	Low-power mode	-	700	-	nV/ √Hz
	V_{noise2}	f = 1 kHz		-	400	-	
	V_{noise3}	f = 1 kHz	High-speed mode	-	90	-	
	V_{noise4}	f = 100 kHz		-	50	-	
Power supply reduction ratio	PSRR	-		-	90	-	dB
Common mode signal reduction ratio	CMRR	-		-	90	-	dB
Stabilization wait time	T_{std1}	CL = 20 pF Only operational amplifier is activated.*1	Low-power mode VCC < 3.6V	1800	-	-	μs
			Low-power mode VCC < 5.5V	2500	-	-	
	T_{std2}		High-speed mode	13	-	-	
	T_{std3}		Low-power mode VCC < 3.6V	1800	-	-	
			Low-power mode VCC < 5.5V	2500	-	-	
	T_{std4}		High-speed mode	13	-	-	
Settling time	T_{set1}	CL = 20 pF	Low-power mode VCC < 3.6V	-	-	1400	μs
			Low-power mode VCC < 5.5V	-	-	2000	μs
	T_{set2}		High-speed mode	-	-	13	μs
Slew rate	T_{slew1}	CL = 20 pF	Low-power mode	-	0.005	-	V/μs
	T_{slew2}		High-speed mode	-	1.1	-	V/μs
Load current	I_{load1}	Low-power mode		-100	-	100	μA
	I_{load2}	High-speed mode		-100	-	100	
Load capacitance	CL	-		-	-	20	pF

Note 1. When the operational amplifier and the reference current circuit have already been activated.

2.13 Flash Memory Characteristics

2.13.1 Code Flash Memory Characteristics

Table 2.59 Code flash characteristics (1)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1	N _{PEC}	1000	-	-	Times	-
Data hold time	After 1000 times N _{PEC}	t _{DRP}	20*2, *3	-	Year	T _a = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 2.60 Code flash characteristics (2)

High-speed operating mode

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter	Symbol	ICLK = 1 MHz			ICLK = 32 MHz			Unit	
		Min	Typ	Max	Min	Typ	Max		
Programming time	4 bytes	t _{P4}	-	116	998	-	54	506	μs
Erasure time	1 KB	t _{E1K}	-	9.03	287	-	5.67	222	ms
Blank check time	4 bytes	t _{BC4}	-	-	56.8	-	-	16.6	μs
	1 KB	t _{BC1K}	-	-	1899	-	-	140	μs
Erase suspended time		t _{SED}	-	-	22.5	-	-	10.7	μs
Startup area switching setting time		t _{SAS}	-	21.9	585	-	12.1	447	ms
Access window time		t _{AWS}	-	21.9	585	-	12.1	447	ms
OCD/serial programmer ID setting time		t _{OSIS}	-	21.9	585	-	12.1	447	ms
Flash memory mode transition wait time 1		t _{DIS}	2	-	-	2	-	-	μs
Flash memory mode transition wait time 2		t _{MS}	5	-	-	5	-	-	μs

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.

Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.61 Code flash characteristics (3)

Middle-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4 bytes	t _{P4}	-	157	1411	-	101	966	μs
Erasure time	1 KB	t _{E1K}	-	9.10	289	-	6.10	228	ms
Blank check time	2 bytes	t _{BC4}	-	-	87.7	-	-	52.5	μs
	1 KB	t _{BC1K}	-	-	1930	-	-	414	μs
Erase suspended time		t _{SED}	-	-	32.7	-	-	21.6	μs
Startup area switching setting time		t _{SAS}	-	22.8	592	-	14.2	465	ms
Access window time		t _{AWS}	-	22.8	592	-	14.2	465	ms
OCD/serial programmer ID setting time		t _{OSIS}	-	22.8	592	-	14.2	465	ms
Flash memory mode transition wait time 1		t _{DIS}	2	-	-	2	-	-	μs
Flash memory mode transition wait time 2		t _{MS}	720	-	-	720	-	-	ns

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.

Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.13.2 Data Flash Memory Characteristics

Table 2.62 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N _{DPEC}	100000	1000000	-	Times	-
Data hold time	After 10000 times of N _{DPEC}	t _{DDRP}	20*2, *3	-	-	Year	Ta = +85°C
	After 100000 times of N _{DPEC}		5*2, *3	-	-	Year	
	After 1000000 times of N _{DPEC}		-	1*2, *3	-	Year	

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. These results are obtained from reliability testing.

Table 2.63 Data flash characteristics (2)

High-speed operating mode

Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	ICLK = 4 MHz			ICLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t _{DP1}	-	52.4	463	-	42.1	387	μs
Erase time	1-KB	t _{DE1K}	-	8.98	286	-	6.42	237	ms
Blank check time	1-byte	t _{DBC1}	-	-	24.3	-	-	16.6	μs
	1-KB	t _{DBC1K}	-	-	1872	-	-	512	μs
Suspended time during erasing		t _{DSED}	-	-	13.0	-	-	10.7	μs
Data flash STOP recovery time		t _{DSTOP}	5	-	-	5	-	-	μs

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.

Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.64 Data flash characteristics (3)

Middle-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	ICLK = 4 MHz			ICLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t _{DP1}	-	94.7	886	-	89.3	849	μs
Erase time	1-KB	t _{DE1K}	-	9.59	299	-	8.29	273	ms
Blank check time	1-byte	t _{DBC1}	-	-	56.2	-	-	52.5	μs
	1-KB	t _{DBC1K}	-	-	2.17	-	-	1.51	ms
Suspended time during erasing		t _{DSED}	-	-	23.0	-	-	21.7	μs
Data flash STOP recovery time		t _{DSTOP}	720	-	-	720	-	-	ns

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.

Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.13.3 Serial Wire Debug (SWD)

Table 2.65 SWD characteristics (1) (1 of 2)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	t _{SWCKcyc}	80	-	-	ns	Figure 2.70
SWCLK clock high pulse width	t _{SWCKH}	35	-	-	ns	
SWCLK clock low pulse width	t _{SWCKL}	35	-	-	ns	
SWCLK clock rise time	t _{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t _{SWCKf}	-	-	5	ns	

Table 2.65 SWD characteristics (1) (2 of 2)

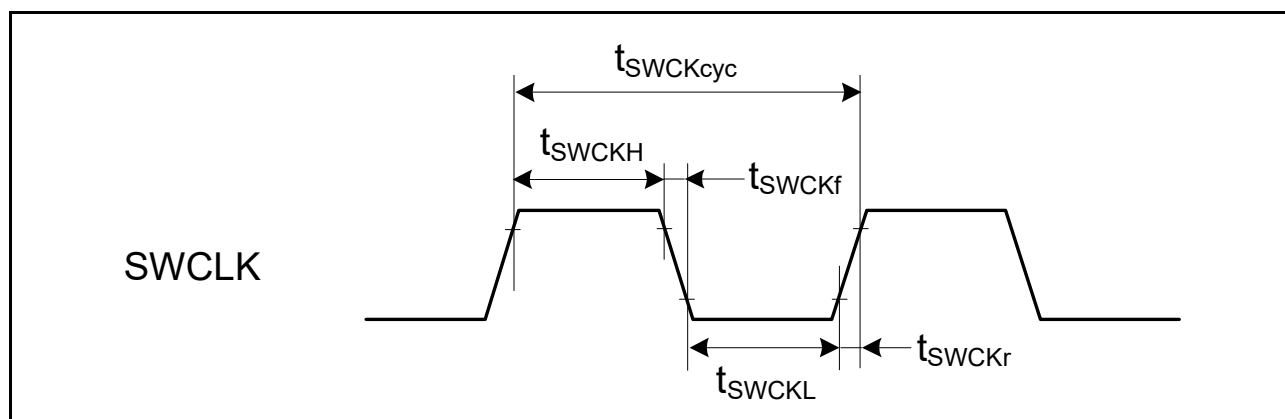
Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWDIO setup time	t_{SWDS}	16	-	-	ns	Figure 2.71
SWDIO hold time	t_{SWDH}	16	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	70	ns	

Table 2.66 SWD characteristics (2)

Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	t_{SWCKcyc}	250	-	-	ns	Figure 2.70
SWCLK clock high pulse width	t_{SWCKH}	120	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	Figure 2.71
SWDIO setup time	t_{SWDS}	50	-	-	ns	
SWDIO hold time	t_{SWDH}	50	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	150	ns	

**Figure 2.70 SWD SWCLK timing**

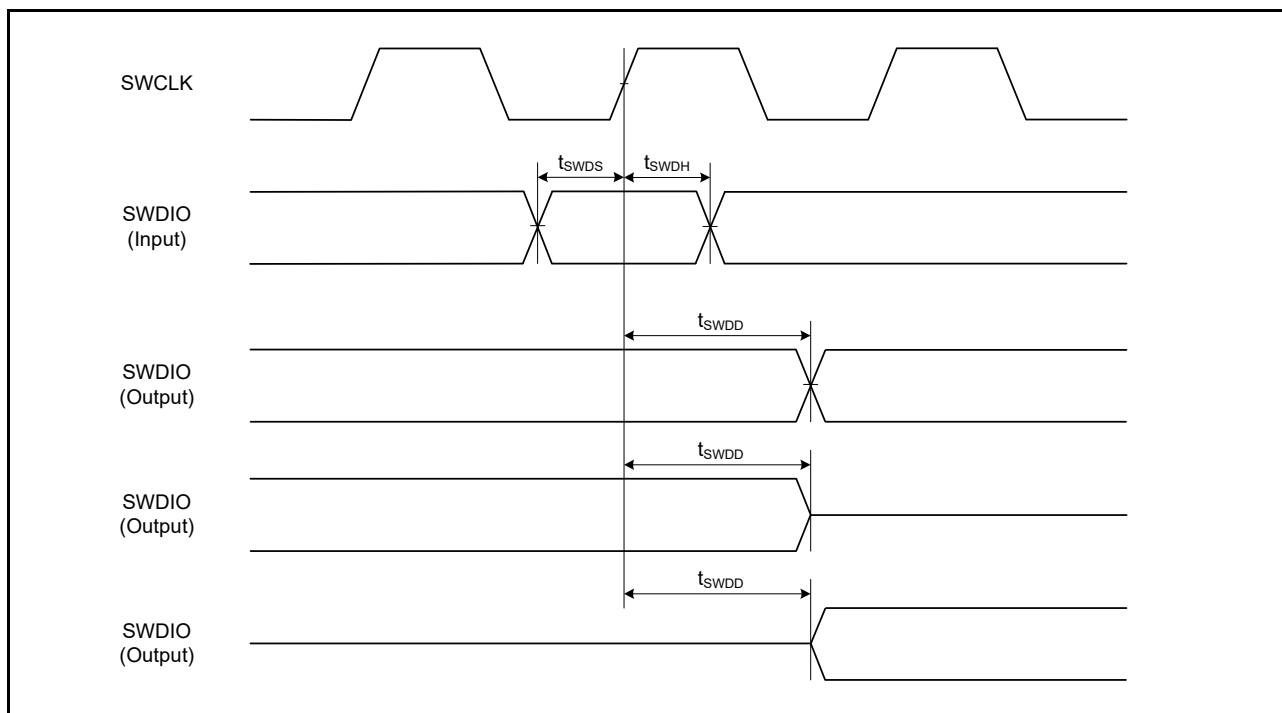


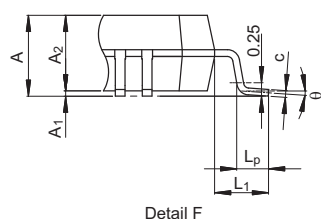
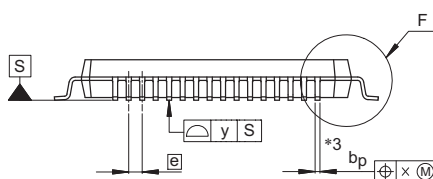
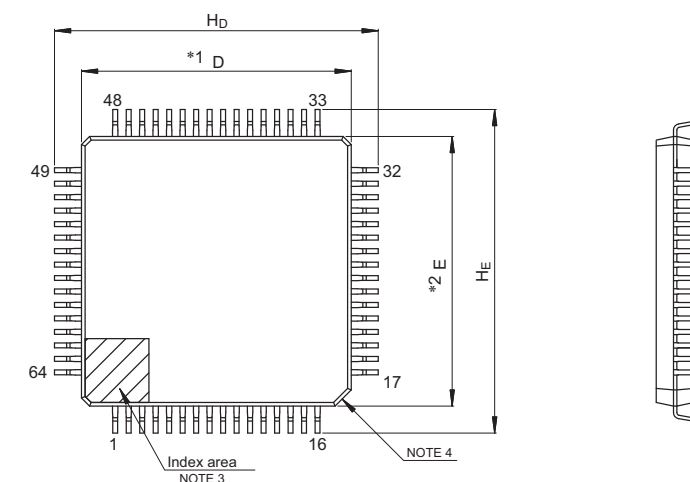
Figure 2.71 SWD input/output timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



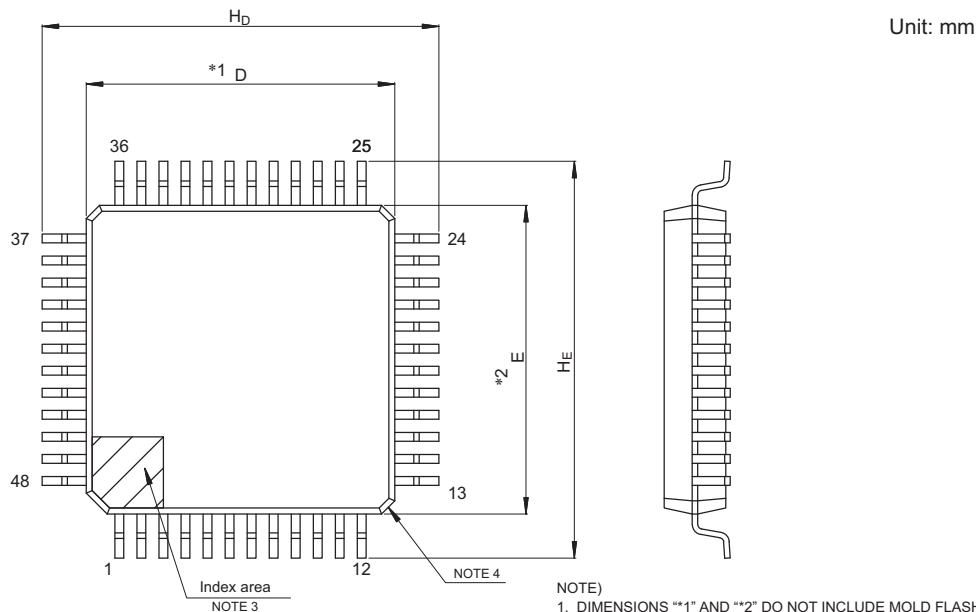
- NOTE)
1. DIMENSIONS **1" AND **2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3" DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A ₂	—	1.4	—
H _D	11.8	12.0	12.2
H _E	11.8	12.0	12.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

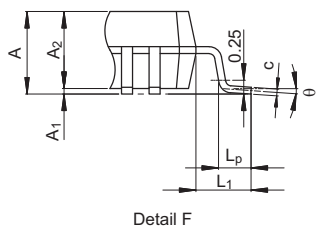
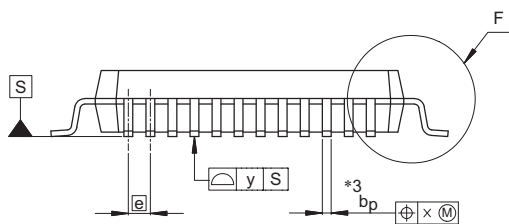
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Figure 1.1 LQFP 64-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2



- NOTE)
1. DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A ₂	—	1.4	—
H _D	8.8	9.0	9.2
H _E	8.8	9.0	9.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

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Figure 1.2 LQFP 48-pin

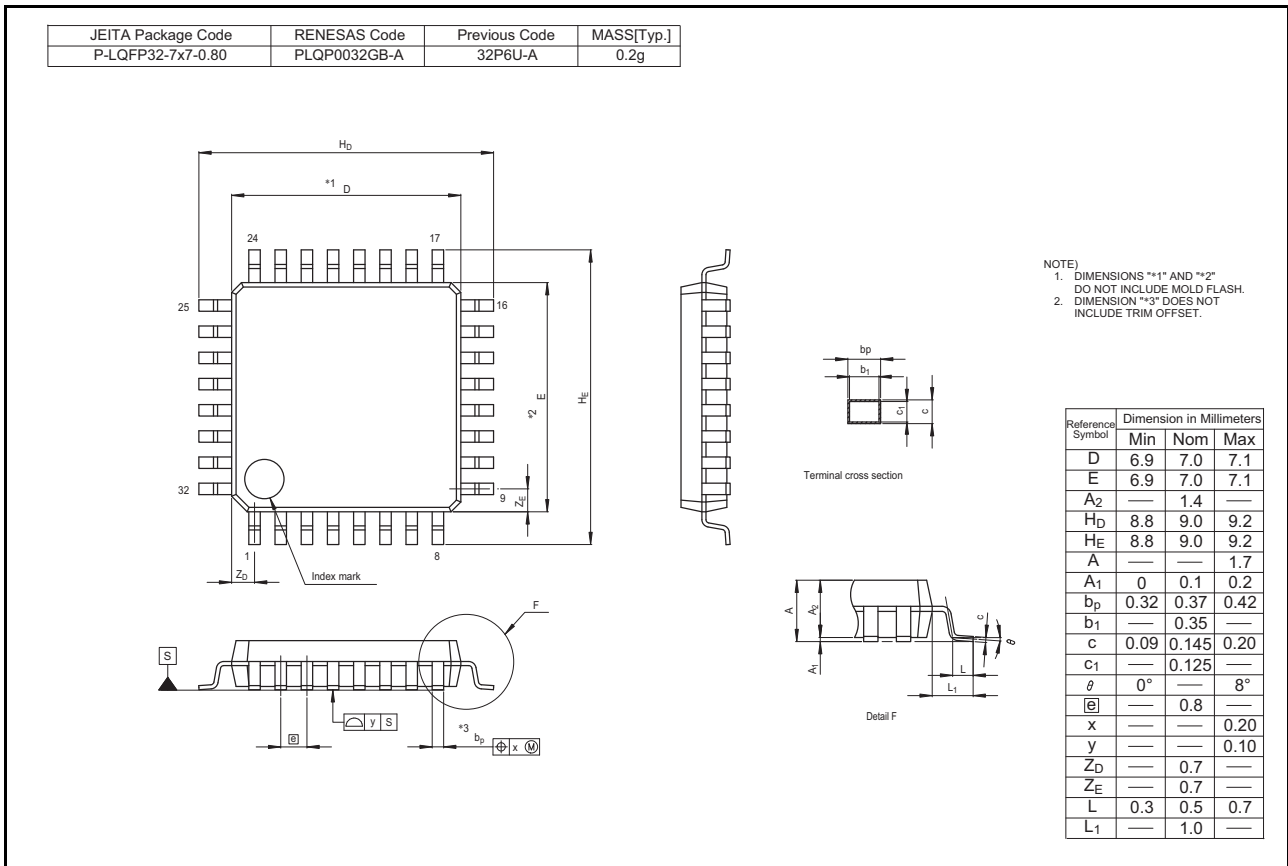


Figure 1.3 LQFP 32-pin

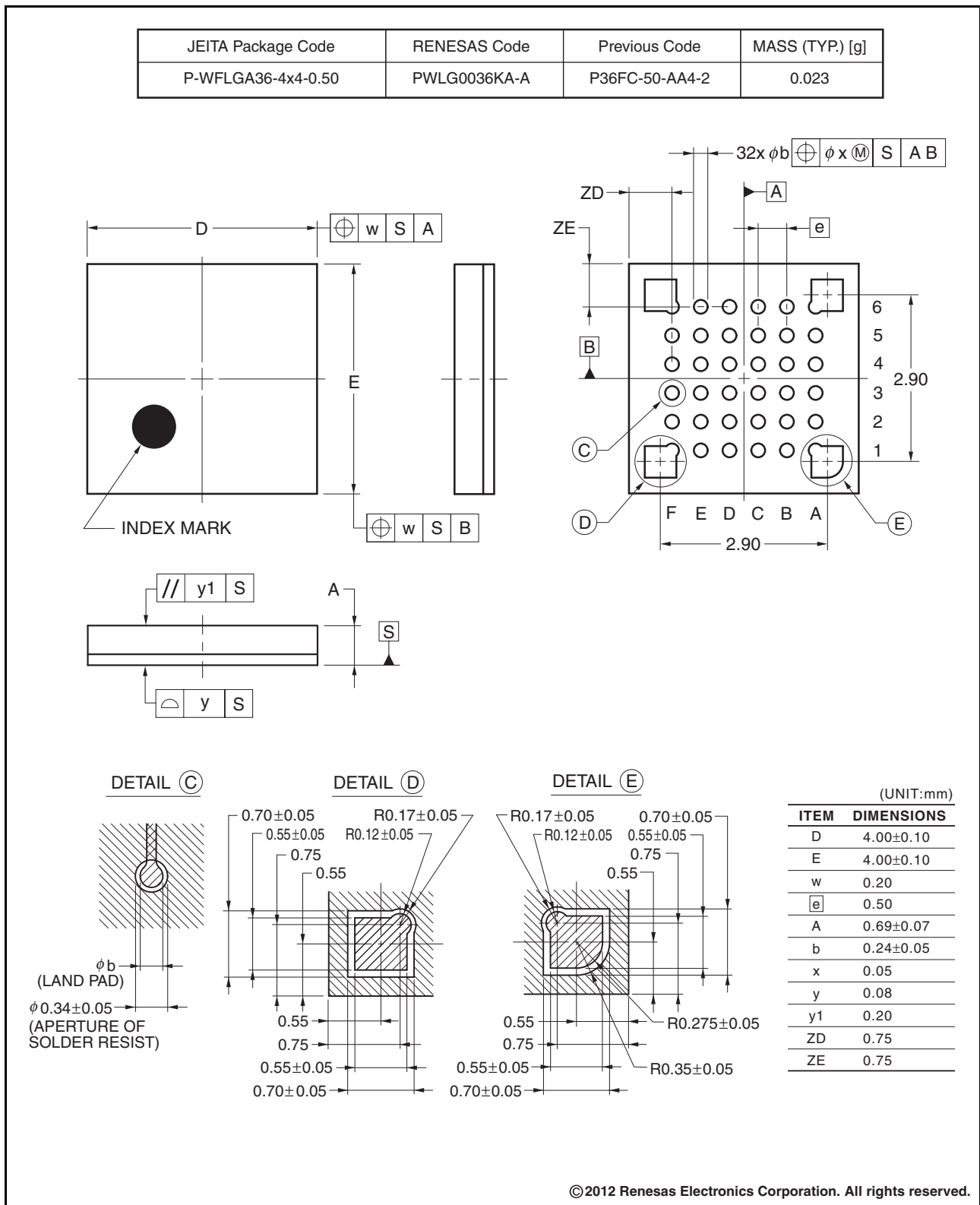
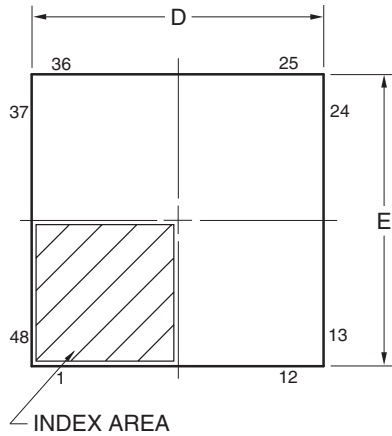
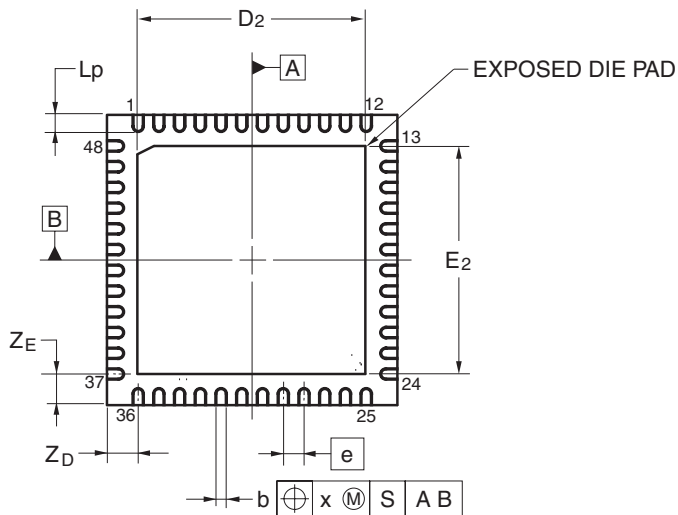
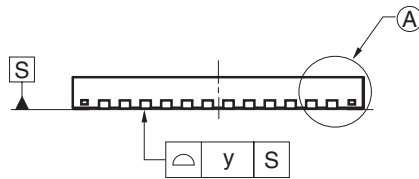
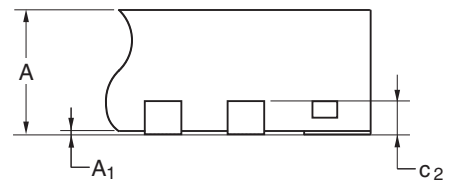


Figure 1.4 LGA 36-pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13



DETAIL OF (A) PART

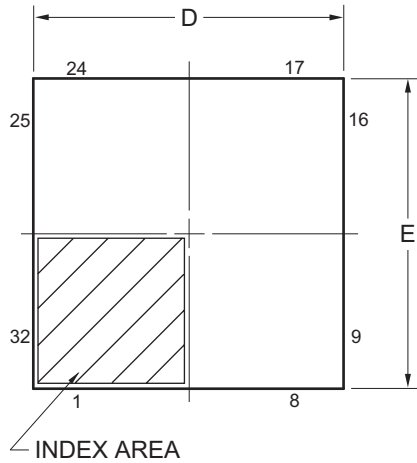


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A ₁	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
L _p	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z _D	—	0.75	—
Z _E	—	0.75	—
c ₂	0.15	0.20	0.25
D ₂	—	5.50	—
E ₂	—	5.50	—

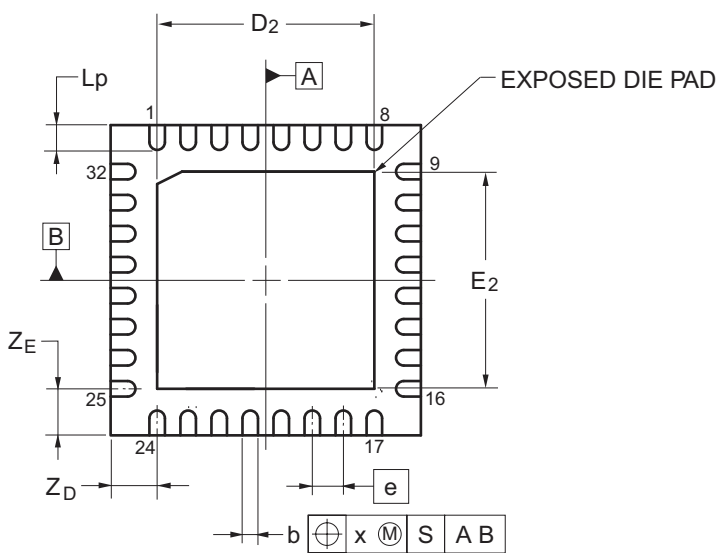
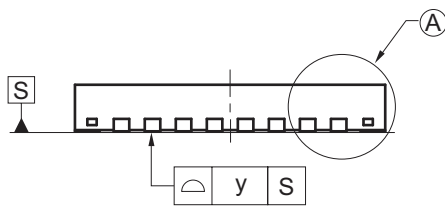
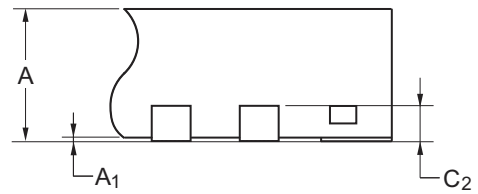
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Figure 1.5 QFN 48-pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06



DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	—	—	0.80
A ₁	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
L _p	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z _D	—	0.75	—
Z _E	—	0.75	—
c ₂	0.15	0.20	0.25
D ₂	—	3.50	—
E ₂	—	3.50	—

Figure 1.6 QFN 32-pin

Revision History	S128 Microcontroller Group Datasheet
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Rev.	Date	Summary
1.00	Feb 23, 2016	1st release
1.10	Nov 28, 2018	Updated for 1.10

Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

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S128 Microcontroller Group Datasheet

Publication Date: Rev.1.10 Nov 28, 2018

Published by: Renesas Electronics Corporation

General Precautions

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)



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