

# RMLV0416E Series

4Mb Advanced LPSRAM (256-kword × 16-bit)

R10DS0205EJ0300  
Rev.3.00  
2021.8.18

## Description

The RMLV0416E Series is a family of 4-Mbit static RAMs organized 262,144-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0416E Series has realized higher density, higher performance and low power consumption. The RMLV0416E Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 44-pin TSOP (II) or 48-ball fine pitch ball grid array.

## Features

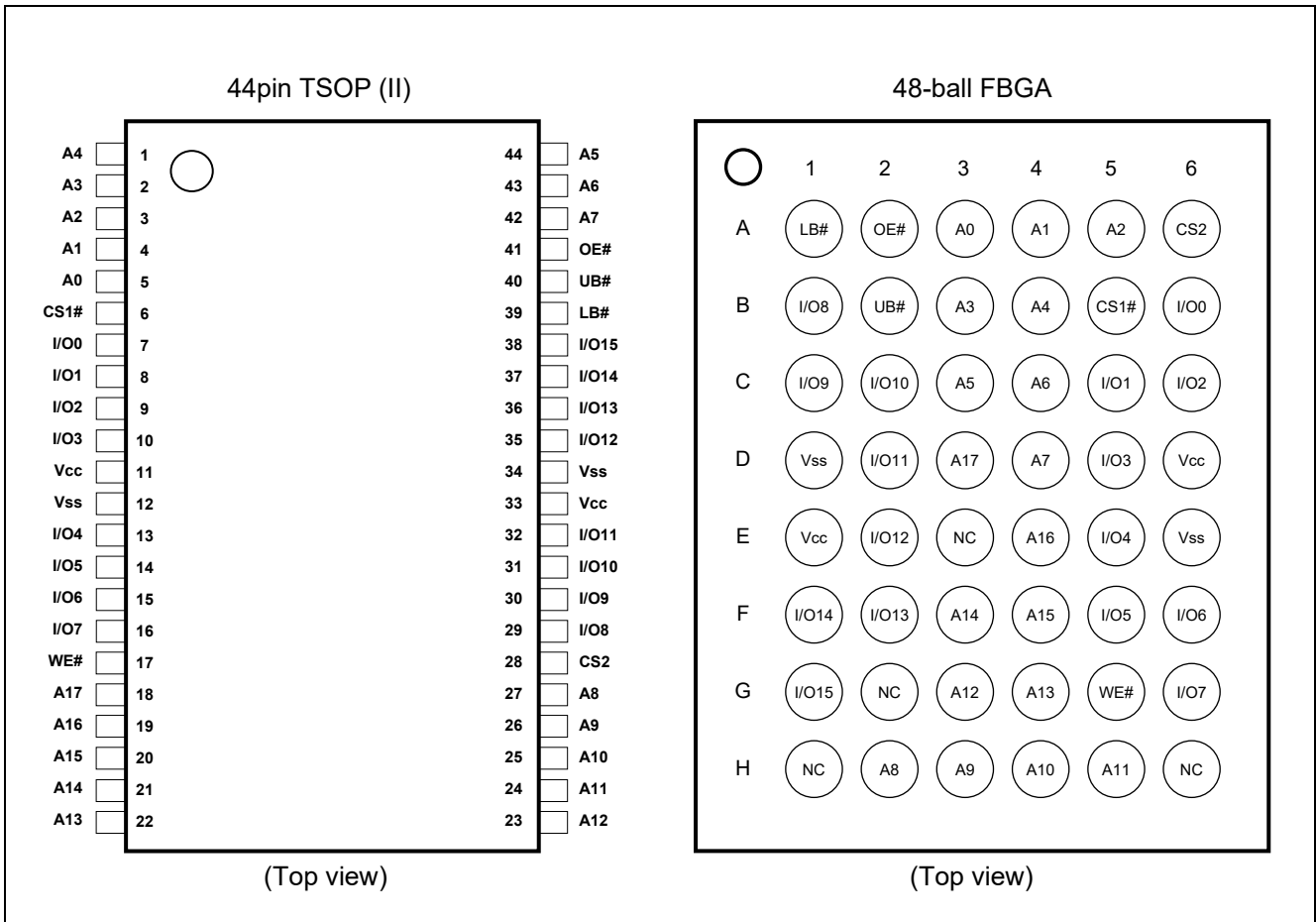
- Single 3V supply: 2.7V to 3.6V
- Access time: 45ns (max.)
- Current consumption:
  - Standby: 0.3μA (typ.)
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Battery backup operation

## Orderable part number information

Orderable part number	Access time	Temperature range	Package	Shipping container
RMLV0416EGSB-4S2#AA*	45 ns	-40 ~ +85°C	400-mil 44pin plastic TSOP (II)	Tray
RMLV0416EGSB-4S2#HA*				Embossed tape
RMLV0416EGBG-4S2#AC*			48-ball FBGA with 0.75mm ball pitch	Tray
RMLV0416EGBG-4S2#KC*				Embossed tape

Note 1. \* = Revision code for Assembly site change, etc. (\* = 0, 1, etc.)

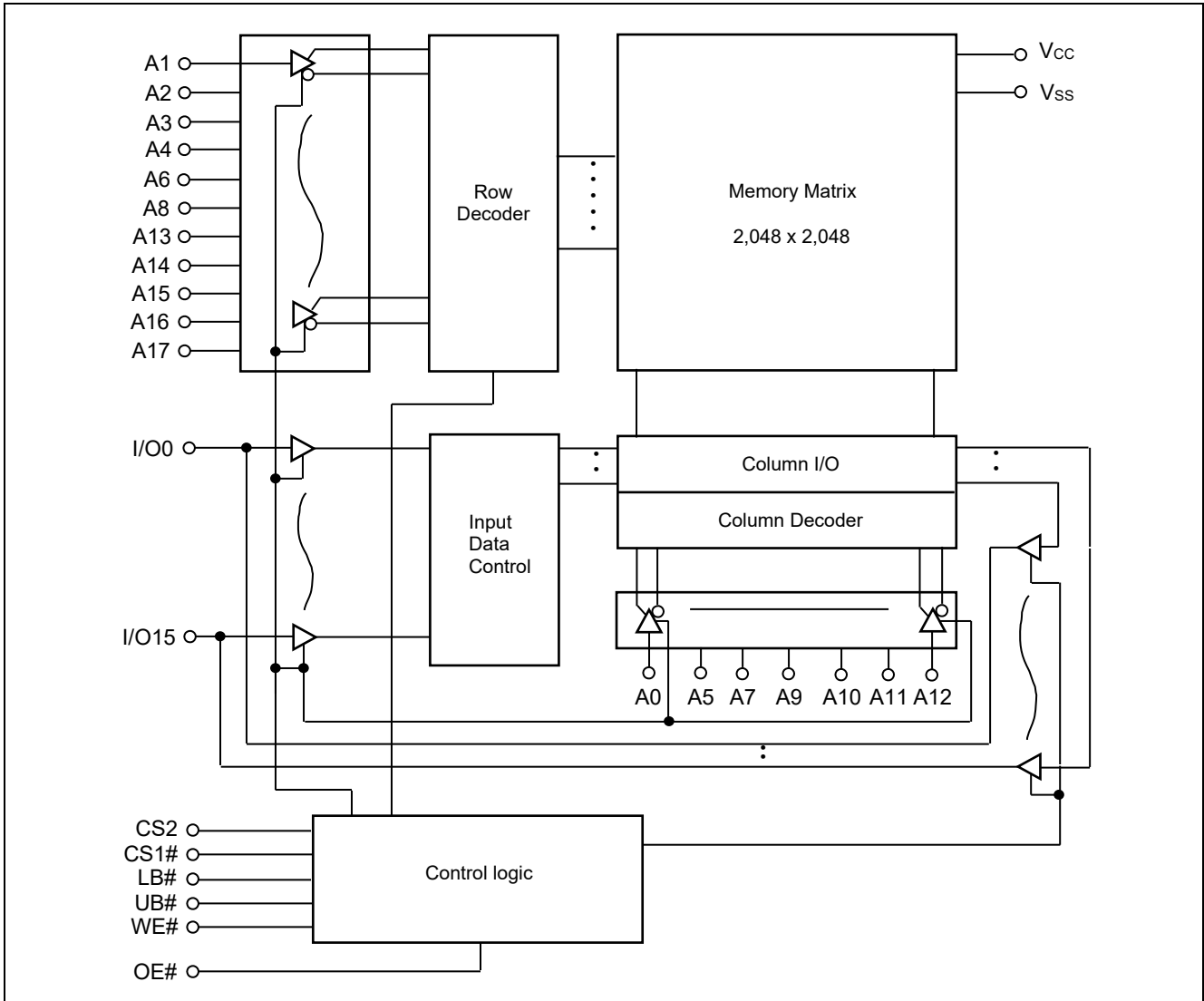
## Pin Arrangement



## Pin Description

Pin name	Function
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
NC	No connection

### Block Diagram



### Operation Table

CS1#	CS2	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	X	X	X	X	X	High-Z	High-Z	Standby
X	L	X	X	X	X	High-Z	High-Z	Standby
X	X	X	X	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	X	L	L	Din	Din	Write
L	H	L	X	H	L	Din	High-Z	Lower byte write
L	H	L	X	L	H	High-Z	Din	Upper byte write
L	H	H	H	X	X	High-Z	High-Z	Output disable

Note 2. H: V<sub>IH</sub> L: V<sub>IL</sub> X: V<sub>IH</sub> or V<sub>IL</sub>

## Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to +4.6	V
Terminal voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	-0.5 <sup>3</sup> to V <sub>CC</sub> +0.3 <sup>4</sup>	V
Power dissipation	P <sub>T</sub>	0.7	W
Operation temperature	T <sub>opr</sub>	-40 to +85	°C
Storage temperature range	T <sub>stg</sub>	-65 to +150	°C
Storage temperature range under bias	T <sub>bias</sub>	-40 to +85	°C

Note 3. -3.0V for pulse ≤ 30ns (full width at half maximum)

4. Maximum voltage is +4.6V.

## DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V	
	V <sub>SS</sub>	0	0	0	V	
Input high voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> +0.3	V	
Input low voltage	V <sub>IL</sub>	-0.3	—	0.6	V	5
Ambient temperature range	T <sub>a</sub>	-40	—	+85	°C	

Note 5. -3.0V for pulse ≤ 30ns (full width at half maximum)

## DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	—	—	1	μA	CS1# = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub> or LB# = UB# = V <sub>IH</sub> , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Operating current	I <sub>CC</sub>	—	—	10	mA	CS1# = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	
Average operating current	I <sub>CC1</sub>	—	—	20	mA	Cycle = 55ns, duty = 100%, I <sub>I/O</sub> = 0mA, CS1# = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>	
		—	—	25	mA	Cycle = 45ns, duty = 100%, I <sub>I/O</sub> = 0mA, CS1# = V <sub>IL</sub> , CS2 = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>	
	I <sub>CC2</sub>	—	—	2.5	mA	Cycle = 1μs, duty = 100%, I <sub>I/O</sub> = 0mA, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V, V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V, V <sub>IL</sub> ≤ 0.2V	
Standby current	I <sub>SB</sub>	—	0.1 <sup>6</sup>	0.3	mA	CS2 = V <sub>IL</sub> , Others = V <sub>SS</sub> to V <sub>CC</sub>	
Standby current	I <sub>SB1</sub>	—	0.3 <sup>6</sup>	2	μA	~+25°C	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub> , (1) CS2 ≤ 0.2V or (2) CS1# ≥ V <sub>CC</sub> -0.2V, CS2 ≥ V <sub>CC</sub> -0.2V or (3) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V
		—	—	3	μA	~+40°C	
		—	—	5	μA	~+70°C	
		—	—	7	μA	~+85°C	
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1mA	
	V <sub>OH2</sub>	V <sub>CC</sub> -0.2	—	—	V	I <sub>OH</sub> = -0.1mA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2mA	
	V <sub>OL2</sub>	—	—	0.2	V	I <sub>OL</sub> = 0.1mA	

Note 6. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>=25°C), and not 100% tested.

## Capacitance

(V<sub>CC</sub> = 2.7V ~ 3.6V, f = 1MHz, T<sub>a</sub> = -40 ~ +85°C)

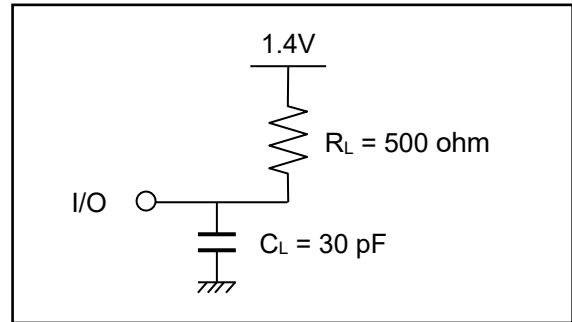
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C <sub>in</sub>	—	—	8	pF	V <sub>in</sub> = 0V	7
Input / output capacitance	C <sub>I/O</sub>	—	—	10	pF	V <sub>I/O</sub> = 0V	7

Note 7. This parameter is sampled and not 100% tested.

## AC Characteristics

Test Conditions ( $V_{CC} = 2.7V \sim 3.6V$ ,  $T_a = -40 \sim +85^{\circ}C$ )

- Input pulse levels:  $V_{IL} = 0.4V$ ,  $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



## Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	$t_{RC}$	45		ns	
Address access time	$t_{AA}$	—	45	ns	
Chip select access time	$t_{ACS1}$	—	45	ns	
	$t_{ACS2}$	—	45	ns	
Output enable to output valid	$t_{OE}$	—	22	ns	
Output hold from address change	$t_{OH}$	10	—	ns	
LB#, UB# access time	$t_{BA}$	—	45	ns	
Chip select to output in low-Z	$t_{CLZ1}$	10	—	ns	8,9
	$t_{CLZ2}$	10	—	ns	8,9
LB#, UB# enable to low-Z	$t_{BLZ}$	5	—	ns	8,9
Output enable to output in low-Z	$t_{OLZ}$	5	—	ns	8,9
Chip deselect to output in high-Z	$t_{CHZ1}$	0	18	ns	8,9,10
	$t_{CHZ2}$	0	18	ns	8,9,10
LB#, UB# disable to high-Z	$t_{BHZ}$	0	18	ns	8,9,10
Output disable to output in high-Z	$t_{OHZ}$	0	18	ns	8,9,10

Note 8. This parameter is sampled and not 100% tested.

9. At any given temperature and voltage condition,  $t_{CHZ1}$  max is less than  $t_{CLZ1}$  min,  $t_{CHZ2}$  max is less than  $t_{CLZ2}$  min,  $t_{BHZ}$  max is less than  $t_{BLZ}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.

10.  $t_{CHZ1}$ ,  $t_{CHZ2}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

## Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	$t_{WC}$	45	—	ns	
Address valid to write end	$t_{AW}$	35	—	ns	
Chip select to write end	$t_{CW}$	35	—	ns	
Write pulse width	$t_{WP}$	35	—	ns	11
LB#,UB# valid to write end	$t_{BW}$	35	—	ns	
Address setup time to write start	$t_{AS}$	0	—	ns	
Write recovery time from write end	$t_{WR}$	0	—	ns	
Data to write time overlap	$t_{DW}$	25	—	ns	
Data hold from write end	$t_{DH}$	0	—	ns	
Output enable from write end	$t_{OW}$	5	—	ns	12
Output disable to output in high-Z	$t_{OHZ}$	0	18	ns	12,13
Write to output in high-Z	$t_{WHZ}$	0	18	ns	12,13

Note 11.  $t_{WP}$  is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

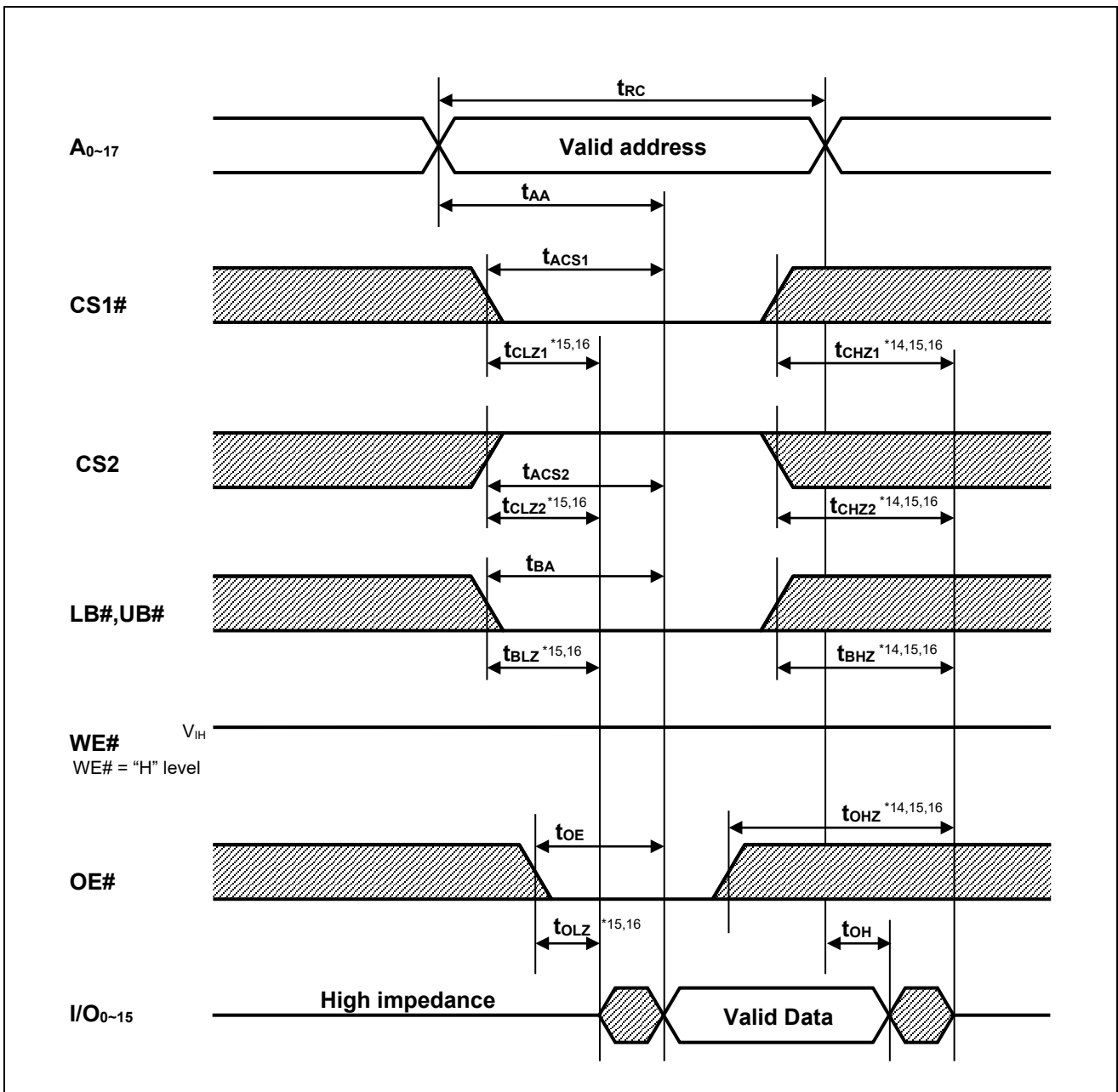
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

12. This parameter is sampled and not 100% tested.

13.  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

## Timing Waveforms

### Read Cycle

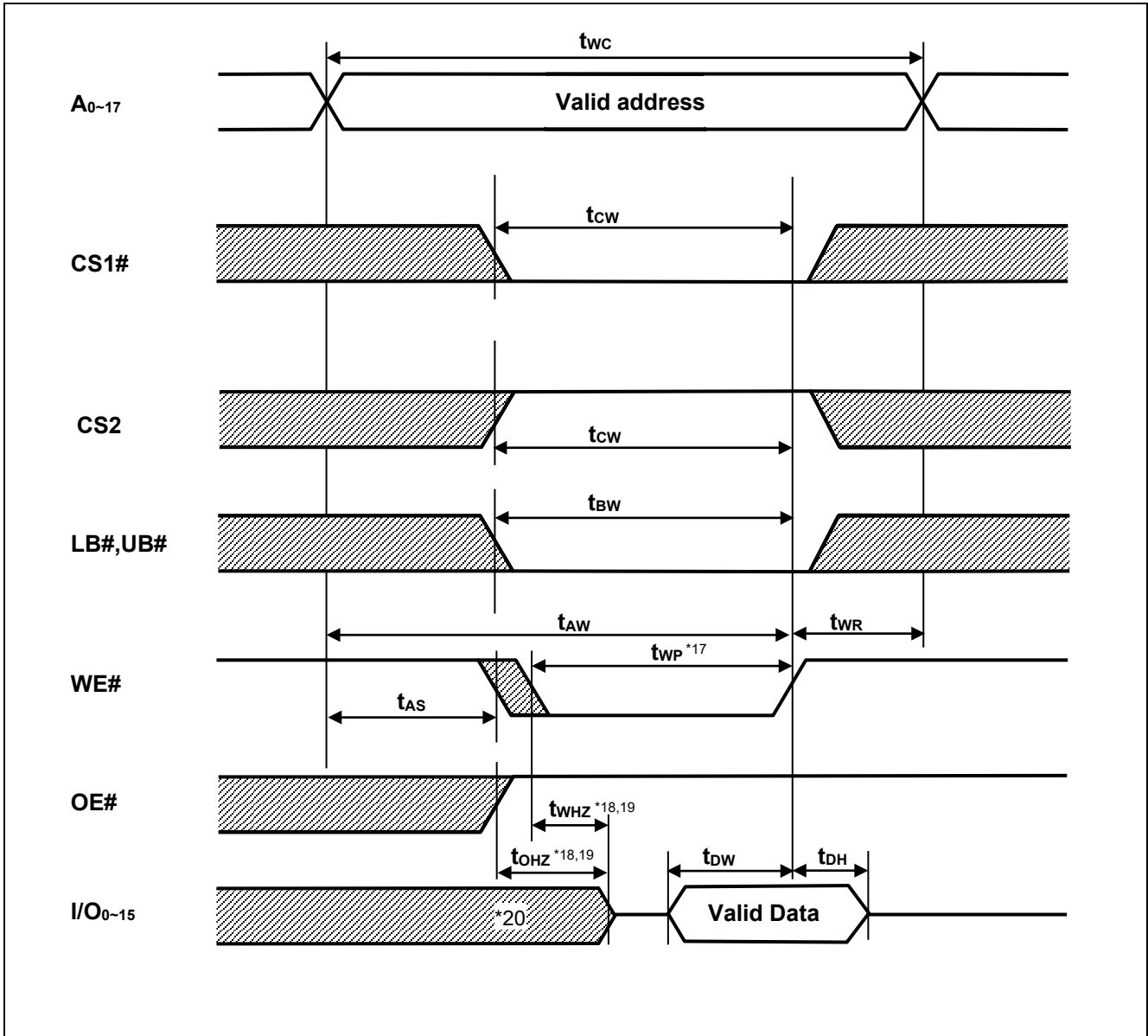


Note 14.  $t_{CHZ1}$ ,  $t_{CHZ2}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

15. This parameter is sampled and not 100% tested

16. At any given temperature and voltage condition,  $t_{CHZ1}$  max is less than  $t_{CLZ1}$  min,  $t_{CHZ2}$  max is less than  $t_{CLZ2}$  min,  $t_{BHZ}$  max is less than  $t_{BLZ}$  min, and  $t_{OHZ}$  max is less than  $t_{OLZ}$  min, for any device.

Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



Note 17.  $t_{wp}$  is the minimum time to perform a write.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

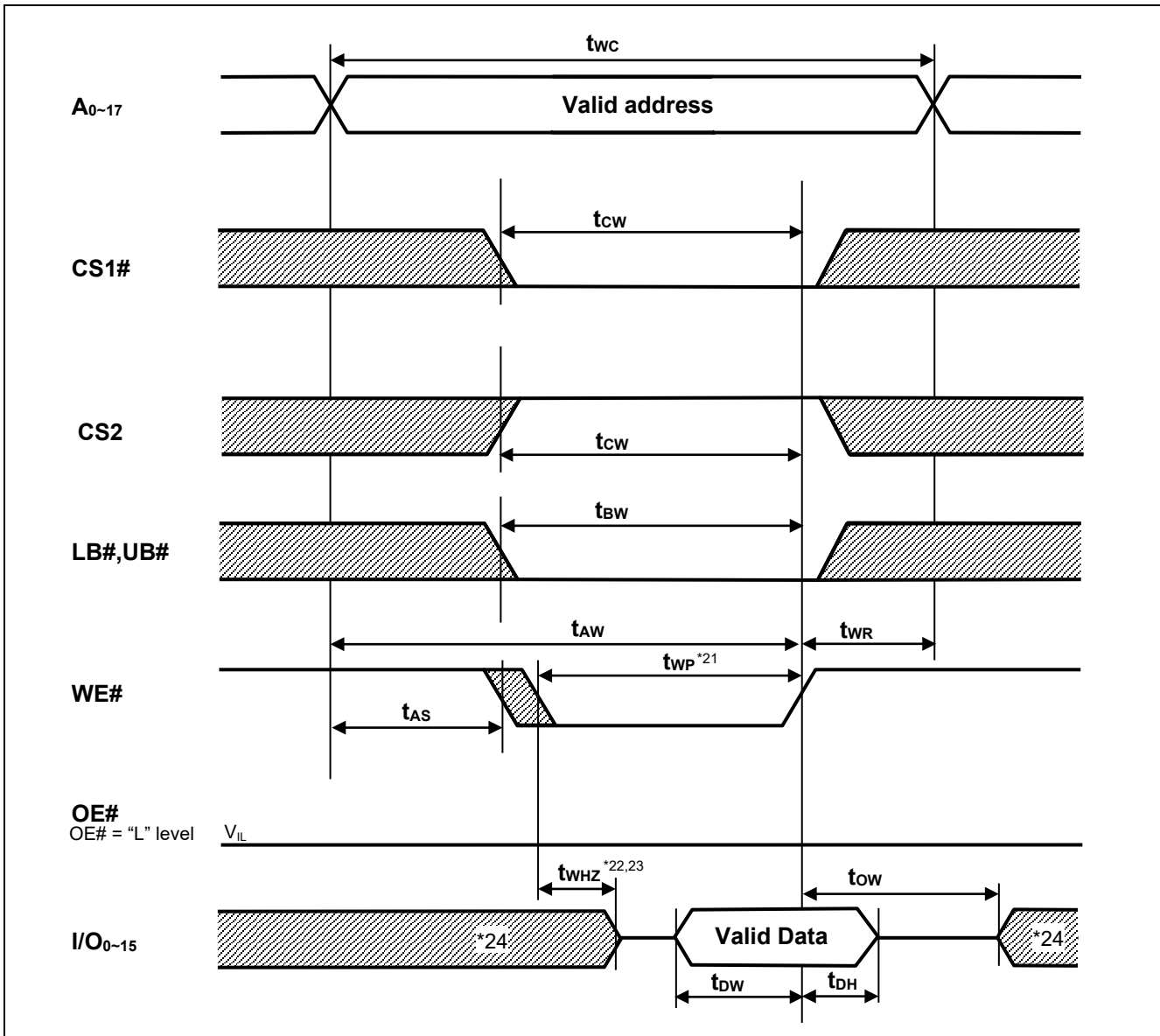
18.  $t_{ohz}$  and  $t_{whz}$  are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

19. This parameter is sampled and not 100% tested

20. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.



Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



Note 21.  $t_{wp}$  is the minimum time to perform a write.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

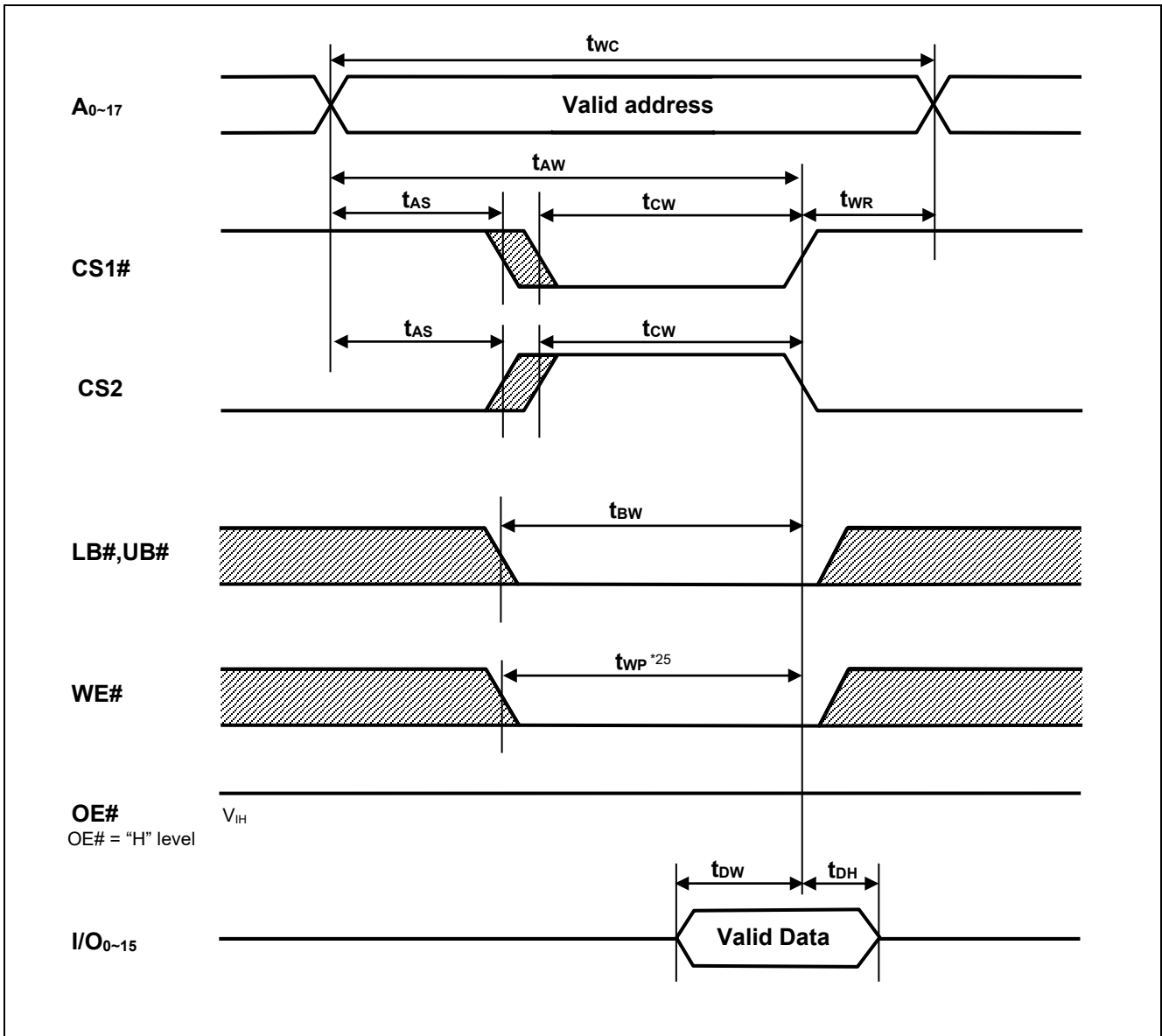
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

22.  $t_{whz}$  is defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

23. This parameter is sampled and not 100% tested.

24. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.

Write Cycle (3) (CS1#, CS2 CLOCK)



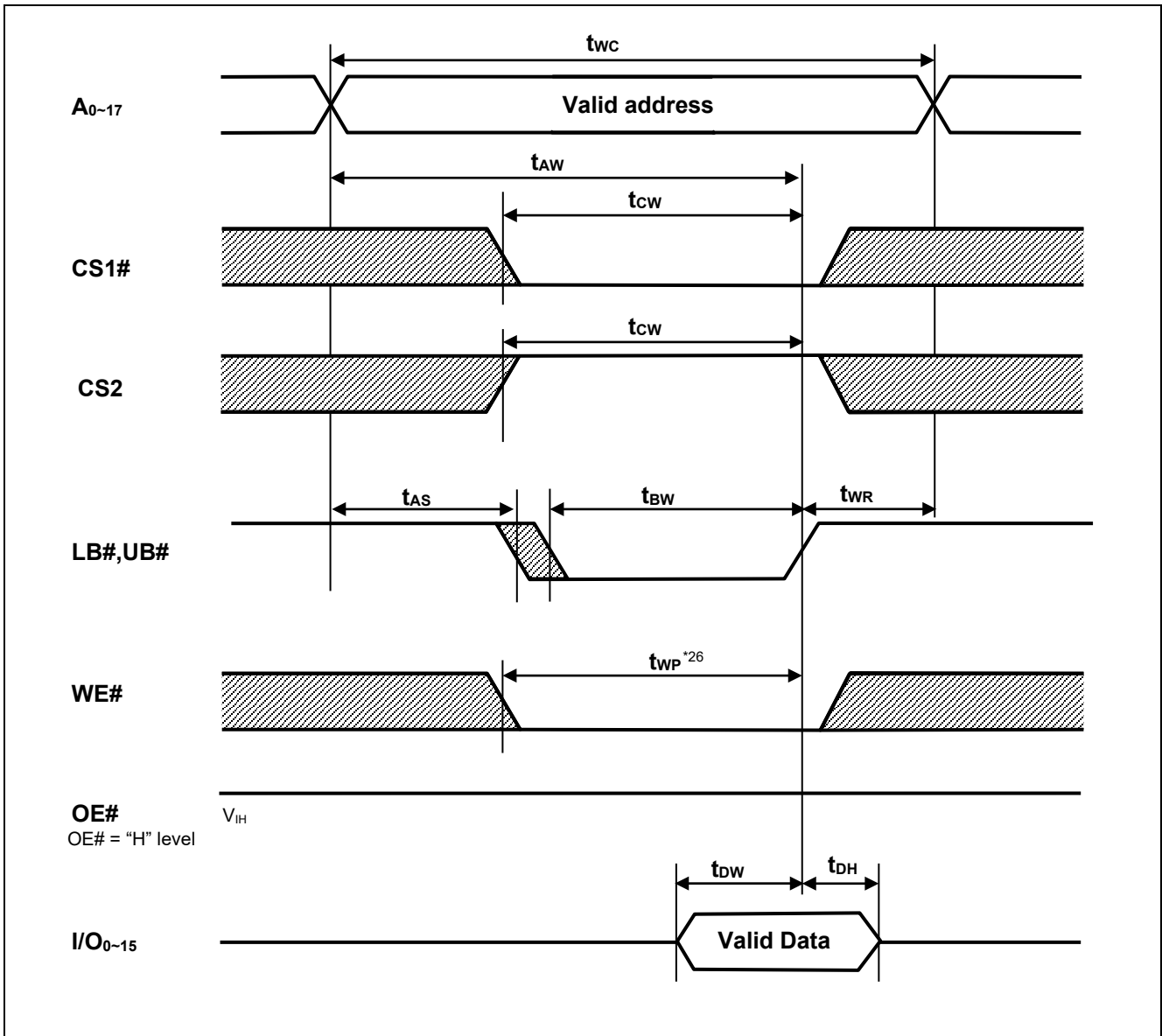
Note 25.  $t_{WP}$  is the minimum time to perform a write.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4) (LB#, UB# CLOCK)



Note 26.  $t_{WP}$  is the minimum time to perform a write.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

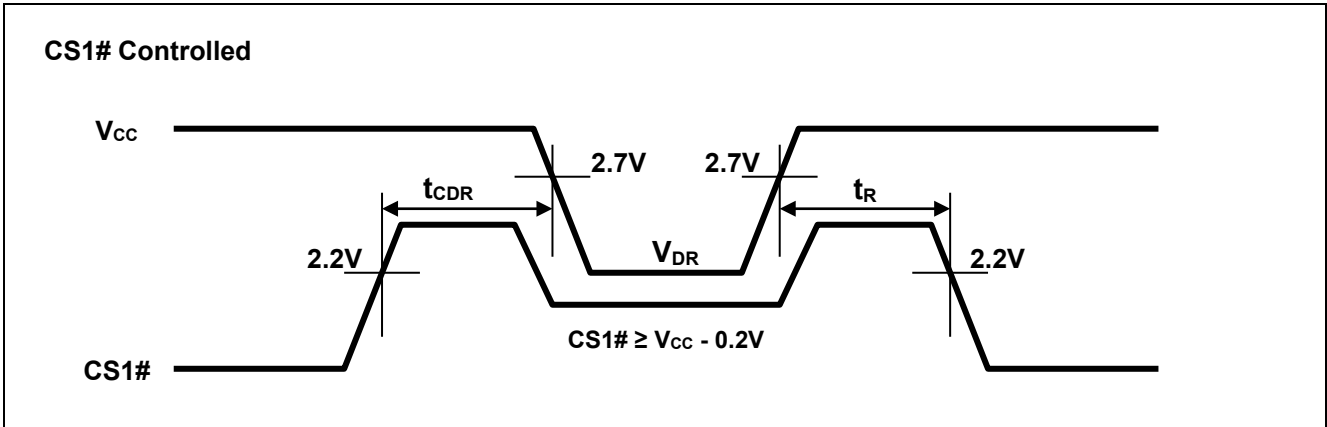
Low  $V_{CC}$  Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions <sup>*28</sup>	
$V_{CC}$ for data retention	$V_{DR}$	1.5	—	—	V	$V_{in} \geq 0V$ , (1) $CS2 \leq 0.2V$ or (2) $CS1\# \geq V_{CC}-0.2V$ , $CS2 \geq V_{CC}-0.2V$ or (3) $LB\# = UB\# \geq V_{CC}-0.2V$ , $CS1\# \leq 0.2V$ , $CS2 \geq V_{CC}-0.2V$	
Data retention current	$I_{CCDR}$	—	0.3 <sup>*27</sup>	2	$\mu A$	$\sim +25^{\circ}C$	$V_{CC} = 3.0V$ , $V_{in} \geq 0V$ , (1) $CS2 \leq 0.2V$ or (2) $CS1\# \geq V_{CC}-0.2V$ , $CS2 \geq V_{CC}-0.2V$ or (3) $LB\# = UB\# \geq V_{CC}-0.2V$ , $CS1\# \leq 0.2V$ , $CS2 \geq V_{CC}-0.2V$
		—	—	3	$\mu A$	$\sim +40^{\circ}C$	
		—	—	5	$\mu A$	$\sim +70^{\circ}C$	
		—	—	7	$\mu A$	$\sim +85^{\circ}C$	
Chip deselect time to data retention	$t_{CDR}$	0	—	—	ns	See retention waveform.	
Operation recovery time	$t_R$	5	—	—	ms		

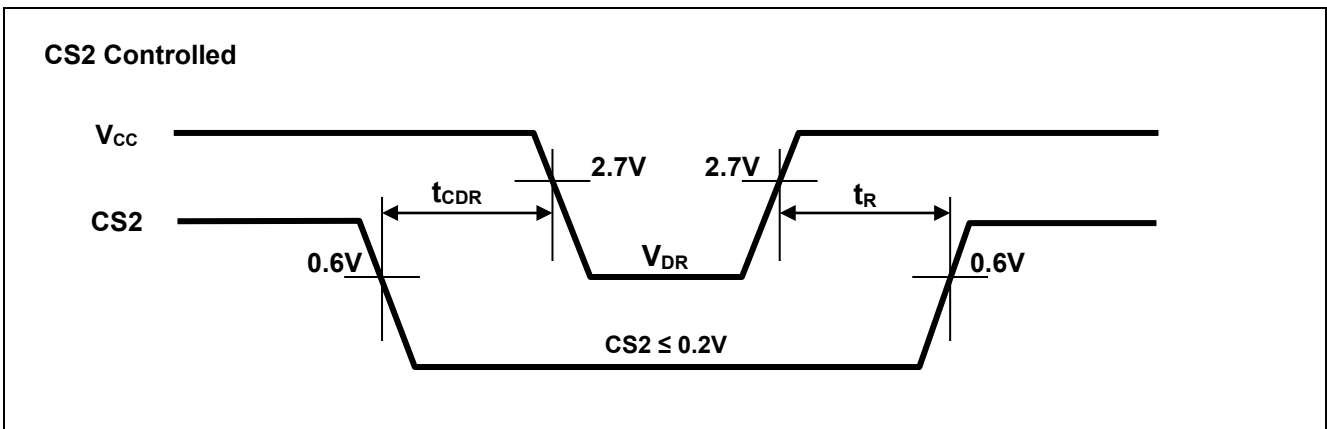
Note 27. Typical parameter indicates the value for the center of distribution at 3.0V ( $T_a=25^{\circ}C$ ), and not 100% tested.

28. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and I/O buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address, WE#, CS1#, OE#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be  $CS2 \geq V_{CC}-0.2V$  or  $CS2 \leq 0.2V$ . The other inputs levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high-impedance state.

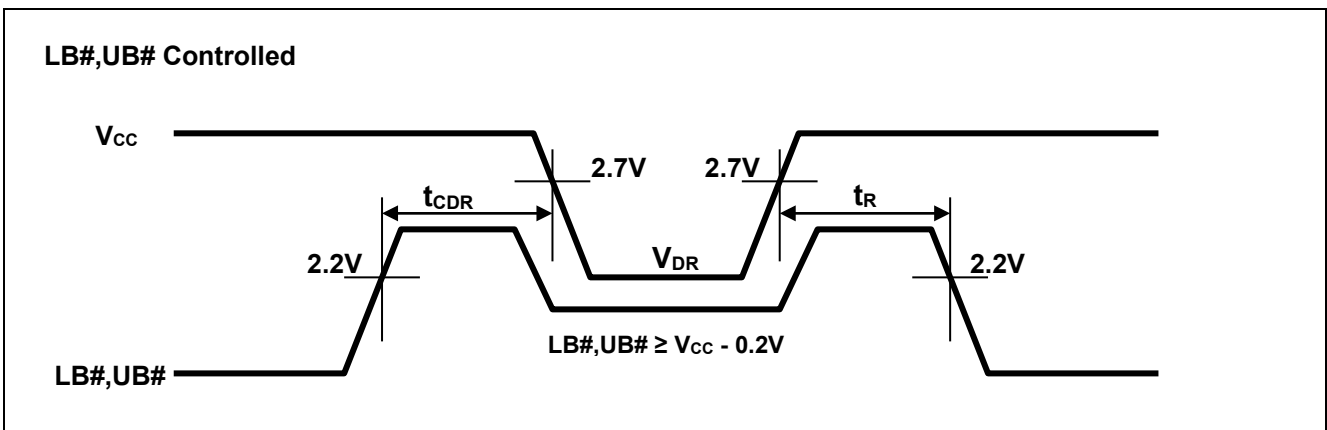
Low Vcc Data Retention Timing Waveforms (CS1# controlled)



Low Vcc Data Retention Timing Waveforms (CS2 controlled)



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled)



Revision History	RMLV0416E Series Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2014.2.27	—	First edition issued
2.00	2016.1.12	1	Changed section from “Part Name Information” to “Orderable part number information”
2.01	2020.2.20	Last page	Updated the Notice to the latest version
3.00	2021.8.18	1,4,12	Changed the typical value of I <sub>SB1</sub> and I <sub>CCDR</sub> from 0.4μA to 0.3μA. Revised orderable part number information

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