MPQ2167B

6V, 4A, Configurable Frequency, Synchronous Buck Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ2167B is a synchronous step-down converter that achieves up to 4A of continuous output current with peak current control for excellent transient response and efficiency performance. The device operates from a 2.7V to 6.0V input range, generates an output voltage as low as 0.606V, and has a configurable frequency (300kHz to 2.2MHz). It is ideal for a wide range of applications, including automotive infotainment, clusters, telematics, and portable instruments.

The device integrates a 35mΩ high-side MOSFET and a 25mΩ synchronous rectifier for high efficiency without an external Schottky diode. It can be configured for either advanced asynchronous mode (AAM) or forced continuous conduction mode (FCCM) at light-load. AAM provides high efficiency by reducing switching losses, while FCCM has a controllable frequency and lower output ripple.

The MPQ2167B offers standard features including soft start, external sync clock, enable control, and a power good indicator. In addition, the device provides over-current protection with valley current detection to avoid current runaway. Additional safety features include short-circuit protection, reliable over-voltage protection, and auto-recovery thermal protection.

With internal compensation, the MPQ2167B requires a minimal number of readily available, standard external components, and is available in a QFN-11 (2mmx3mm) package.

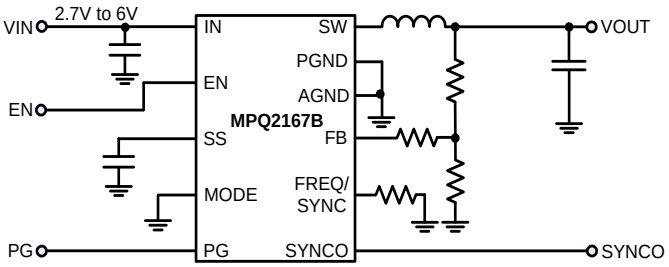
FEATURES

- 2.7V to 6.0V Operating Input Range
- Adjustable Output from 0.606V
- Up to 4A Continuous Output Current
- High-Efficiency Synchronous Mode Control
- 35mΩ and 25mΩ Internal Power MOSFET
- Configurable Frequency Up to 2.2MHz
- External Sync Clock Up to 2.2MHz
- 42μA Quiescent Current
- Low Shutdown Mode Current
- 100% Duty Cycle Operation
- Internal Compensation Mode
- Selectable AAM or FCCM Operation
- External Soft Start
- Remote EN Control
- Power Good Indicator
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection
- V_{IN} Under-Voltage Lockout
- V_{OUT} Over-Voltage Protection
- Thermal Shutdown
- Available in a QFN-11 (2mmx3mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade-1

APPLICATIONS

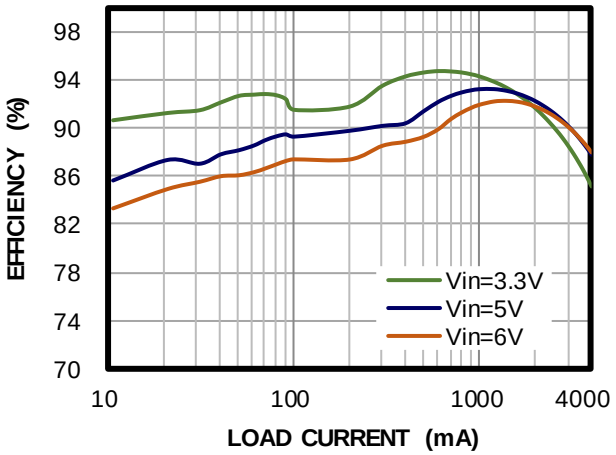
- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Industrial Supplies
- Battery-Powered Devices

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 1.8V, AAM, L = 1µH, f_{SW} = 2.1MHz



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2167BGDE-AEC1***	QFN-11 (2mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MPQ2167BGDE-AEC1–Z).

** Moisture Sensitivity Level Rating

*** Wettable Flank

TOP MARKING

BJM

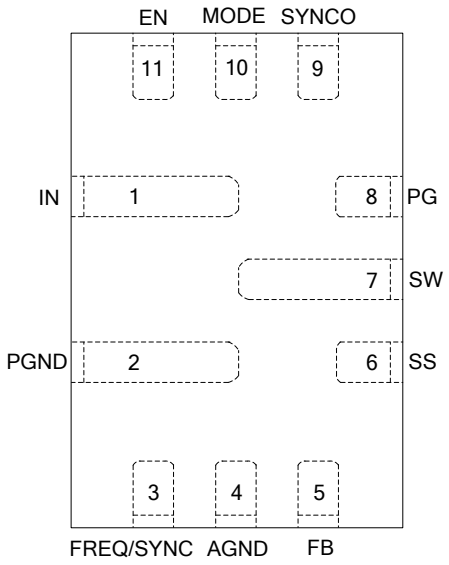
YWW

LLL

BJM: Product code of MPQ2167BGDE-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-11 (2mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Input supply.** IN supplies all power to the converter. Place a decoupling capacitor to ground as close as possible to the IC to reduce switching spikes.
2	PGND	**Power ground.** Connect large copper areas to the negative terminals of the input and output capacitors.
3	FREQ/SYNC	**Switching frequency setting and synchronization input.** Connect a resistor to GND to set the switching frequency. The switching frequency can be synchronized by an external clock via this pin.
4	AGND	**Analog ground.** Ground for internal logic and signal circuit.
5	FB	**Feedback point.** Negative input of the error amplifier. Connect to the tap of an external resistor divider between the output and GND to set the regulation voltage. Power good and under-voltage lockout circuits use FB to monitor the output voltage.
6	SS	**Soft start.** Place a capacitor from SS to GND to set the soft-start time externally. Float this pin to activate the internal, default 1ms soft-start setting.
7	SW	**Switch output.** Internally connect this pin to the high-side and low-side power switches. Externally connect it to the output inductor.
8	PG	**Power good indicator.** The PG output is an open drain that connects to VIN by an internal pull-up resistor. PG is pulled up to VIN when the FB voltage (V_{FB}) is within 15% of the regulation level. If V_{FB} is out of that regulation range, PG is pulled low.
9	SYNCO	**Synchronization output.** Output a 180° out of phase clock to the other devices.
10	MODE	**Mode selection.** Connect this pin to logic high or the input voltage (V_{IN}) for FCCM. Connect this pin to logic low or ground for AAM. Do not leave MODE floating.
11	EN	**Enable input.** Drive EN high to turn on the device. Float or ground EN to disable the device.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} 6.5V
V_{SW} ..... -0.3V (-3V for <10ns) to 6.5V (7.0V for <10ns)
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) 1.78W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Continuous supply voltage (V_{IN}) ..... 2.7V to 6.0V
Output voltage (V_{OUT}) ..... 0.606V to V_{IN}
Load current range ..... 0A to 4A
Operating junction temp (T_J) -40°C to +125°C (3)

Thermal Resistance θ_{JA} θ_{JC}

QFN-11 (2mmx3mm)		
JESD51-7 (4)	70	15 °C/W
EV2167B-D-00A (5)	42	13.5 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the module will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Operating junction temperatures above 125°C may be supported; contact MPS for details.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on MPS standard EVB, 6.35cmx6.35cm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, unless otherwise noted, typical values are at T_J = 25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply and Under-Voltage Lockout (UVLO)						
Supply current (quiescent)	I_Q	Mode = AAM, V_{EN} = 2V, no load, R_{FREQ} = 1MΩ, T_J = 25°C		42	50	μA
		T_J = -40°C to +125°C			120	
Shutdown current	I_{SD}	Mode = AAM, V_{EN} = 0V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			20	
V_{IN} UVLO rising threshold	$INUV_{Vth-R}$		2.3	2.5	2.7	V
V_{IN} UVLO falling threshold	$INUV_{Vth-F}$		2	2.15	2.3	V
V_{IN} UVLO threshold hysteresis	$INUV_{HYS}$			350		mV
Output and Regulation						
Regulated FB voltage	V_{FB}	T_J = 25°C	0.596	0.606	0.616	V
		T_J = -40°C to +125°C	0.591		0.621	V
FB input current	I_{FB}	V_{FB} = 0.63V		10	100	nA
Output discharge resistor	$R_{DISCHARGE}$		50	100	150	Ω
Switches and Frequency						
High-side switch on resistance	$R_{DS(ON-P)}$	V_{IN} = 5V, I_{OUT} = 200mA		35	70	mΩ
Low-side switch on resistance	$R_{DS(ON-N)}$	V_{IN} = 5V, I_{OUT} = 200mA		25	70	mΩ
High-side SW leakage current	$I_{HSW-LKG}$	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 6V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			30	
Low-side SW leakage current	$I_{LSW-LKG}$	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			10	
Switching frequency	f_{SW}	R_{FREQ} = 499kΩ	380	450	520	kHz
		R_{FREQ} = 75kΩ	1800	2100	2400	
Sync frequency range	f_{SYNC}		0.3		2.2	MHz
Sync voltage high threshold	$V_{SYNC-HIGH}$	V_{IN} = 2.7V (6)	1.5			V
		V_{IN} = 3.6V	1.8			
		V_{IN} = 6V (6)	3.2			
Sync voltage low threshold	$V_{SYNC-LOW}$	V_{IN} = 2.7V (6)			0.8	V
		V_{IN} = 3.6V			1.1	
		V_{IN} = 6V (6)			1.6	
Maximum duty	D_{MAX}			100		%
Minimum on time (6)	t_{ON-MIN}			50		ns
Minimum off time (6)	$t_{OFF-MIN}$			95		ns
PG						
PG sink current capacity	$V_{PG-SINK}$	Sink 1mA			300	mV
PG logic high voltage	$V_{PG-HIGH}$	V_{IN} = 5V	4.5			V
PG delay time	$t_{PG-DELAY}$	V_{OUT} rising edge	40	100	180	μs
		V_{OUT} falling edge	5	20	30	μs
PG upper rising threshold	PG_{UP_R}	A percentage of V_{FB}	108	115	122	%
PG upper hysteresis	PG_{UP_HYS}	A percentage of V_{FB}		5		%
PG lower rising threshold	PG_{LOW_R}	A percentage of V_{FB}	80	85	90	%
PG lower hysteresis	PG_{LOW_HYS}	A percentage of V_{FB}		5		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, unless otherwise noted, typical values are at T_J = 25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
EN						
EN input rising threshold	$V_{EN-RISING}$		1.2			V
EN input falling threshold	$V_{EN-FALLING}$				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		2	5	µA
		V_{EN} = 0V		0	0.5	µA
MODE and Soft Start						
MODE pin rising threshold	$V_{MODE-FCCM}$	Into FCCM	1.2			V
MODE pin falling threshold	$V_{MODE-AAM}$	Into AAM			0.4	V
MODE input leakage current	I_{MODE}	Pulled up to 6V			1	µA
Soft-start charging current	I_{SS}	V_{SS} = 0V	2	4	6	µA
Default soft-start time	$t_{SS-DEFAULT}$			1		ms
Protections						
Peak current limit	$I_{PEAK-LIMIT}$	Sourcing, D = 40%	4.8	6.7	8.6	A
Valley current limit	$I_{VALLEY-LIMIT}$			4.7		A
Over-current protection timer (6)	t_{OCP}			100		µs
Zero cross threshold	I_{ZCD}			100		mA
Output over-voltage limit	OV_{Limit}	A Percentage of V_{FB}		115		%
Thermal shutdown (6)	T_{SD}	Temperature Rising		170		°C
Thermal shutdown hysteresis (6)	T_{SD-SYS}			25		°C

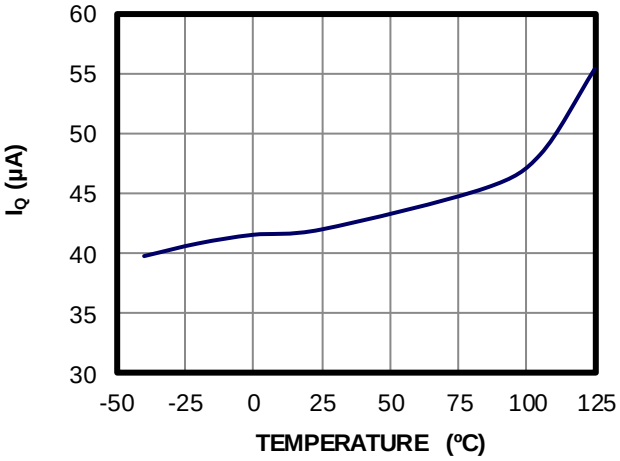
Note:

6) Not tested in production. Guaranteed by design and characterization.

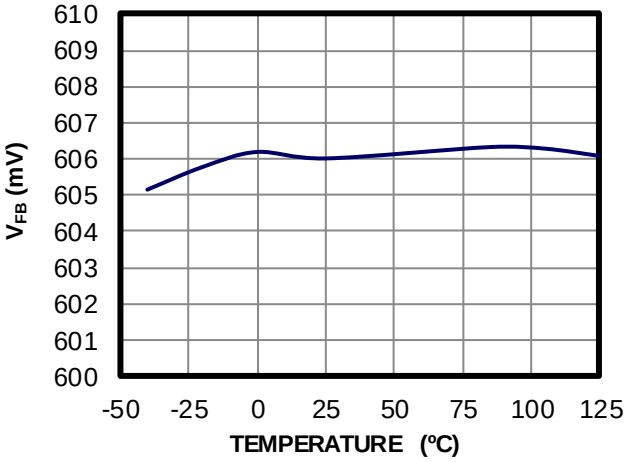
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

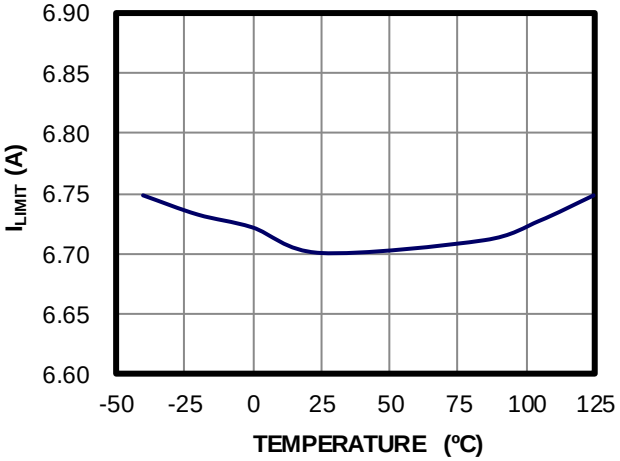
Quiescent Current vs. Temperature



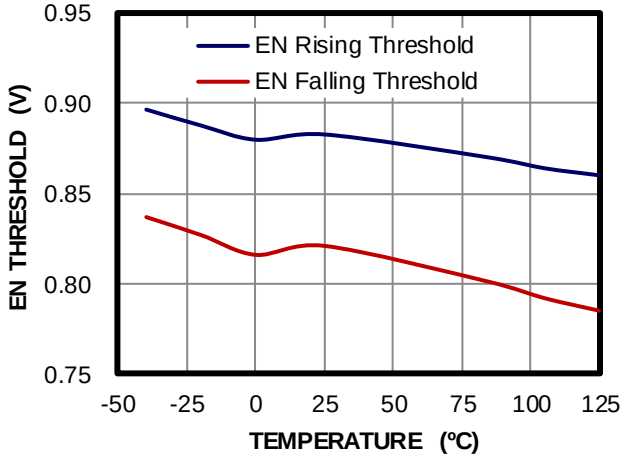
Feedback Voltage vs. Temperature



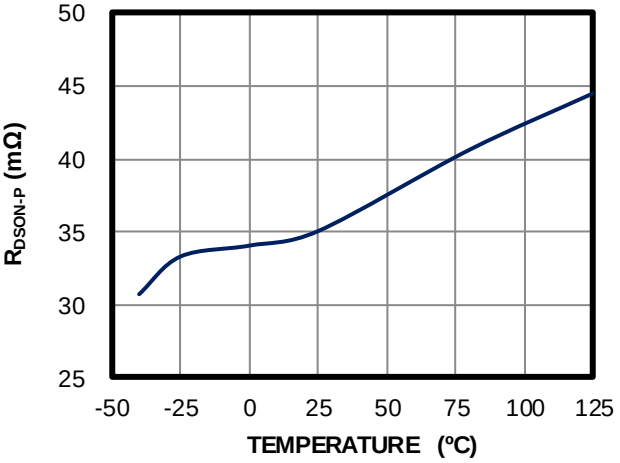
Current Limit vs. Temperature



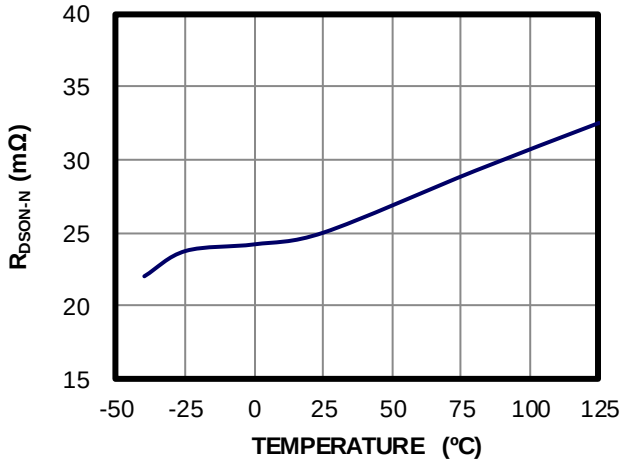
EN Threshold vs. Temperature



High-Side Switch On Resistance vs. Temperature



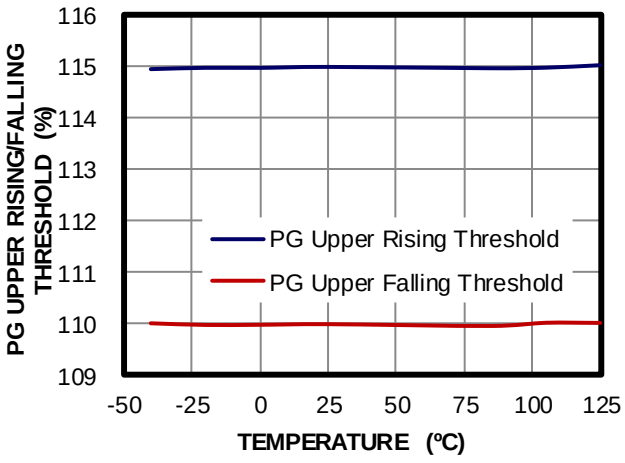
Low-Side Switch On Resistance vs. Temperature



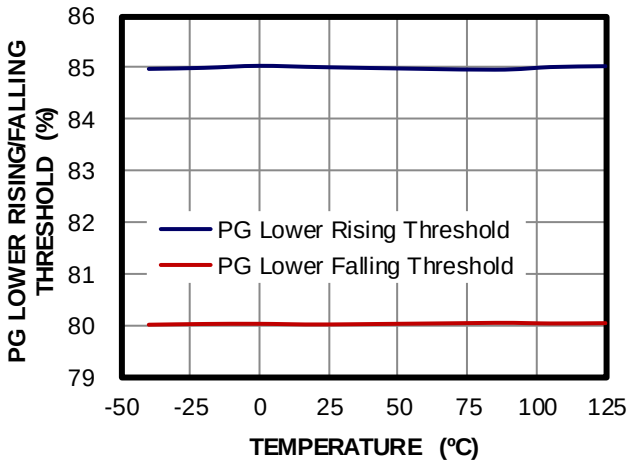
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

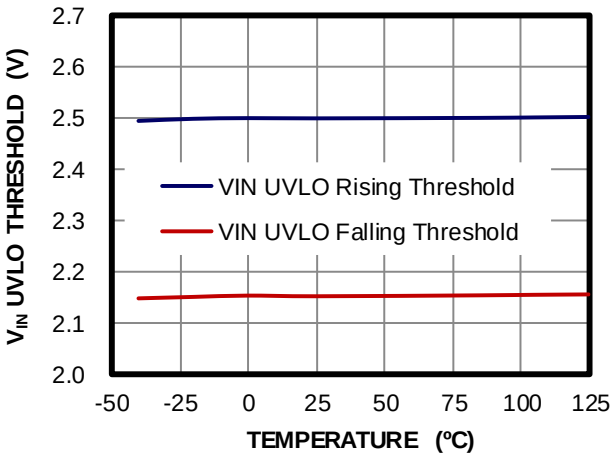
PG Upper Rising/Falling Threshold vs. Temperature



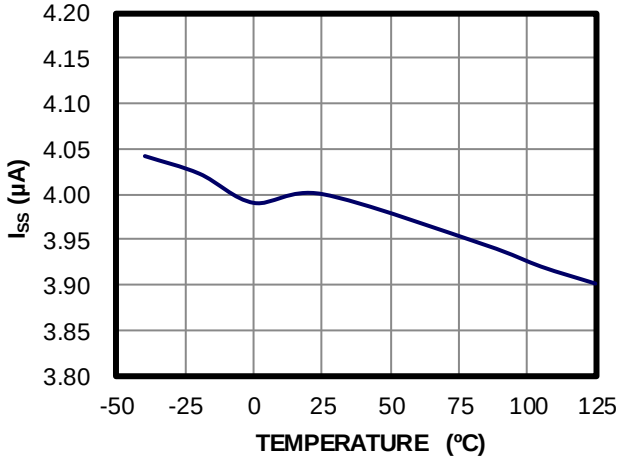
PG Lower Rising/Falling Threshold vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



Soft-Start Current vs. Temperature

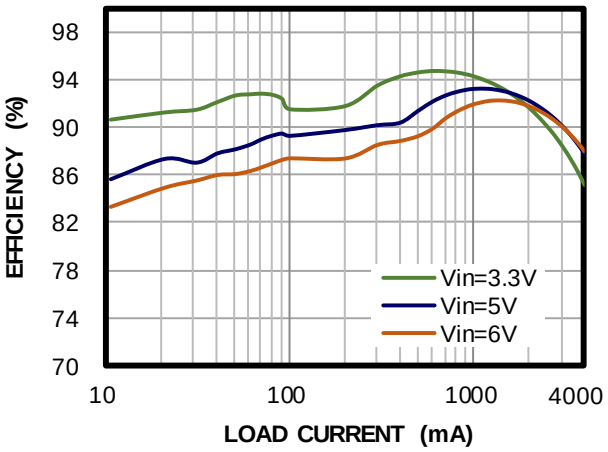


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

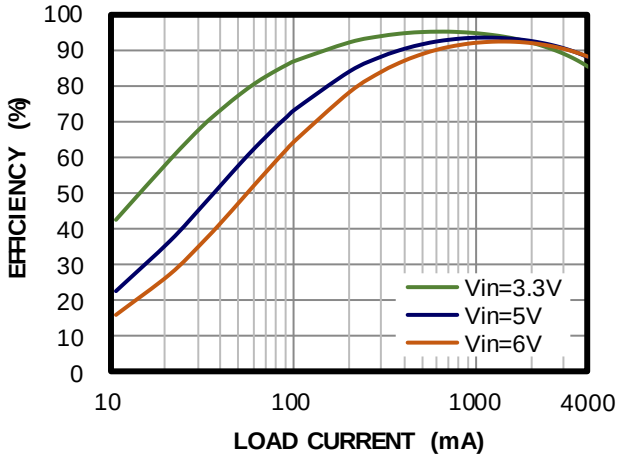
Efficiency vs. Load Current

V_{OUT} = 1.8V, AAM



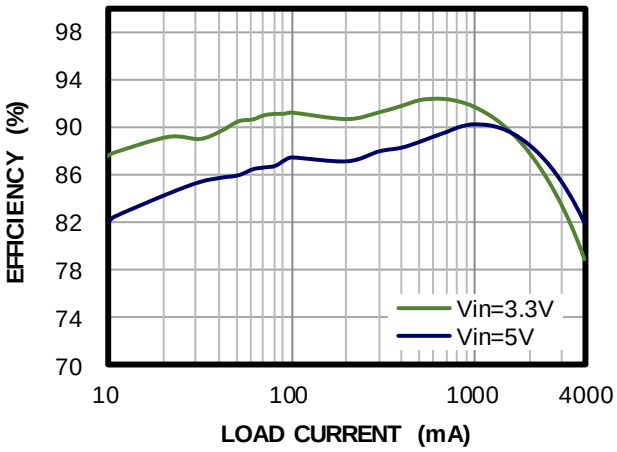
Efficiency vs. Load Current

V_{OUT} = 1.8V, CCM



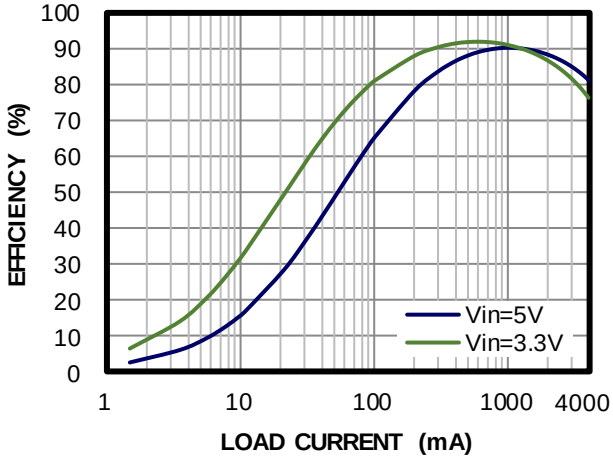
Efficiency vs. Load Current

V_{OUT} = 1.2V, AAM



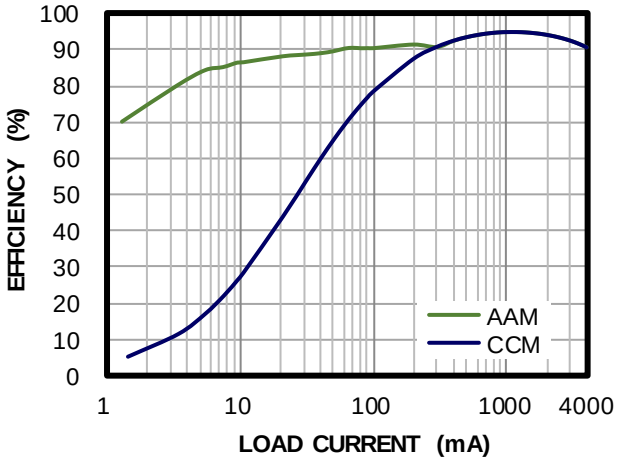
Efficiency vs. Load Current

V_{OUT} = 1.2V, CCM



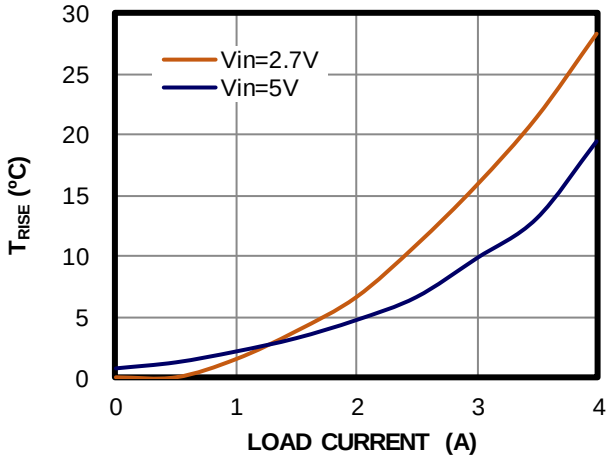
Efficiency vs. Load Current

V_{IN} = 5V, V_{OUT} = 2.5V



Case Thermal Rise

V_{OUT} = 1.8V, AAM

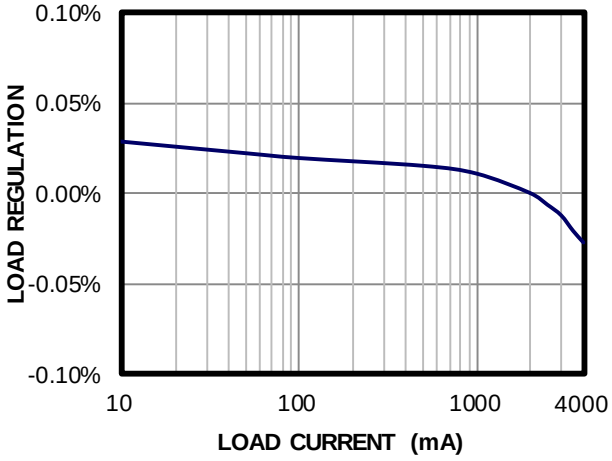


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

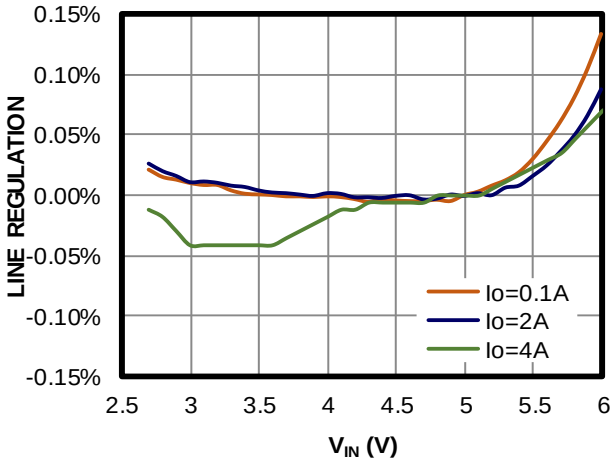
Load Regulation

V_{OUT} = 1.8V, AAM

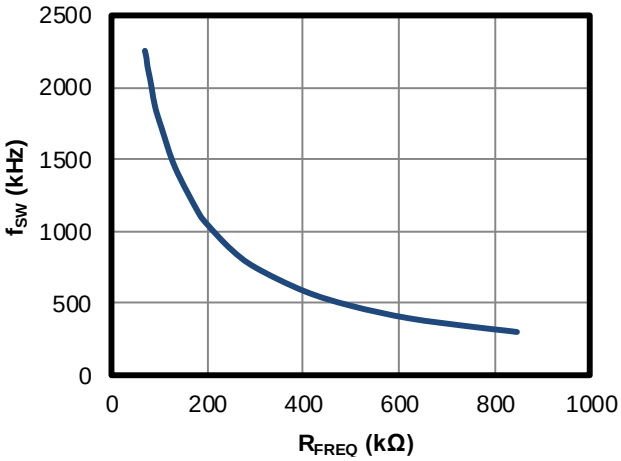


Line Regulation

V_{OUT} = 1.8V, AAM



Switching Frequency vs. Frequency Resistor

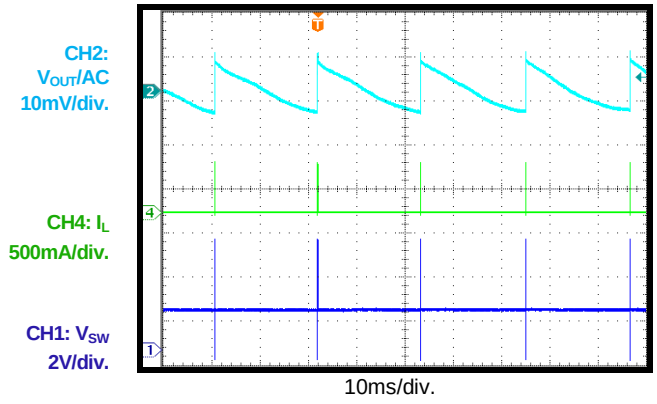


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

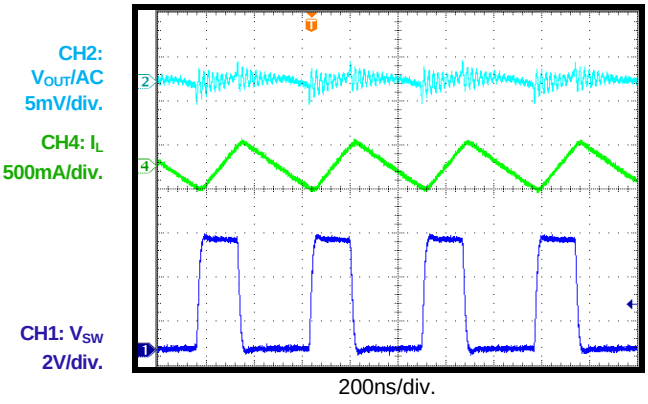
Steady State

I_{OUT} = 0A, AAM



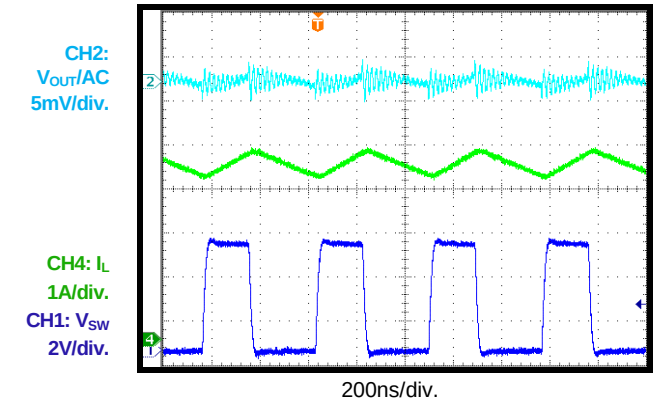
Steady State

I_{OUT} = 0A, CCM



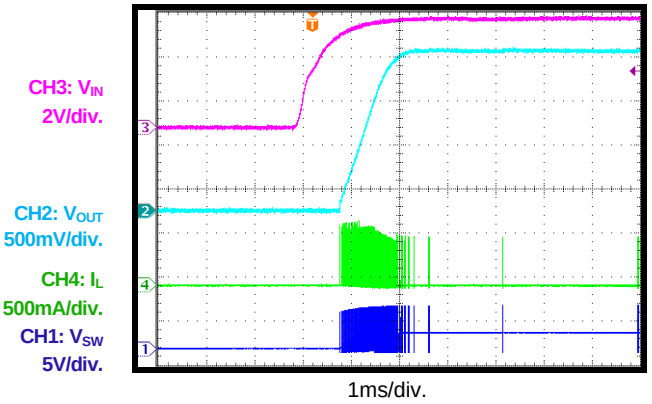
Steady State

I_{OUT} = 4A



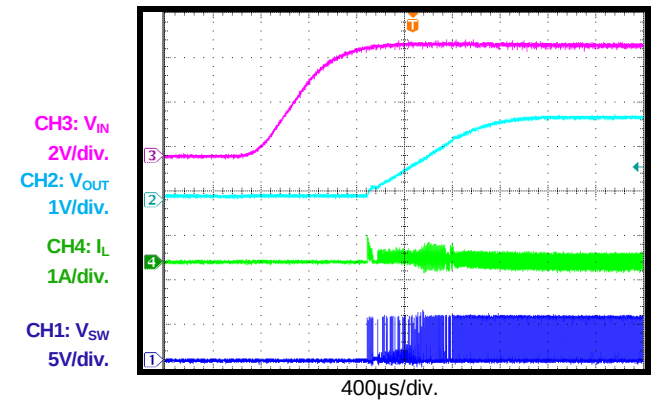
Start-Up through VIN

I_{OUT} = 0A, AAM



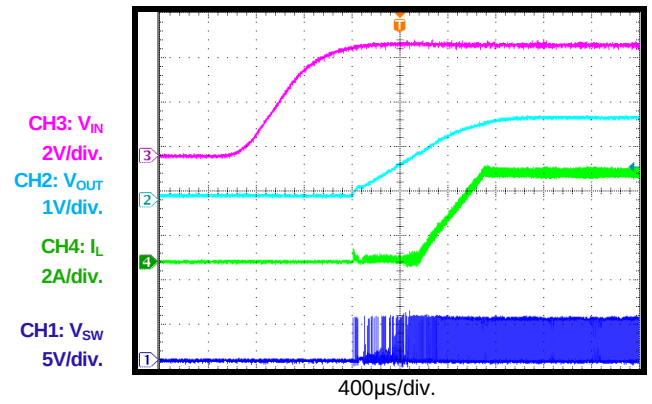
Start-Up through VIN

I_{OUT} = 0A, CCM



Start-Up through VIN

I_{OUT} = 4A

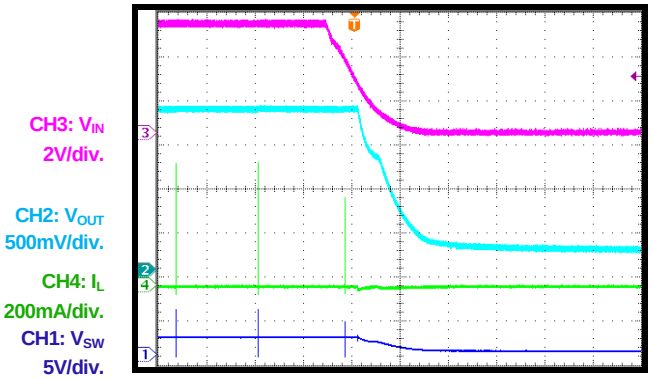


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

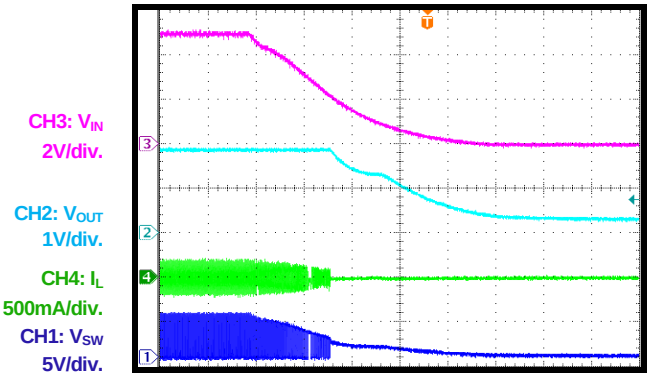
I_{OUT} = 0A, AAM



10ms/div.

Shutdown through VIN

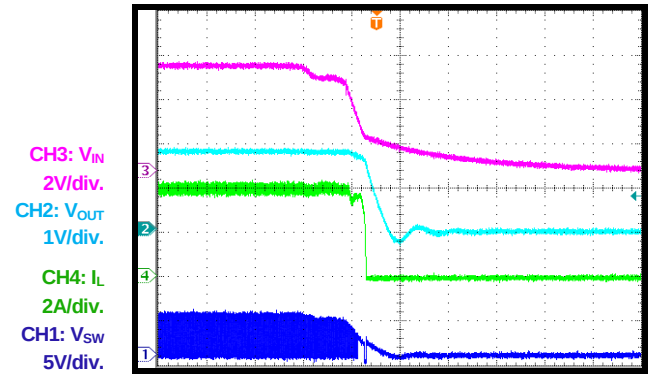
I_{OUT} = 0A, CCM



4ms/div.

Shutdown through VIN

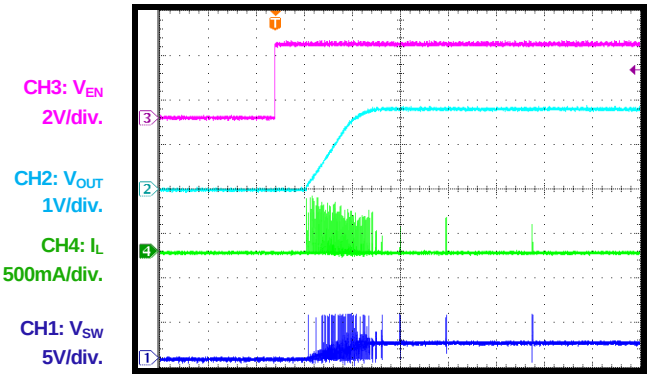
I_{OUT} = 4A



40µs/div.

Start-Up through EN

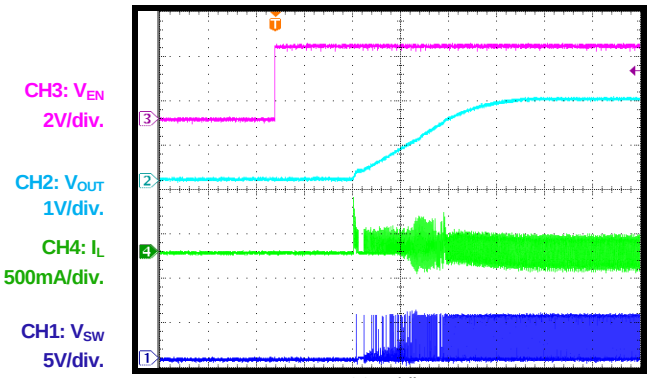
I_{OUT} = 0A, AAM



1ms/div.

Start-Up through EN

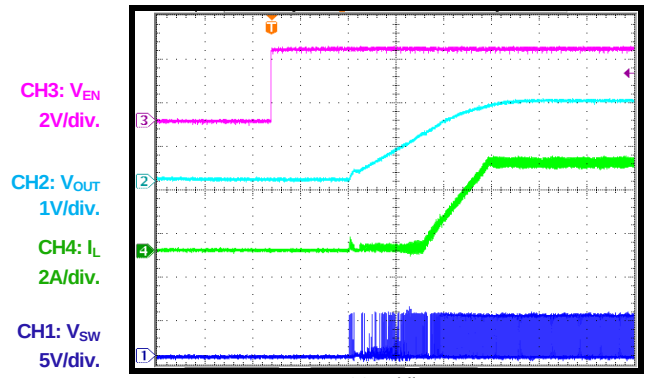
I_{OUT} = 0A, CCM



400µs/div.

Start-Up through EN

I_{OUT} = 4A



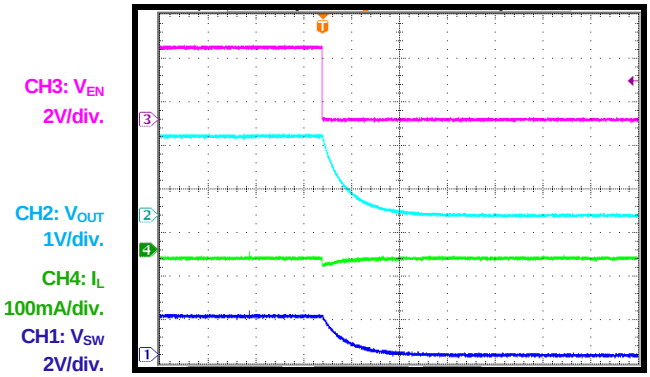
400µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Shutdown through EN

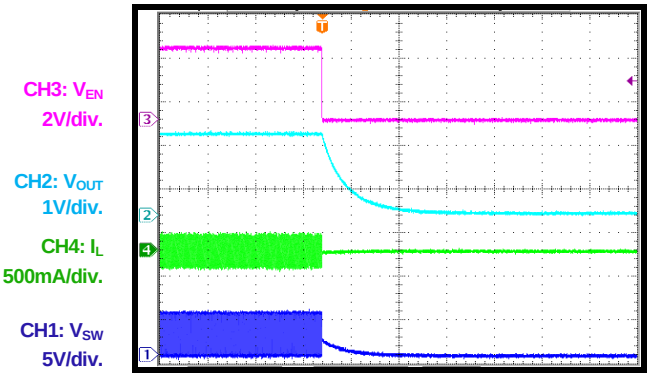
I_{OUT} = 0A, AAM



10ms/div.

Shutdown through EN

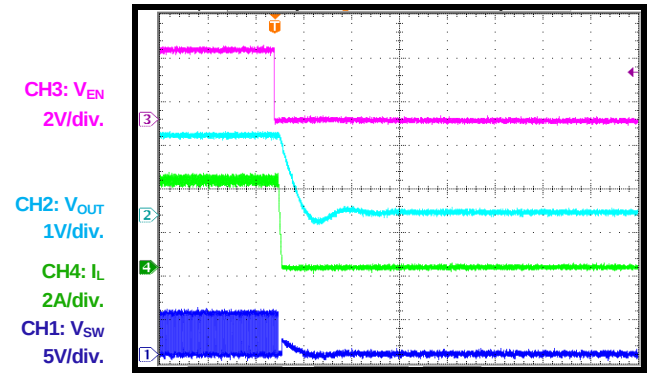
I_{OUT} = 0A, CCM



10ms/div.

Shutdown through EN

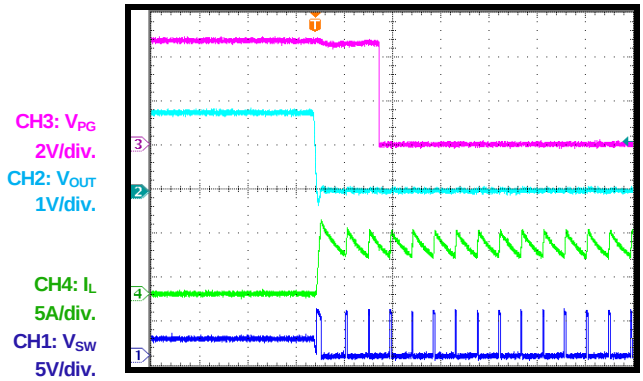
I_{OUT} = 4A



40µs/div.

Short-Circuit Protection (SCP) Entry

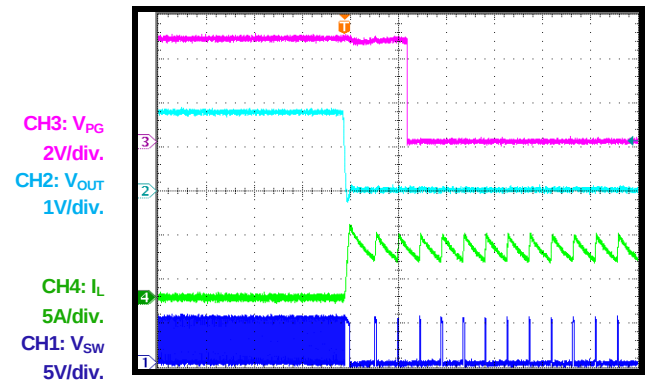
I_{OUT} = 0A, AAM



20µs/div.

Short-Circuit Protection (SCP) Entry

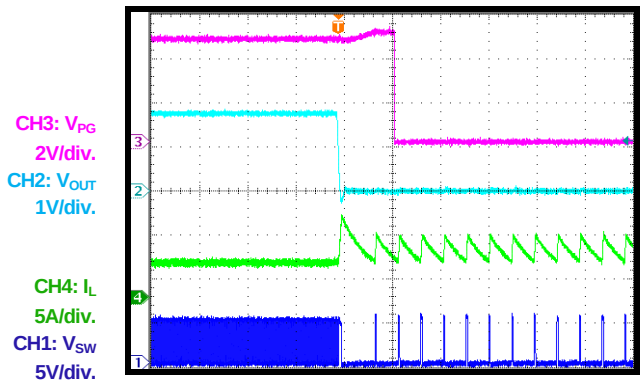
I_{OUT} = 0A, CCM



20µs/div.

Short-Circuit Protection (SCP) Entry

I_{OUT} = 4A



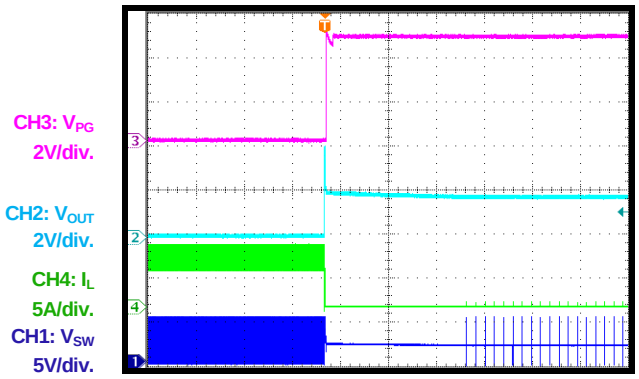
20µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Short-Circuit Protection (SCP) Recovery

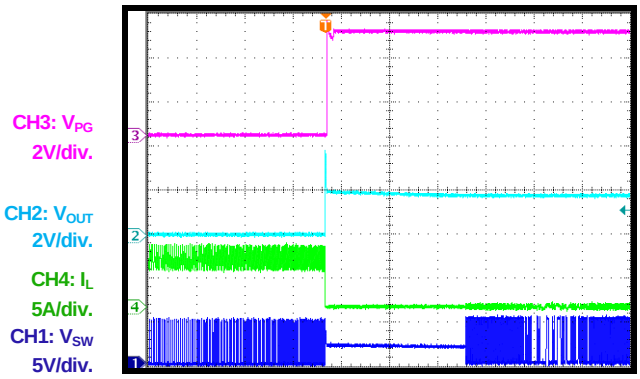
I_{OUT} = 0A, AAM



100ms/div.

Short-Circuit Protection (SCP) Recovery

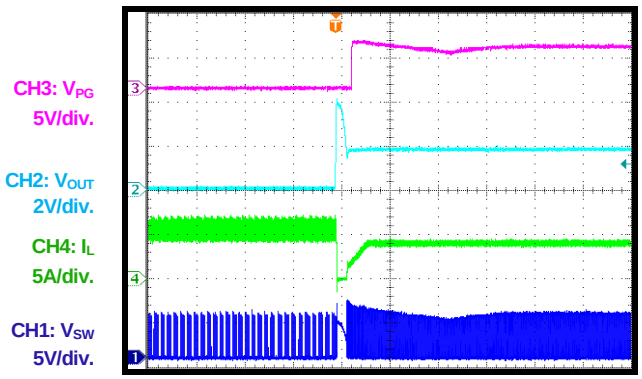
I_{OUT} = 0A, CCM



100ms/div.

Short-Circuit Protection (SCP) Recovery

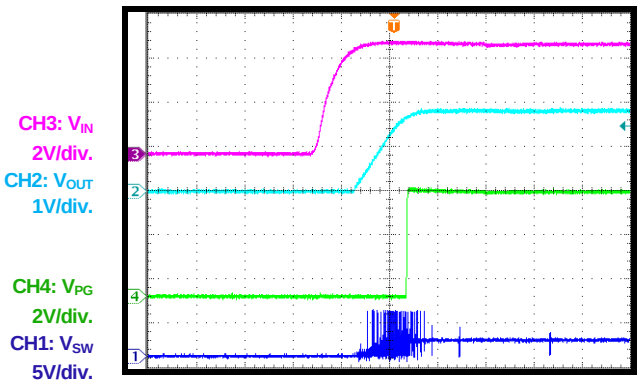
I_{OUT} = 4A



1ms/div.

PG Start-Up through VIN

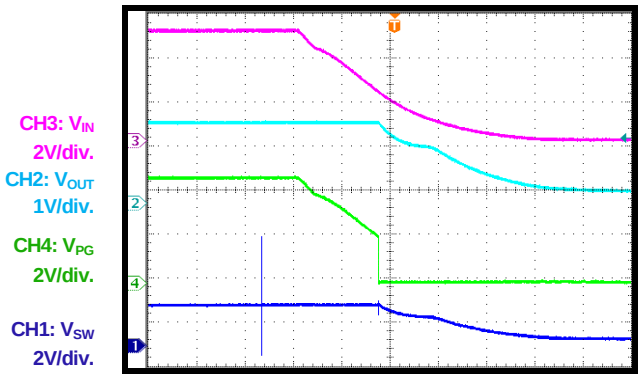
I_{OUT} = 0A, AAM



1ms/div.

PG Shutdown through VIN

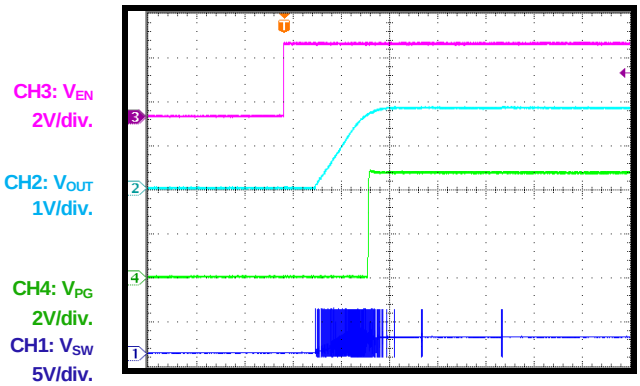
I_{OUT} = 0A, AAM



4ms/div.

PG Start-Up through EN

I_{OUT} = 0A, AAM



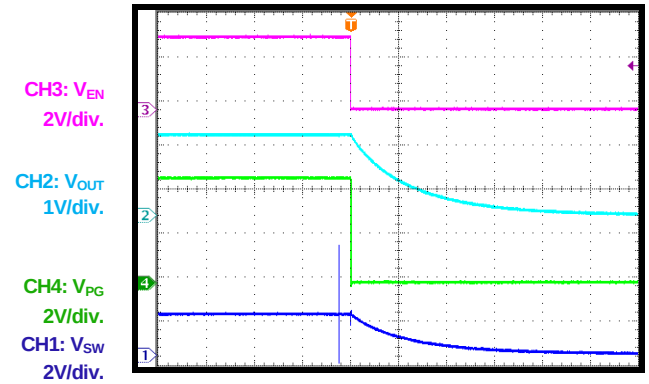
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

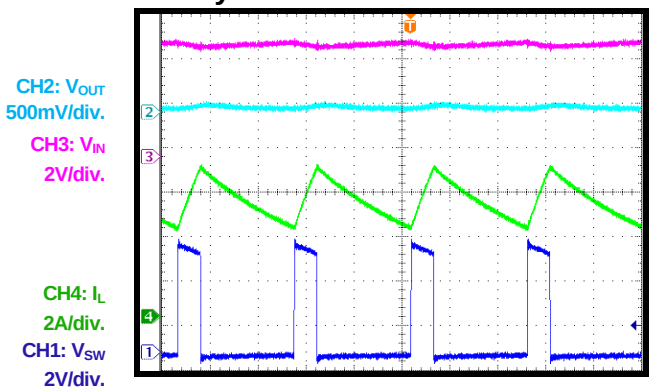
V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

PG Shutdown through EN

I_{OUT} = 0A, AAM

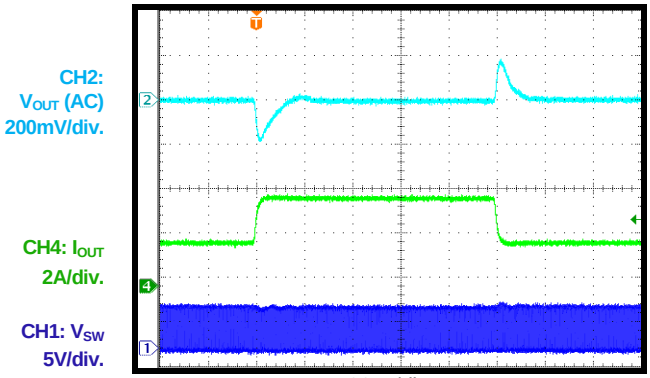


Short-Circuit Protection (SCP) Steady State



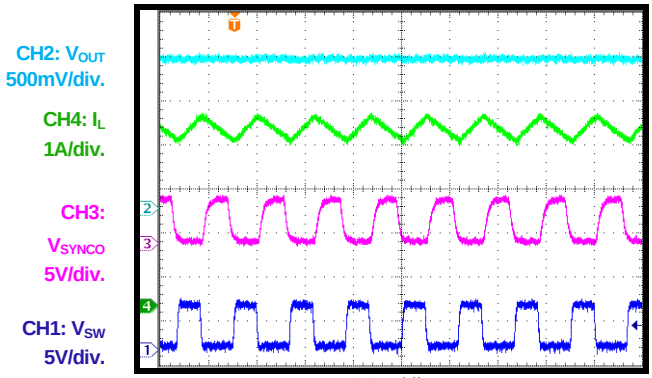
Load Transient

I_{OUT} = 2A to 4A, 1.6A/µs



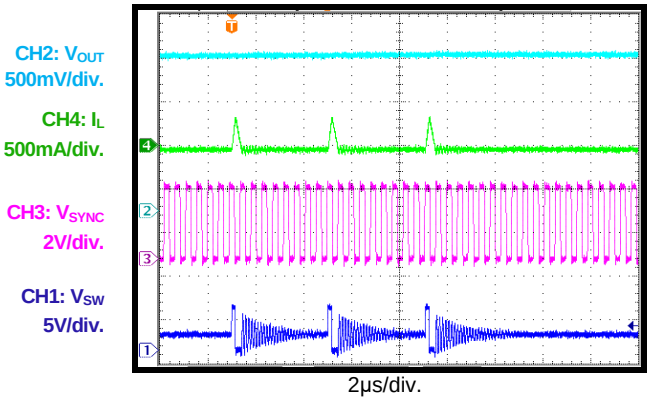
SYNCO

I_{OUT} = 4A



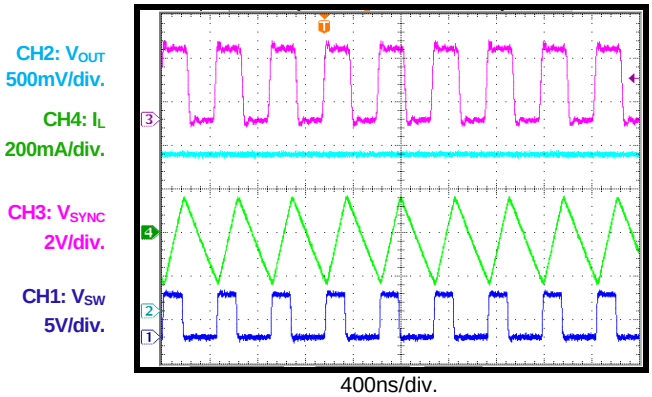
SYNCIN

I_{OUT} = 0A, AAM, SYNC clock = 2.2MHz



SYNCIN

I_{OUT} = 0A, FCCM, SYNC clock = 2.2MHz

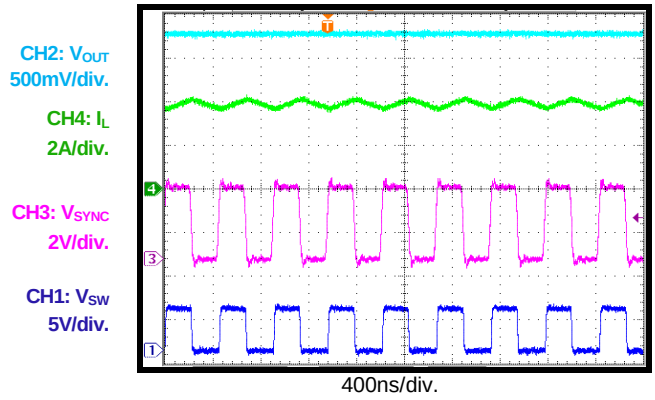


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 44µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

SYNCIN

I_{OUT} = 4A, SYNC clock = 2.2MHz



FUNCTIONAL BLOCK DIAGRAM

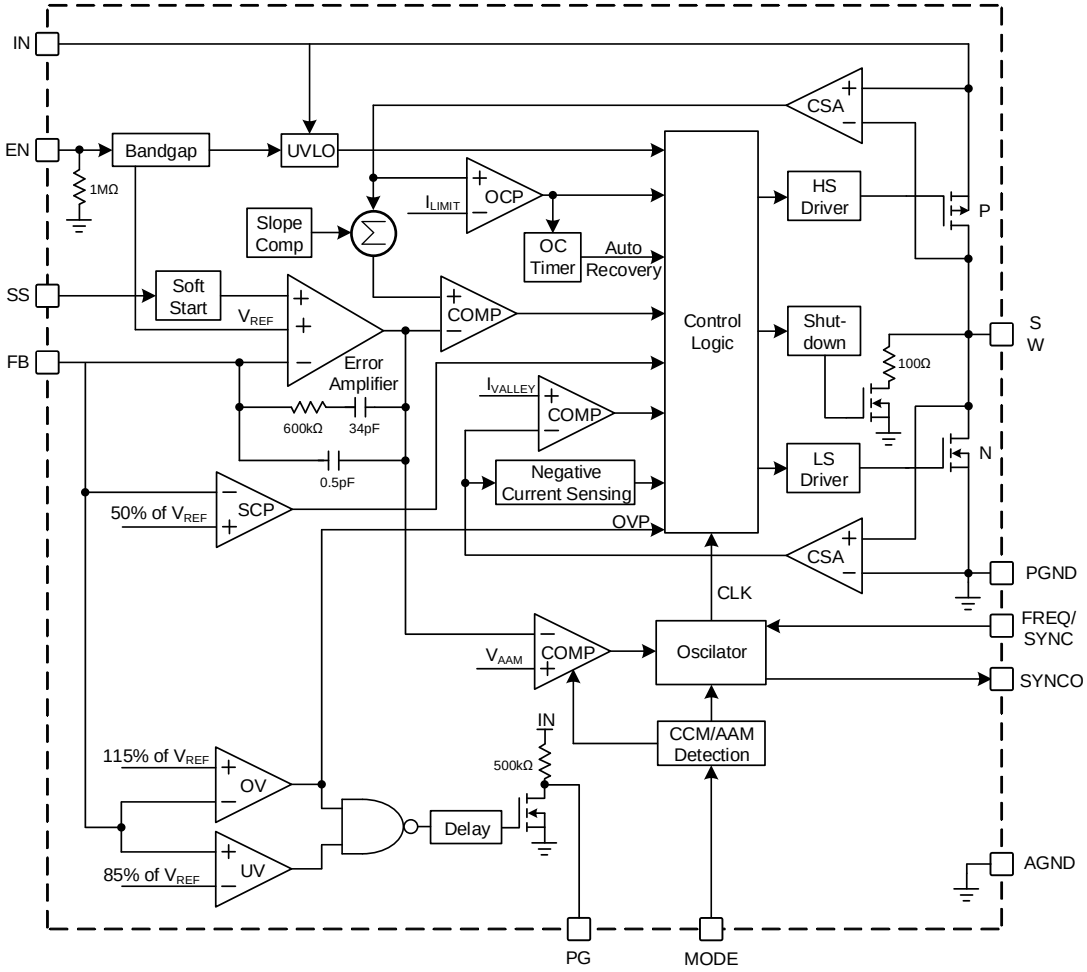


Figure 1: Functional Block Diagram

OPERATION

The MPQ2167B is a fully integrated, synchronous, rectified, step-down, non-isolated switch-mode converter. It uses peak current control mode with internal compensation for faster transient response and cycle-by-cycle current limiting.

The device offers a 2.7V to 6.0V input supply range, and can achieve up to 4A of continuous output current with excellent load and line regulation over an ambient temperature range of -40°C to +125°C. The output voltage can be regulated as low as 0.606V.

The MPQ2167B is optimized for low-voltage portable applications where efficiency and small size are critical. It can operate with a maximum 2.2MHz switching frequency, which enables the use of a smaller inductor while providing excellent efficiency. It also allows for high power-conversion efficiency under light-load conditions with AAM.

Forced Continuous Conduction Mode (FCCM)

Pull MODE above 1.2V to force the converter into forced continuous conduction mode (FCCM). In FCCM, the MPQ2167B operates in a fixed-frequency, peak current control mode to regulate the output voltage, regardless of the output current. An internal clock initiates an FCCM cycle.

At the rising edge of the clock, the high-side MOSFET (HS-FET) turns on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage (V_{COMP}), which is the output of the internal error amplifier. The output voltage of the error amplifier is based on the difference of the output feedback voltage and the internal high-precision reference. This value determines how much energy should be transferred to the load. A higher load current leads to an increased V_{COMP}.

When the HS-FET is off, the low-side MOSFET (LS-FET) turns on and remains on until the next clock starts. During this time, the inductor current flows through the LS-FET. To avoid shoot-through, a dead time is asserted to avoid the HS-FET and LS-FET turning on at the same time. For each turn-on/off period in a switching cycle, the HS-FET remains on/off with a minimum on/off time limit.

AAM

Pull MODE below 0.4V to force the converter into light-load advanced asynchronous mode (AAM). There is an internally fixed AAM threshold voltage (V_{AAM}). Under light-load conditions, V_{COMP} is low. If V_{COMP} exceeds V_{AAM}, the MPQ2167B first enters discontinuous conduction operation with a fixed frequency while the inductor current approaches zero.

If the load decreases further, or there is no load that drops V_{COMP} below V_{AAM}, the internal clock is blocked, and the MPQ2167B skips some pulses. During this time, V_{FB} is below V_{REF}, so V_{COMP} ramps up until it exceeds V_{AAM}. The internal clock is reset, and the crossover time is used as a benchmark for the next clock cycle. This control scheme achieves high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As the output current increases from a light-load condition, V_{COMP} and the switching frequency increase.

If the output current exceeds the critical level when V_{COMP} exceeds V_{AAM}, the MPQ2167B resumes fixed-frequency control, which functions similarly to FCCM (see Figure 2).

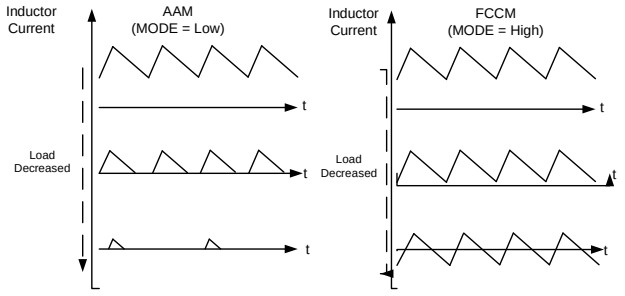


Figure 2 : AAM and FCCM

Enable

The MPQ2167B can be enabled or disabled via a remote EN signal that is referenced to ground. The remote EN control operates with a positive logic that is compatible with popular logic devices. Positive logic implies that when the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), the converter is enabled by pulling EN above 1.2V. Float or ground the EN pin to disable the MPQ2167B. There is an internal 1MΩ resistor from EN to ground.

Oscillator and SYNC Function

The oscillating frequency of the MPQ2167B can be configured by an external frequency resistor. The frequency resistor should be placed between FREQ and GND, a as close to the device as possible.

Select the R_{FREQ} value based on the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics section on page 10.

The FREQ pin can synchronize the internal oscillator rising edge to an external clock falling edge. To drive the internal logic, choose the correct SYNC clock amplitude using the Electrical Characteristics section on page 5. The recommended external SYNC frequency is between 300kHz and 2.2MHz.

If the pulse width is short, any parasitic capacitance could make it difficult to see a clear rising and falling edge. It is recommended to make the pulse longer than 100ns. Add the external SYNC clock (300kHz to 2.2MHz) before the device starts up and keep the clock until the device is off. Constant high, constant low, or a high-to-low transition on the SYNC signal cannot occur during the operation.

The MPQ2167B also has SYNCO pin that can output a 180° phase-shift clock. This signal synchronizes other devices to the same operation frequency, but opposite phase, to reduce the total input current ripple.

Soft Start (SS) and Output Discharge

To avoid overshoot at start-up, the MPQ2167B has a soft start (SS) that ramps up the output voltage in a controlled slew rate when EN goes high.

When the soft-start time begins, an internal current source charges the external soft-start capacitor. When the SS voltage (V_{SS}) falls below the internal reference (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. After soft start finishes, the MPQ2167B enters steady state. It can be used for tracking and sequencing.

The SS time set by the external SS capacitor can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.606V), and I_{SS} is the internal 4μA SS charge current.

When SS is floating, the SS time is 1ms following the internal setting.

When disabled or in an input shutdown, the MPQ2167B discharges the output voltage to GND through an internal 100Ω resistor that is placed in parallel to the LS-FET.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} at start-up, the output has a pre-biased voltage, and the MOSFETs remain off until V_{SS} exceeds V_{FB}.

100% Duty Cycle

The MPQ2167B can operate with 100% duty cycle, which can extend the battery life. When the input voltage is too low to regulate the output, the device turns on the HS-FET to achieve maximum output voltage.

Power Good Indicator

The MPQ2167B has power good (PG) indication. PG is the open drain of the MOSFET. In the presence of an input voltage, the MOSFET turns on PG is pulled to GND before a soft start is ready. When the output voltage is within a ±15% window of the rated voltage set by FB (V_{FB}), PG is pulled up to V_{IN} by an internal resistor after a delay. If V_{FB} moves outside the ±15% range with a hysteresis, the device pulls PG low to indicate a failure output status.

Over-Current Protection (OCP)

The MPQ2167B has a 6.7A, cycle-by-cycle peak current limit control. The inductor current is monitored while the HS-FET is on. Once the inductor current hits the current limit, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor drops below a current threshold, (valley current limit). This prevents the inductor current from running away and possibly damaging the components.

When the valley current limit is triggered, the OCP timer starts immediately. The OCP timer is set at 100μs. Hitting the valley current limit during each cycle during this 100μs timeframe triggers short-circuit protection (SCP).

Short-Circuit Protection (SCP)

When a short circuit occurs, the MPQ2167B immediately reaches its current limit. Meanwhile, the output voltage drops until V_{FB} is below 50% of V_{REF} (0.606V). Then the device considers this a dead short output and triggers short-circuit protection (SCP). In SCP, the inductor current is monitored while the HS-FET is on. When the inductor current reaches the current limit, the HS-FET turns off. Then the LS-FET turns on to discharge the energy, and the inductor current decreases.

The HS-FET does not turn on again until the inductor drops below the valley current limit. The device repeats this operation until the short circuit disappears, then the output returns to the regulation level. This protection mode prevents the inductor current from running away and possibly damaging the components.

Over-Voltage Protection (OVP)

The MPQ2167B monitors the output voltage through FB to detect output over-voltage conditions. If V_{FB} exceeds 115% of V_{REF} (0.606V) and triggers OVP, the LS-FET turns on to discharge VOUT until the inductor current drops to zero. During this process, the HS-FET remains off. Then the LS-FET turns off, and the output is discharged through the internal 100Ω resistor in parallel with the LS-FET. The control does not switch until the output is within the regulation range.

Under Voltage Lockout Protection (UVLO)

The device has input under-voltage lockout (UVLO) protection to ensure reliable output power. Assuming EN is active, the MPQ2167B is powered on when the input voltage exceeds the UVLO rising threshold. It is powered off when the input voltage drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient voltage. It is a non-latch protection.

Thermal Shutdown

Thermal protection prevents the chip from operating at exceedingly high temperatures. The MPQ2467B monitors the IC temperature internally. If the junction temperature exceeds the threshold value (typically 170°C), it shuts down the whole chip. This is a non-latch protection. There is a 25°C hysteresis. When the junction temperature drops to about 145°C, the device resumes operation by initiating a soft start.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure the rest of the circuitries are ready, then slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} UVLO, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 3). The feedback resistor R1 must account for both stability and dynamic response, so it cannot be too large or too small. R1 is estimated to be 100kΩ. Calculate R2 with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.606} - 1} \quad (2)$$

Using a T-type feedback network is highly recommended (see Figure 3).

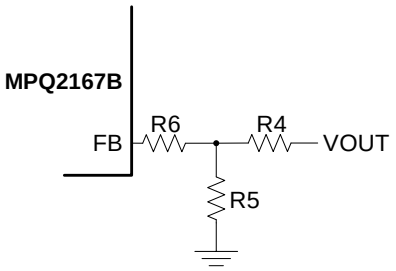


Figure 3: Feedback Network

R6 + R4 sets the loop bandwidth. A higher R6 + R4 creates a lower bandwidth. To ensure loop stability, it is recommended to limit the bandwidth to about 10% of the switching frequency.

Table 1 lists the recommended feedback divider resistor values for common output voltages. Check the loop analysis before using in application. If required, change the resistance of R_T for loop stability.

Table 1: Resistor Values for a Typical V_{OUT}

V_{OUT} (V)	R6 (kΩ)	R4 (kΩ)	R5 (kΩ)
1.2	100	100 (1%)	100 (1%)
1.5	100	100 (1%)	66.5 (1%)
1.8	100	100 (1%)	49.9 (1%)
2.5	100	100 (1%)	31.6 (1%)
3.3	100	100 (1%)	22.1 (1%)

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. For a default 2.1MHz application, a 0.47µH to 1.5µH inductor is recommended. For highest efficiency, choose an inductor with a DC resistance below 15mΩ. When setting the frequency or synchronization function, the inductance should increase while the frequency decreases. A large inductor results in less ripple current and a lower output ripple voltage. However, a larger inductor means the inductor has a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductor value is to make the inductor ripple current about 30% of the maximum load current. Ensure the peak inductor current is below the device peak current limit. The inductance can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. Estimate the peak inductor current with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. Other types, such as Y5V and Z5U, must not be used, as these lose capacitance with frequency, temperature, and bias voltage.

Place the input capacitors as close to IN as possible. For most applications, a 22µF capacitor is sufficient. For a higher output voltage, use a 47µF capacitor to improve system stability. For a small solution size, choose a proper package size capacitor with a rating voltage compliant to the input specification.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating, which must exceed the converter's

maximum input ripple current. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality ceramic capacitor (0.1μF) placed as close to the IC as possible. The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system design, choose an input capacitor that meets the specification.

The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the output DC voltage. Low-ESR ceramic capacitors are recommended for their smaller size and ability to maintain a low output voltage ripple. Electrolytic and polymer capacitors may also be used. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (9)$$

R_{ESR} is the equivalent series resistance of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Another consideration for the output capacitance is the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor is transferred to C_{OUT} and causes its voltage to rise. To achieve an appropriate overshoot relative to the regulated voltage, the output capacitance can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

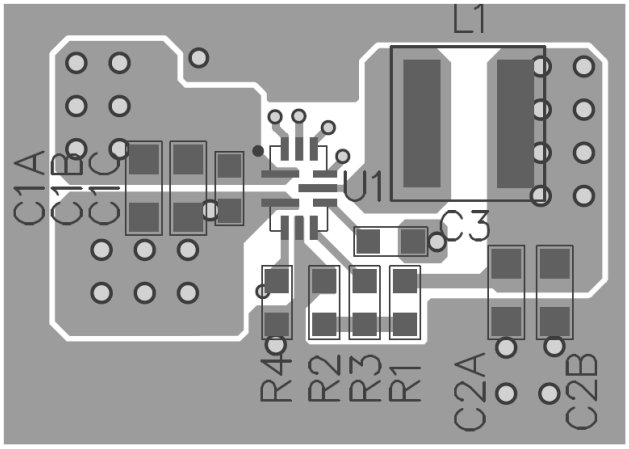
Where V_{OUTMAX} / V_{OUT} is the allowable maximum overshoot. After calculating the capacitance required for both the ripple and overshoot, choose the larger of the calculated values.

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ2167B can be optimized for a wide range of capacitance and ESR values.

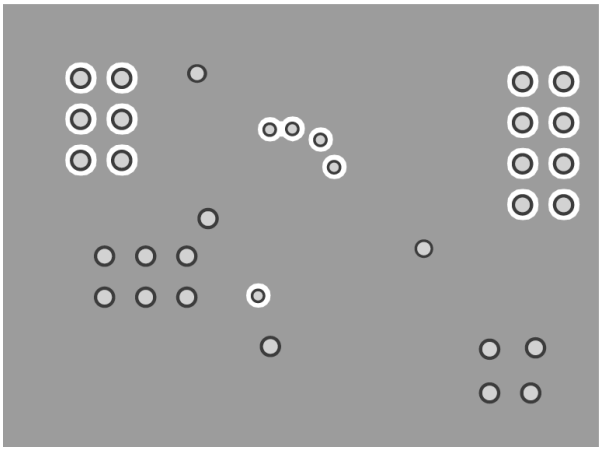
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to achieve better thermal performance. For the best results, refer to Figure 4 and follow the guidelines below:

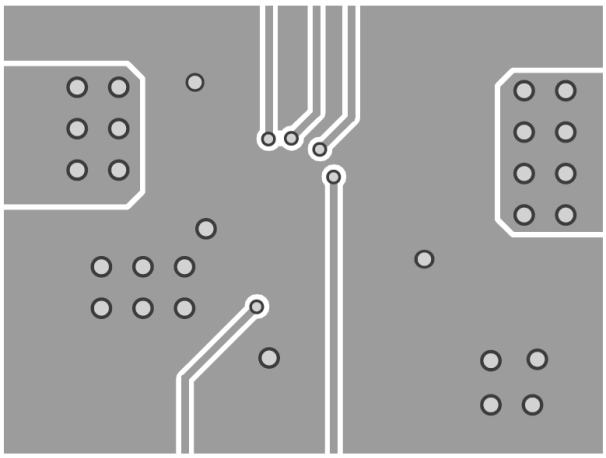
1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitors as close to IN as possible to minimize high-frequency noise.
3. Place the feedback resistor divider as close as possible to FB.
4. Route the FB trace away from the switching node.
5. Connect the bottom IN and SW pads to a large copper area to improve thermal performance.
6. Use large copper areas for the power planes (IN, SW, OUT, and GND) to minimize conduction loss and thermal stress.
7. Use multiple vias to connect the power planes to the internal layers.



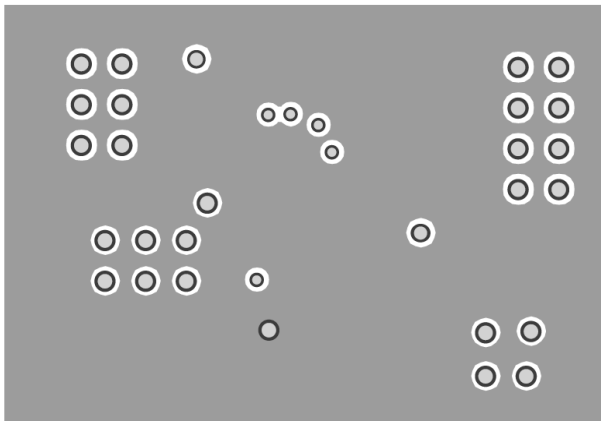
Top and Top Silk Layer



Inner Layer 1



Inner Layer 2



Bottom and Bottom Silk Layer

Figure 4: Recommended PCB Layout (7)

Note:

7) The recommended PCB layout is based on Figure 5.

TYPICAL APPLICATION CIRCUITS

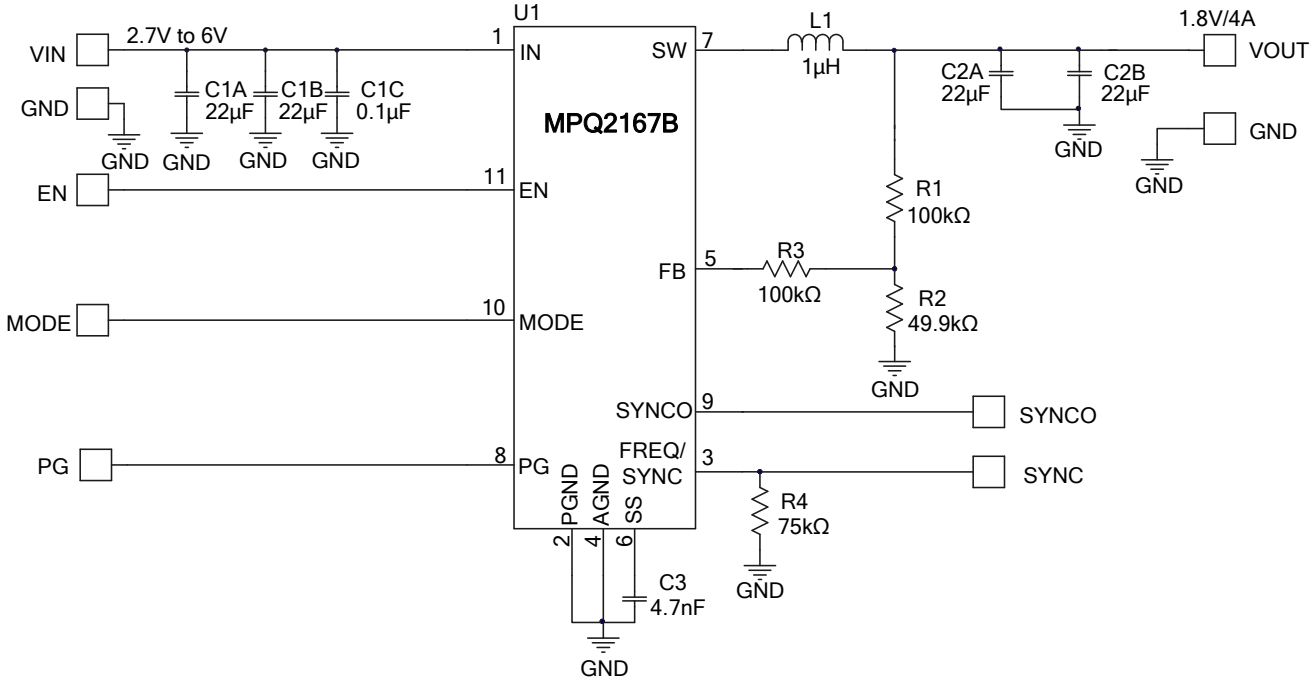


Figure 5: V_{OUT} = 1.8V, I_{OUT} = 4A Application Circuit

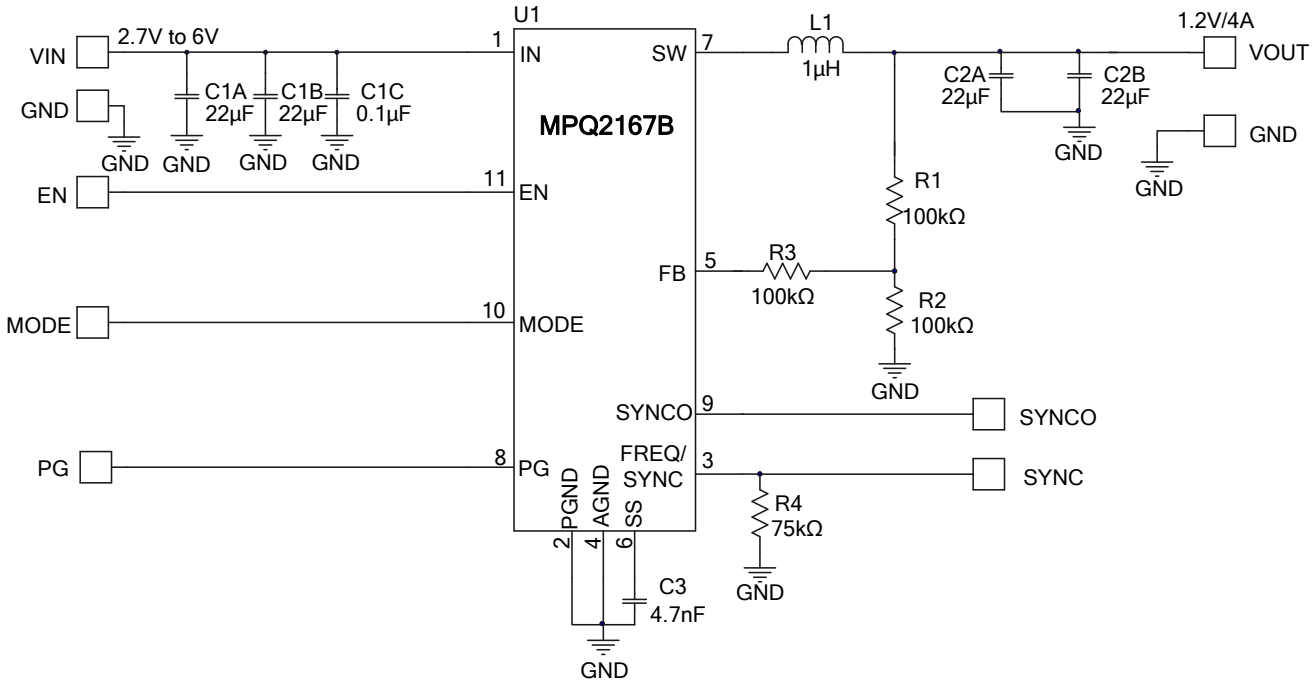
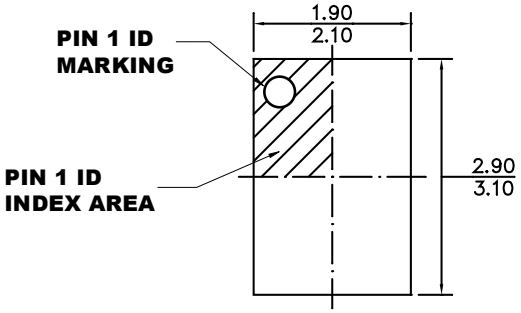


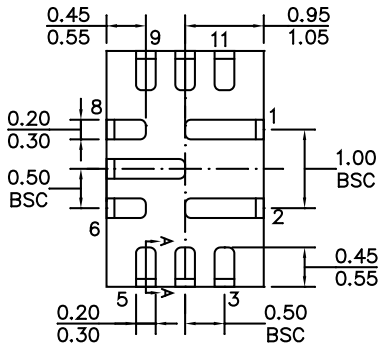
Figure 6: V_{OUT} = 1.2V, I_{OUT} = 4A Application Circuit

PACKAGE INFORMATION

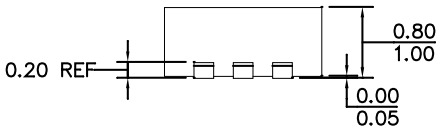
QFN-11 (2mmx3mm)
Wettable Flank



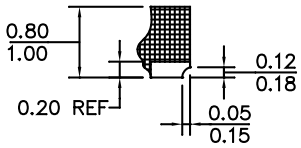
TOP VIEW



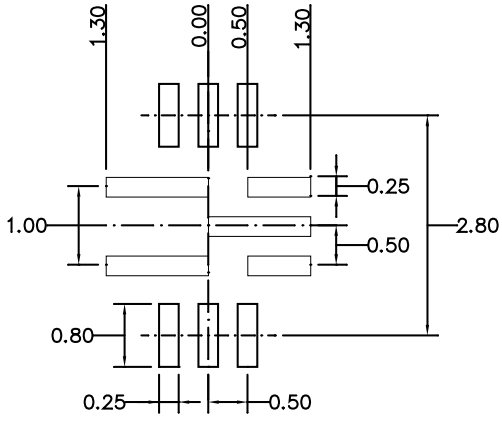
BOTTOM VIEW



SIDE VIEW



SECTION A-A

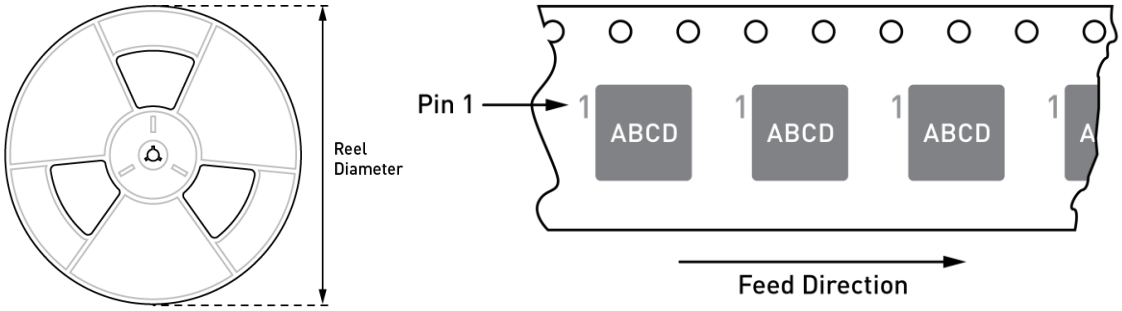


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) LAND PATTERNS OF PIN 1, 2, AND 7 HAVE THE SAME SHAPE.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2167BGDE-AEC1–Z	QFN-11 (2mmx3mm)	5000	13in	12mm	8mm