Document Number: AFT20S015N
Rev. 2, 04/2020

RoHS

RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

These 1.5 W RF power LDMOS transistors are designed for cellular base station applications covering the frequency range of 1805 to 2700 MHz.

2100 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 132 mA, P_{out} = 1.5 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	17.5	22.0	8.9	-43.0	-11
2140 MHz	17.6	22.0	9.0	-44.0	-12
2170 MHz	17.6	22.0	9.1	-44.0	-14

1800 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 132 mA, P_{out} = 1.5 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.0	21.0	9.2	-42.0	-11
1840 MHz	18.1	22.0	9.2	-44.0	-10
1880 MHz	18.0	22.0	9.1	-45.0	-10

2600 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 132 mA, P_{out} = 2.1 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

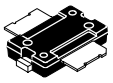
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2300 MHz	15.7	23.0	9.0	-45.0	-6
2400 MHz	16.0	23.0	8.8	-44.0	-7
2500 MHz	15.8	23.0	8.6	-43.0	-6
2600 MHz	15.8	21.0	8.5	-43.0	-7
2700 MHz	15.5	20.0	8.4	-42.0	-8

Features

- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems
- Optimized for Doherty applications

AFT20S015N
AFT20S015GN

1805–2700 MHz, 1.5 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTORS



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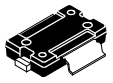
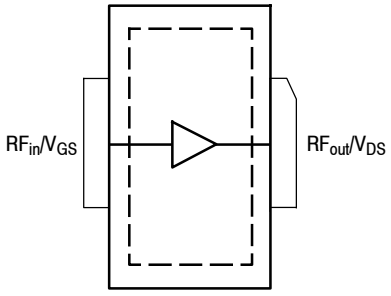
AFT20S015N



TO-270-2 GULL
PLASTIC
AFT20S015GN



(Top View)

Note: The backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	11 0.1	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 1.5 W CW, 28 Vdc, I_{DQ} = 132 mA, 2140 MHz	$R_{\theta JC}$	4.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 17.6 μAdc)	$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 132 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.4	3.0	3.4	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 176 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

(continued)

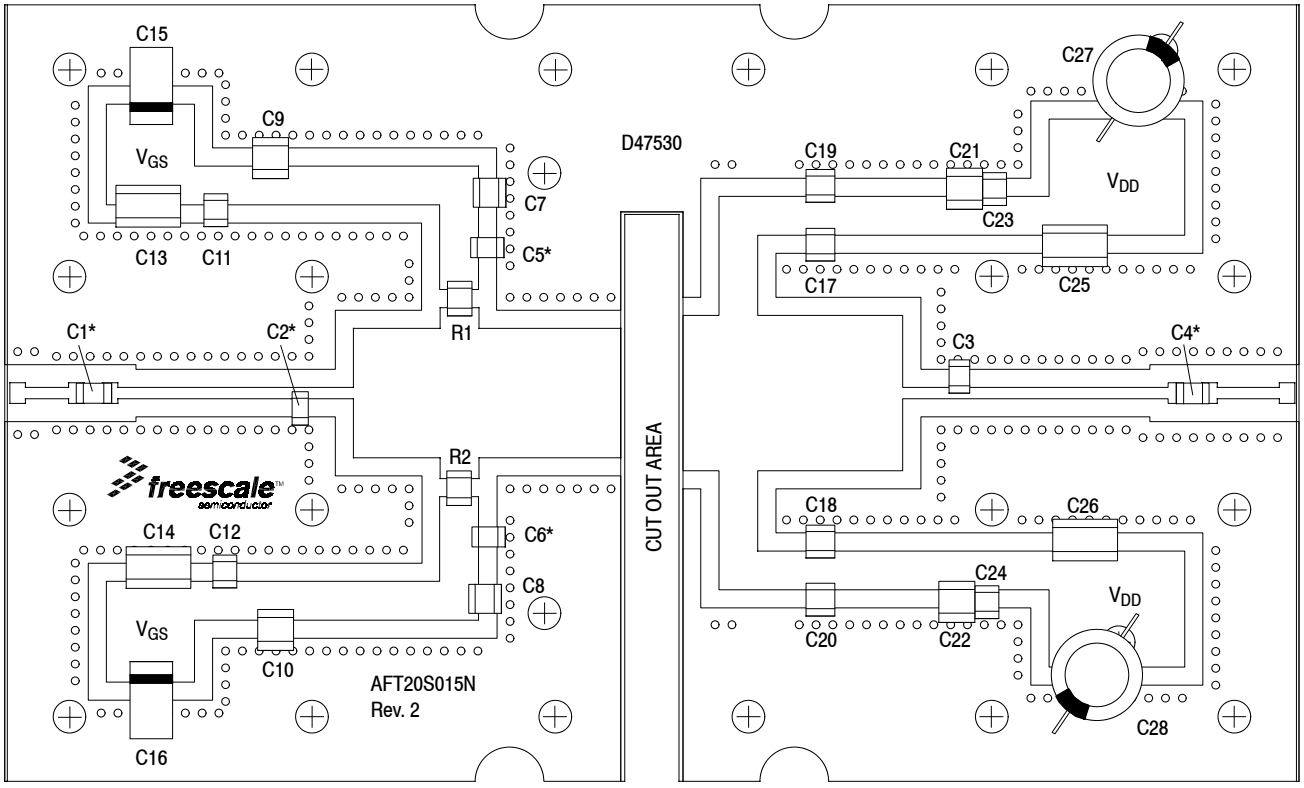
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 132 mA, P_{out} = 1.5 W Avg., f = 2170 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16.0	17.6	19.0	dB
Drain Efficiency	η_D	20.0	22.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	8.6	9.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-44.0	-41.0	dBc
Input Return Loss	IRL	—	-14	-9	dB
Load Mismatch (In NXP Test Fixture, 50 ohm system) I_{DQ} = 132 mA, f = 2140 MHz					
VSWR 10:1 at 32 Vdc, 14 W CW (3) Output Power (3 dB Input Overdrive from 12 W CW (3) Rated Power)	No Device Degradation				
Typical Performance (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 132 mA, 2110-2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	16.2 (3,4)	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110-2170 MHz frequency range.)	Φ	—	-16	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	170	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 1.5 W Avg.	G_F	—	0.05	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) (3)	ΔP1dB	—	0.004	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
AFT20S015NR1	R1 Suffix = 500 Units, 24 mm Tape Width, 13-inch Reel	TO-270-2
AFT20S015GNR1		TO-270G-2

1. Part internally matched on input.
2. Measurements made with device in straight lead configuration, before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
3. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
4. Calculated from load pull P3dB measurements.



*C1, C2, C4, C5 and C6 are mounted vertically.

Note: NXP has begun the transition of marking printed circuit boards (PCBs) with the NXP exception logo. PCBs may have either Freescale or NXP markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. AFT20S015N Test Circuit Component Layout — 2110-2170 MHz

Table 7. AFT20S015N Test Circuit Component Designations and Values — 2110-2170 MHz

Part	Description	Part Number	Manufacturer
C1	8.2 pF Chip Capacitor	ATC100B8R2CT500XT	ATC
C2	2.4 pF Chip Capacitor	ATC800B2R4BT500XT	ATC
C3	1.7 pF Chip Capacitor	ATC100B1R7BT500XT	ATC
C4	9.1 pF Chip Capacitor	ATC100B9R1CT500XT	ATC
C5, C6	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C7, C8	240 pF Chip Capacitors	ATC100B241JT200XT	ATC
C9, C10, C21, C22	220 pF Chip Capacitors	C1812C224K5RAC-TU	Kemet
C11, C12, C23, C24	0.1 μF Chip Capacitors	CDR33BX104AKWS	AVX
C13, C14, C25, C26	2.2 μF Chip Capacitors	C1825C225J5RAC-TU	Kemet
C15, C16	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C17, C18, C19, C20	75 pF Chip Capacitors	ATC800B750JT500XT	ATC
C27, C28	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	1 Ω Chip Resistors	CRCW12061R00FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D47530	MTL

TYPICAL CHARACTERISTICS — 2110–2170 MHZ

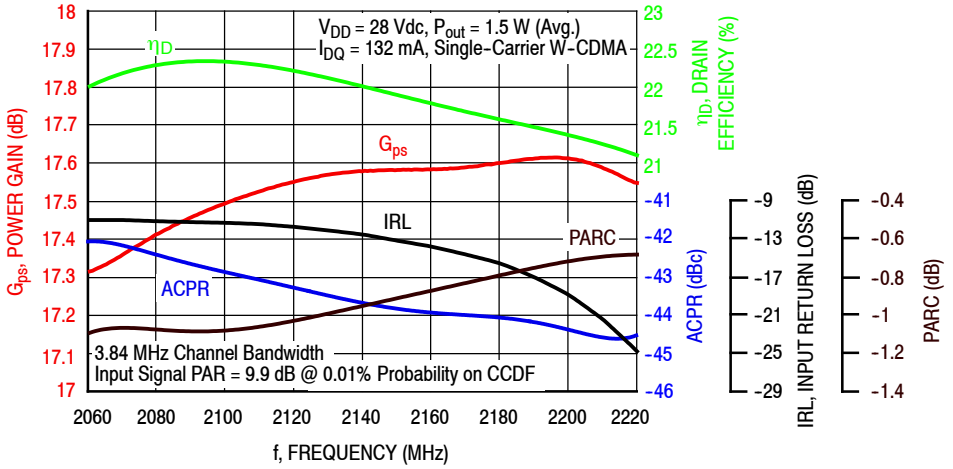


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 1.5 Watts Avg.

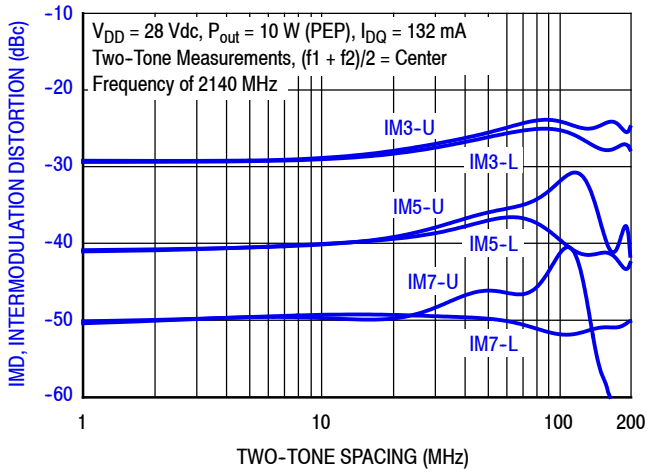


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

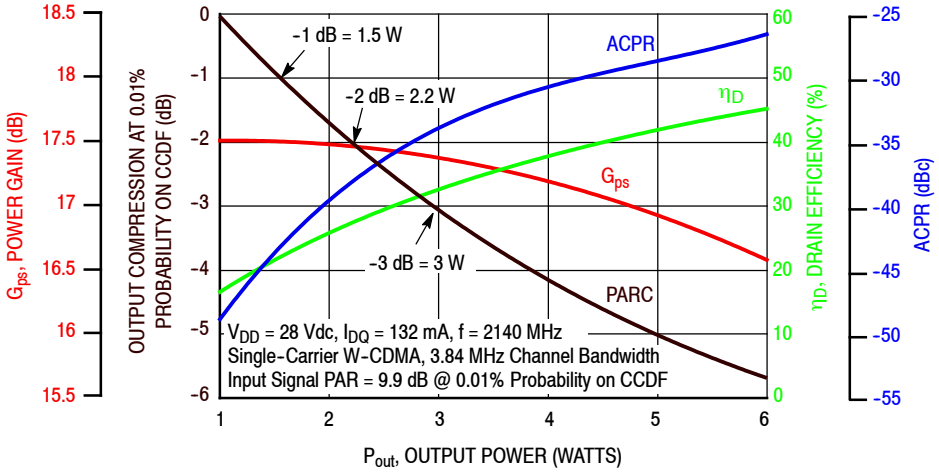


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2170 MHz

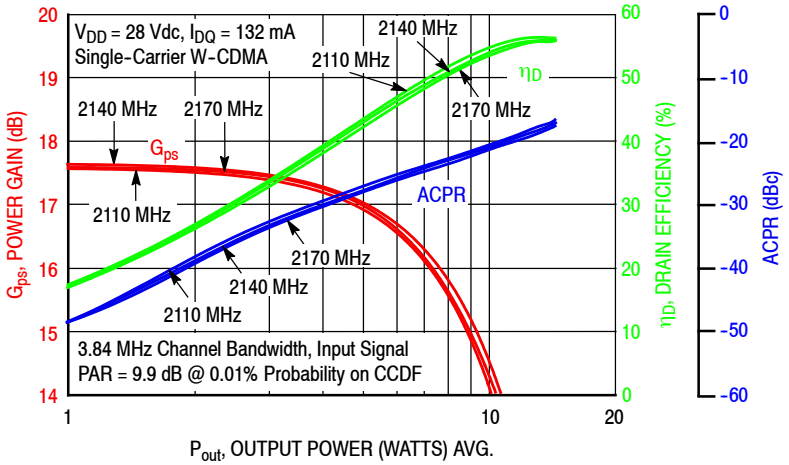


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

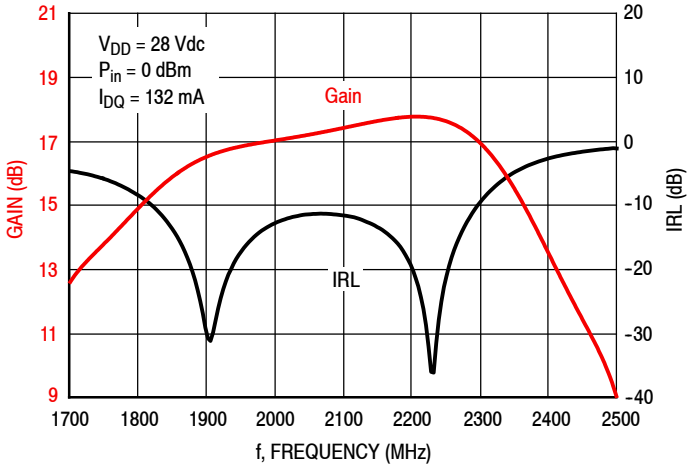
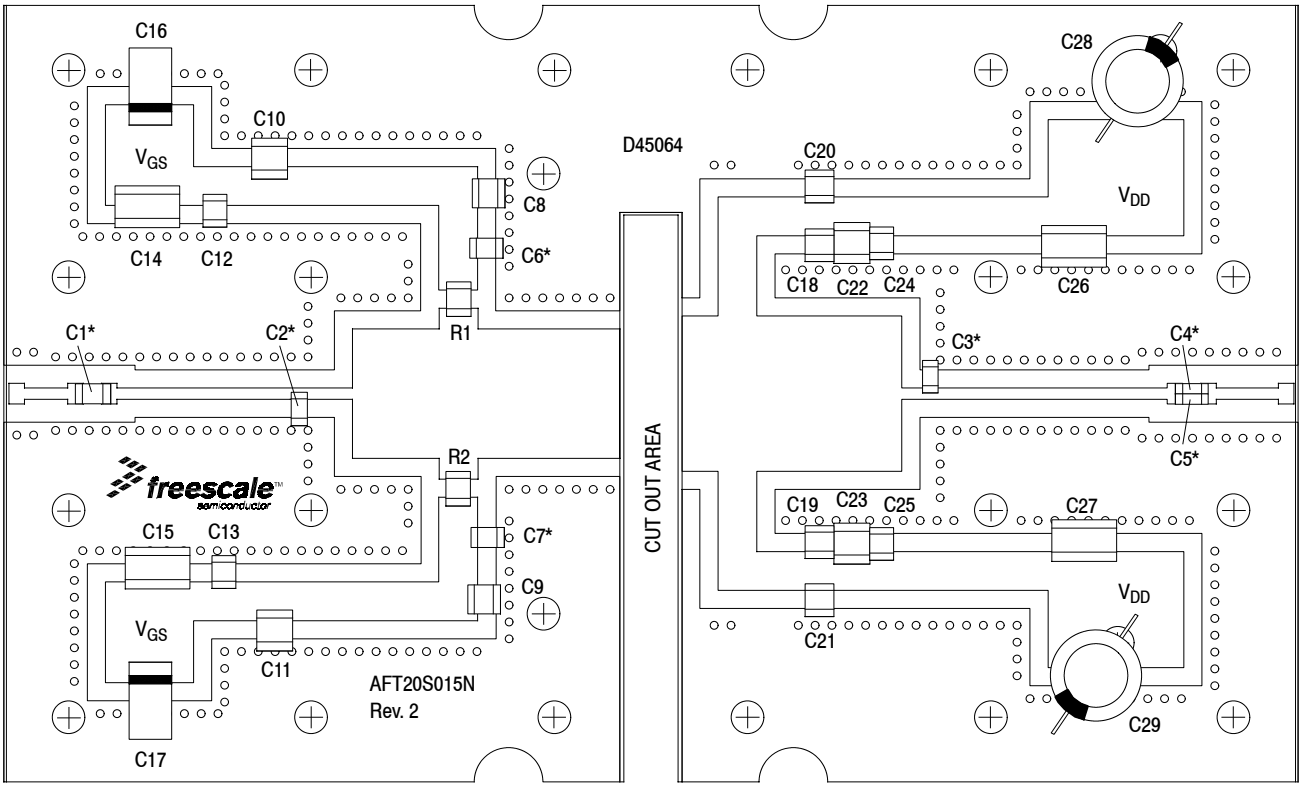


Figure 7. Broadband Frequency Response

ALTERNATE CHARACTERIZATION — 1805–1880 MHz



*C1, C2, C3, C4, C5, C6 and C7 are mounted vertically.

Note: NXP has begun the transition of marking printed circuit boards (PCBs) with the NXP exception logo. PCBs may have either Freescale or NXP markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 8. AFT20S015N Test Circuit Component Layout — 1805–1880 MHz

Table 8. AFT20S015N Test Circuit Component Designations and Values — 1805–1880 MHz

Part	Description	Part Number	Manufacturer
C1	11 pF Chip Capacitor	ATC100B11R0CT500XT	ATC
C2, C3	3.3 pF Chip Capacitors	ATC800B3R3BT500XT	ATC
C4, C5	47 pF Chip Capacitors	ATC600F47BT250XT	ATC
C6, C7	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C8, C9	240 pF Chip Capacitors	ATC100B241JT200XT	ATC
C10, C11, C22, C23	220 pF Chip Capacitors	C1812C224K5RAC–TU	Kemet
C12, C13, C24, C25	0.1 μF Chip Capacitors	CDR33BX104AKWS	AVX
C14, C15, C26, C27	2.2 μF, 50 V Chip Capacitors	C1825C225J5RAC–TU	Kemet
C16, C17	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C18, C19, C20, C21	75 pF Chip Capacitors	ATC800B750JT500XT	ATC
C28, C29	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26–RH	Multicomp
R1, R2	1 Ω Chip Resistors	CRCW12061R00FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D45064	MTL

ALTERNATE CHARACTERIZATION — 1805–1880 MHz

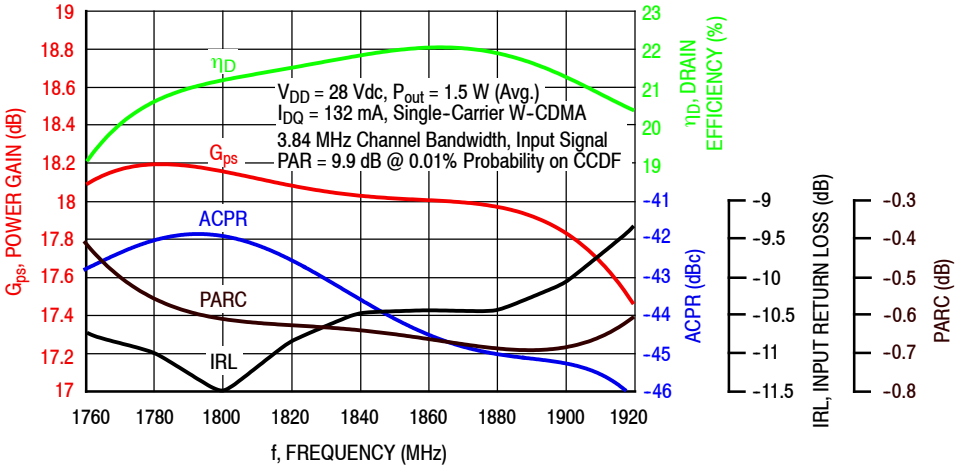


Figure 9. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 1.5 Watts Avg.

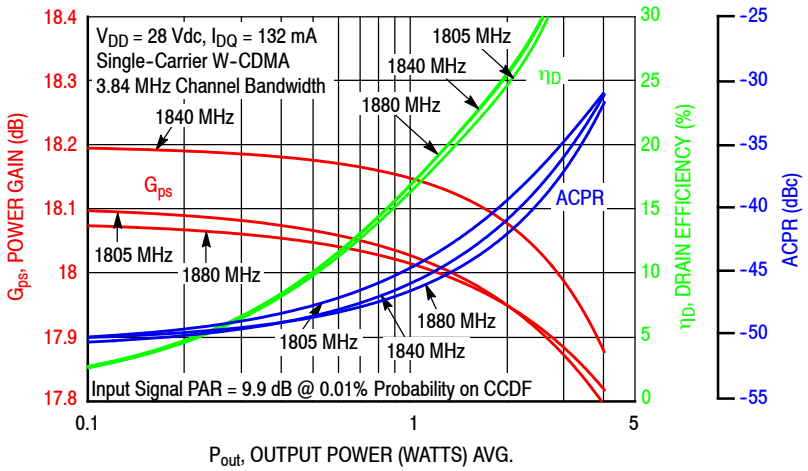


Figure 10. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

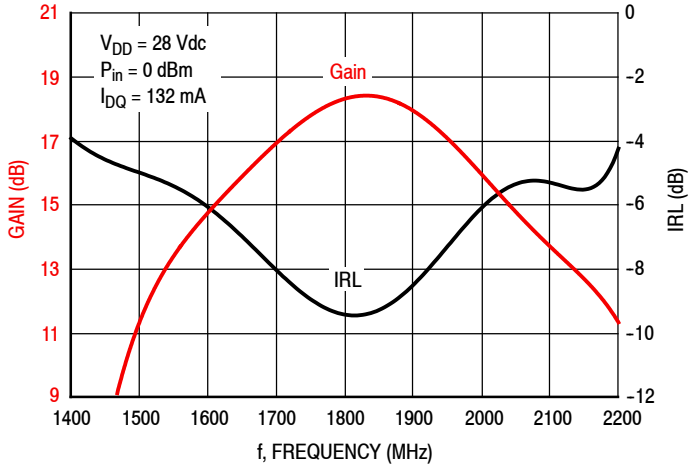
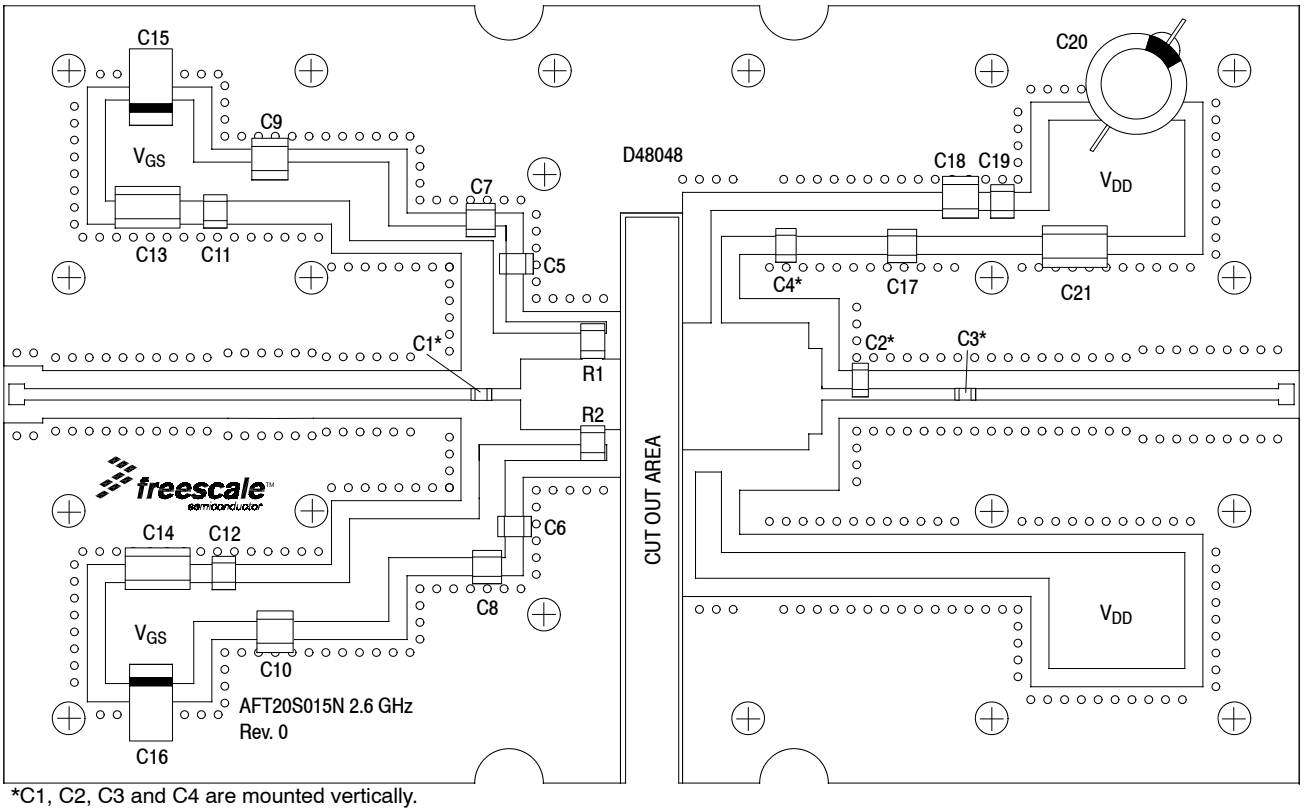


Figure 11. Broadband Frequency Response

ALTERNATE CHARACTERIZATION — 2300–2700 MHz



*C1, C2, C3 and C4 are mounted vertically.

Note: NXP has begun the transition of marking printed circuit boards (PCBs) with the NXP exception logo. PCBs may have either Freescale or NXP markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 12. AFT20S015N Test Circuit Component Layout — 2300–2700 MHz

Table 9. AFT20S015N Test Circuit Component Designations and Values — 2300–2700 MHz

Part	Description	Part Number	Manufacturer
C1	4.3 pF Chip Capacitor	ATC600F4R3CT250XT	ATC
C2	1.3 pF Chip Capacitor	ATC800B1R3BT500XT	ATC
C3	8.2 pF Chip Capacitor	ATC600F8R2BT250XT	ATC
C4	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C5, C6	6.8 pF Chip Capacitors	ATC800B6R8CT500XT	ATC
C7, C8, C17	2.2 μF Chip Capacitors	C3225X7R1H225KT	TDK
C9, C10, C18	220 nF Chip Capacitors	C1812C224K5RAC–TU	Kemet
C11, C12, C19	0.1 μF Chip Capacitors	CDR33BX104AKWS	AVX
C13, C14, C21	2.2 μF Chip Capacitors	C1825C225J5RAC–TU	Kemet
C15, C16	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C20	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26–RH	Multicomp
R1, R2	4.75 Ω Chip Resistors	CRCW12064R75FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D48048	MTL

ALTERNATE CHARACTERIZATION — 2300–2700 MHz

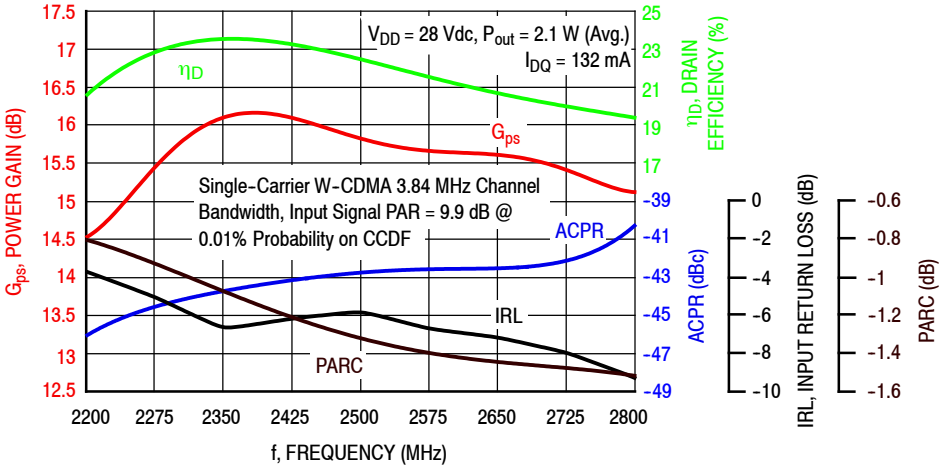


Figure 13. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 2.1 Watts Avg.

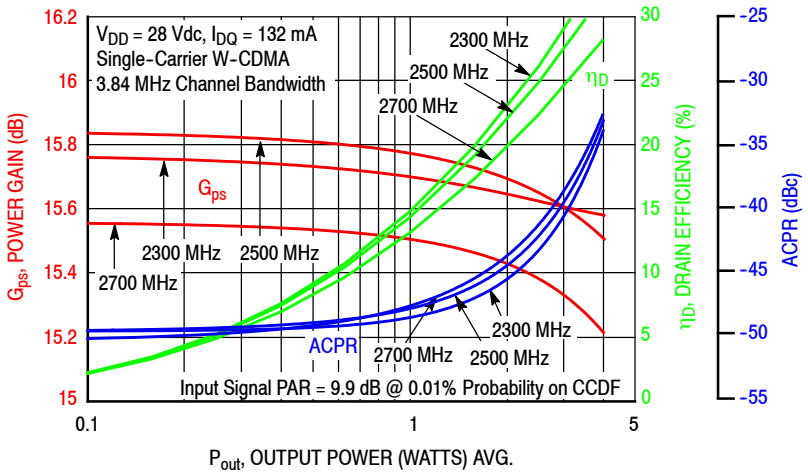


Figure 14. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

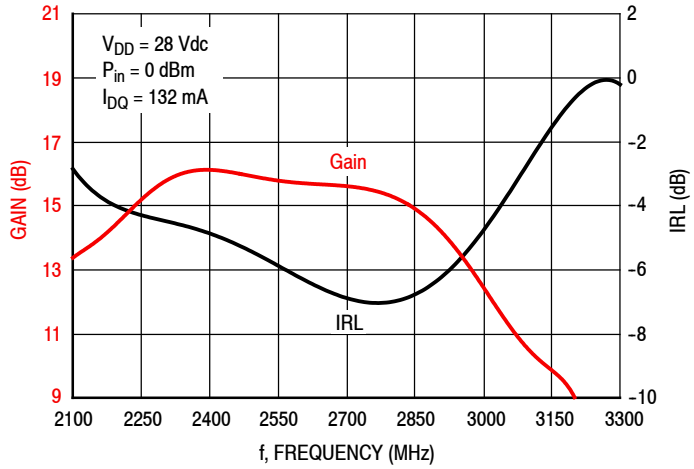
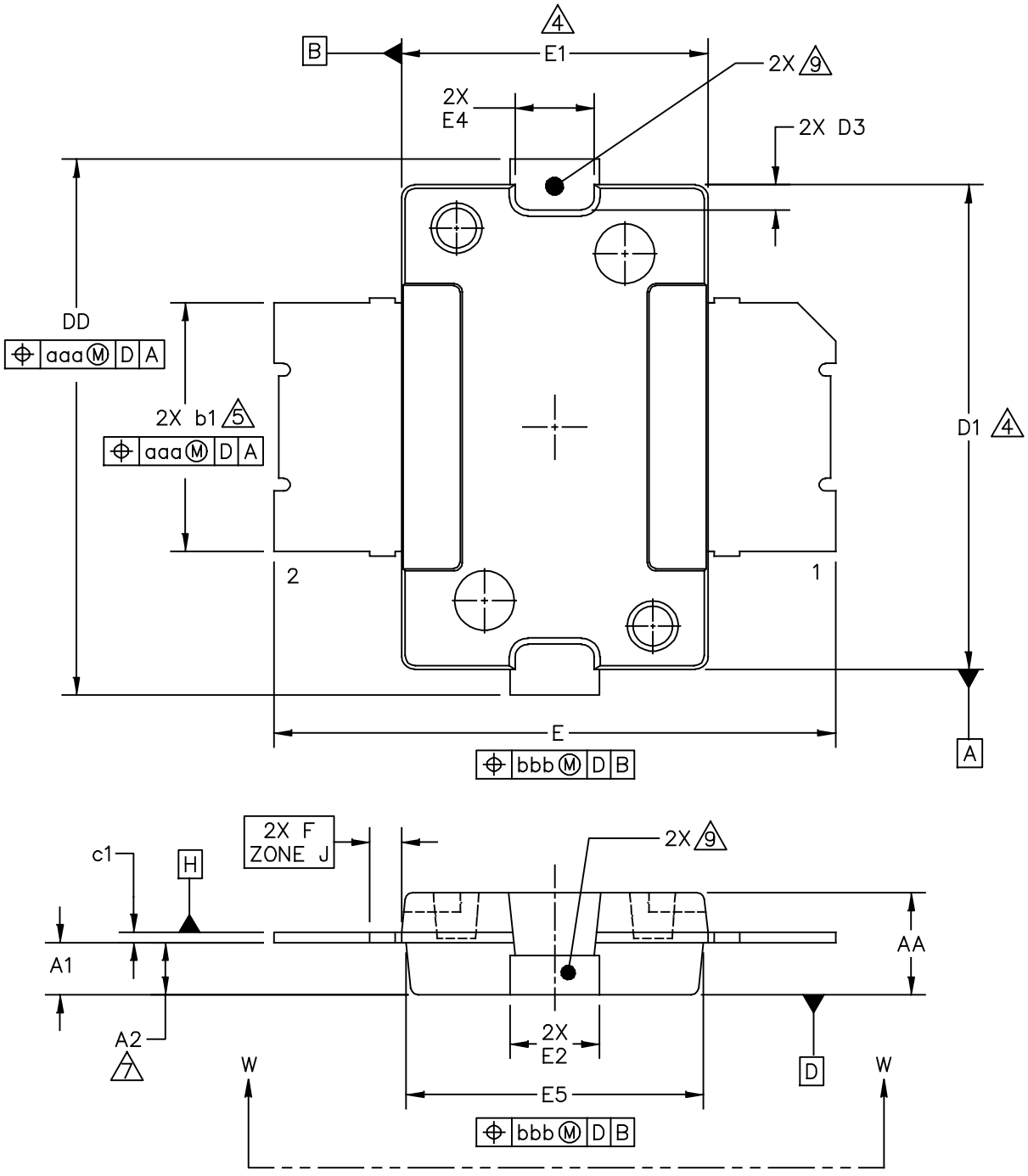


Figure 15. Broadband Frequency Response

PACKAGE INFORMATION



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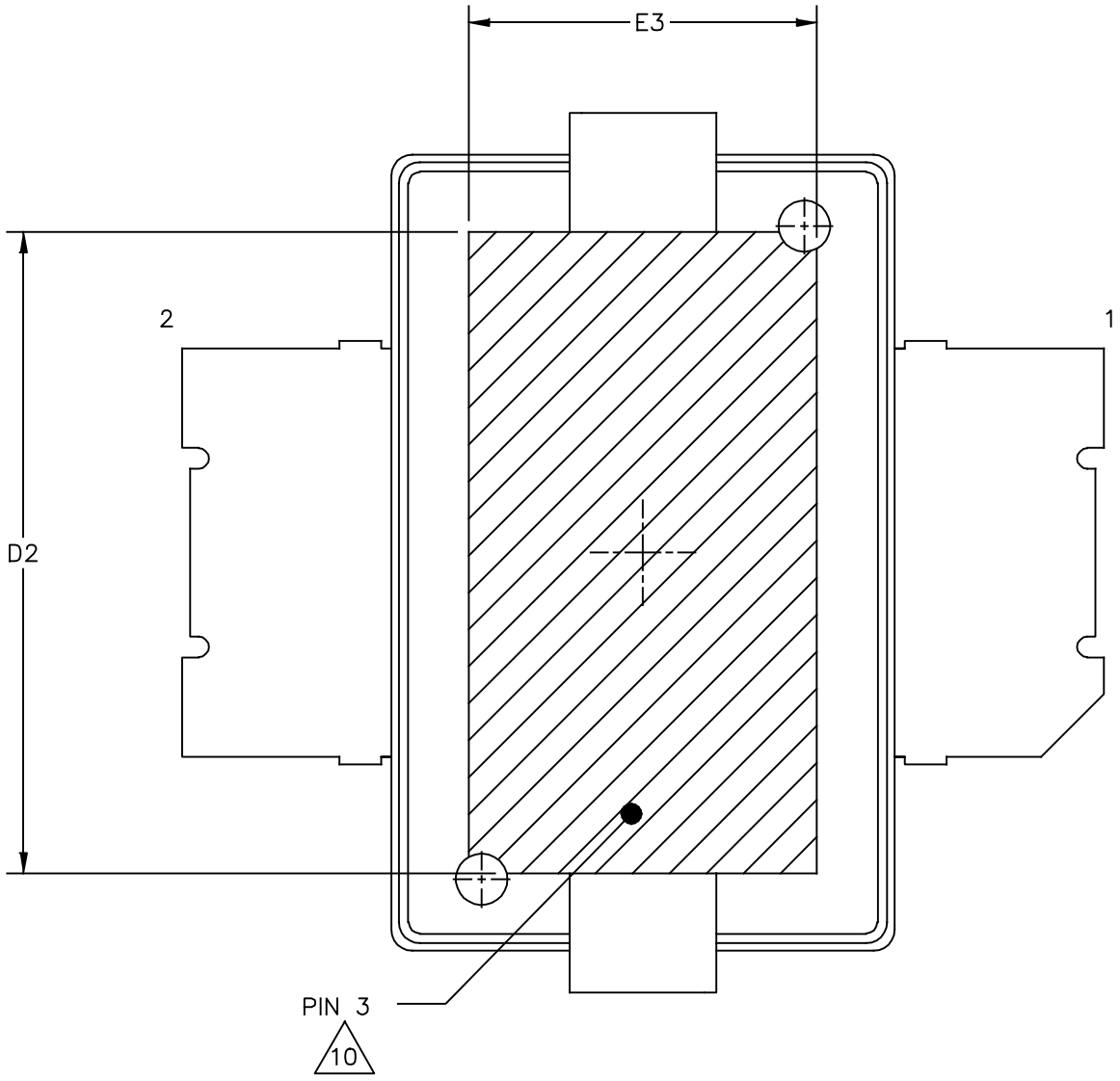

VIEW W–W
BOTTOM VIEW

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	STANDARD: NON–JEDEC	
	SOT1732–1	22 FEB 2016

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.
8. DIMENSIONS DD AND E2 DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH (10.92 MM) FOR DIMENSION DD AND 0.080 INCH (2.03 MM) FOR DIMENSION E2. DIMENSIONS DD AND E2 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE D.
9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.
10. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. DIMENSIONS D2 AND E3 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.078	.082	1.98	2.08	E4	.058	.066	1.47	1.68
A1	.039	.043	0.99	1.09	E5	.231	.235	5.87	5.97
A2	.040	.042	1.02	1.07	F	.025 BSC		0.64 BSC	
DD	.416	.424	10.57	10.77	b1	.193	.199	4.90	5.06
D1	.378	.382	9.60	9.70	c1	.007	.011	0.18	0.28
D2	.290	----	7.37	----	aaa	.004		0.10	
D3	.016	.024	0.41	0.61	bbb	.008		0.20	
E	.436	.444	11.07	11.28					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	----	3.81	----					

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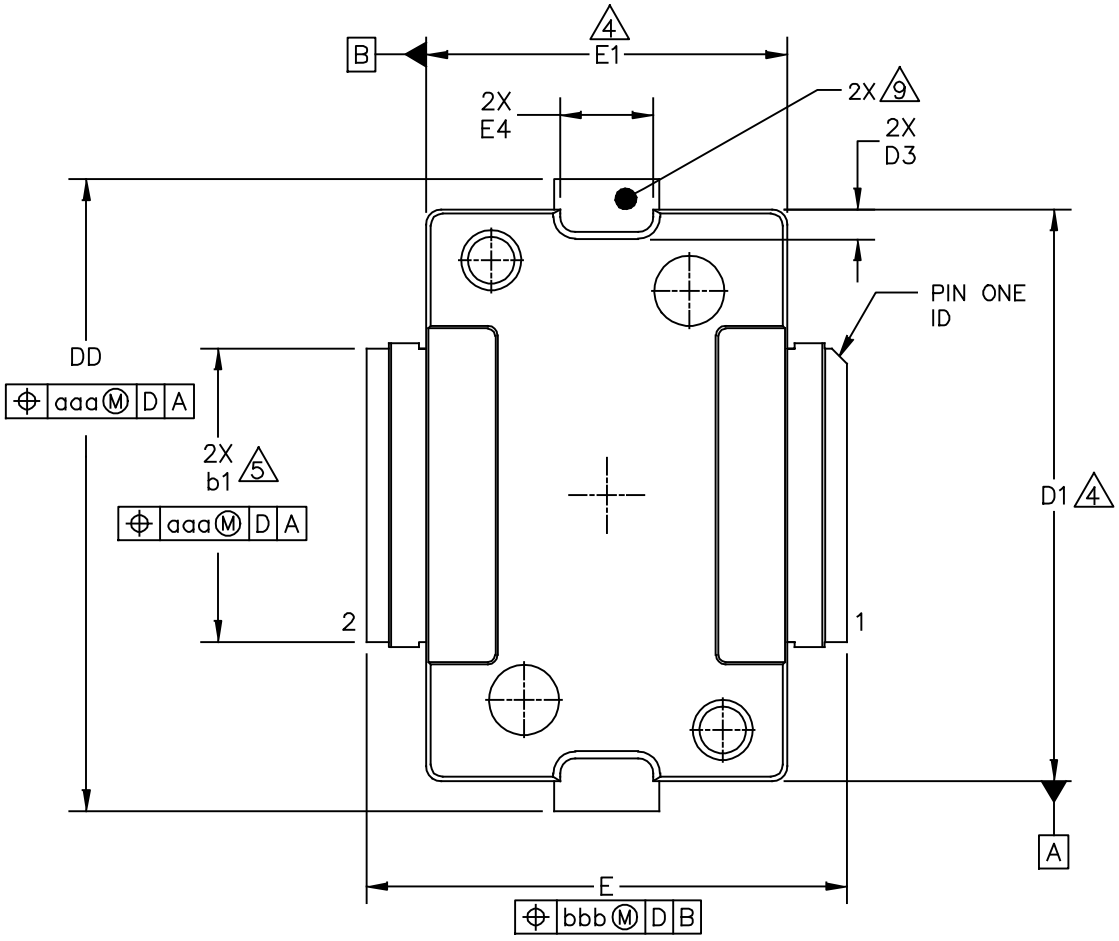

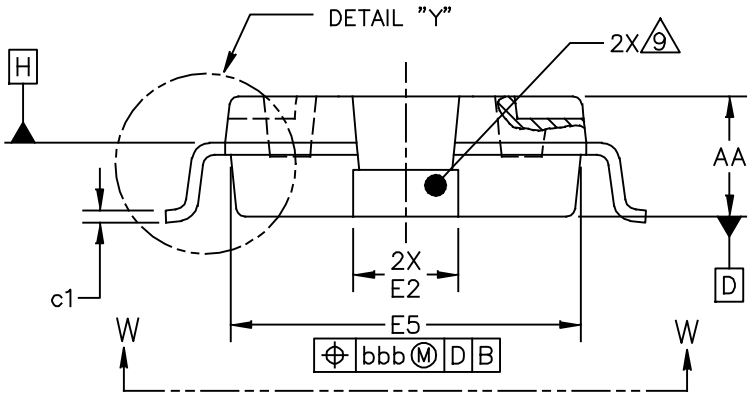

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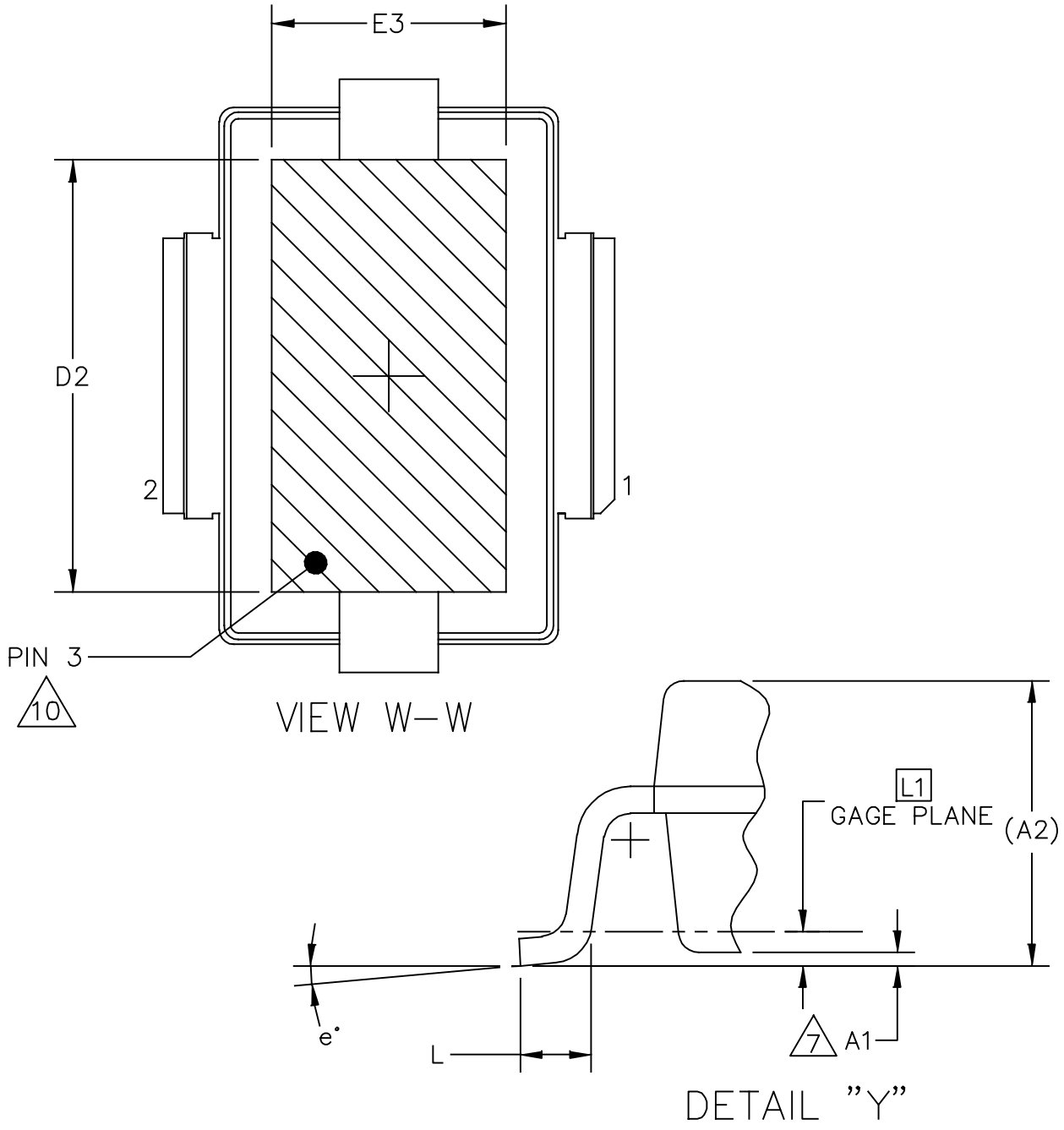
	STANDARD: JEDEC TO−270 BA	
	SOT1731−1	28 MAR 2016



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	SOT1731–1	28 MAR 2016

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15MM) PER SIDE. DIMENSIONS "D1 AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM D. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

8. DIMENSIONS DD AND E2 DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH (10.92 MM) FOR DIMENSION DD AND 0.080 INCH (2.03 MM) FOR DIMENSION E2.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

10. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS D2 AND E3 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.078	.082	1.98	2.08	L	.018	.024	0.46	0.61
A1	.001	.004	0.03	0.10	L1	.010 BSC		0.25 BSC	
A2	(.083)		(2.11)		b1	.193	.199	4.90	5.06
DD	.416	.424	10.57	10.77	c1	.007	.011	0.18	0.28
D1	.378	.382	9.60	9.70	e	2°	8°	2°	8°
D2	.290	–	7.37	–	aaa	.004		0.10	
D3	.016	.024	0.41	0.61	bbb	.008		0.20	
E	.316	.324	8.03	8.23					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	–	3.81	–					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over−Molded Plastic Packages

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2013	• Initial Release of Data Sheet
1	Nov. 2013	• Upper frequency limit changed from 2690 to 2700 MHz to reflect measurement data, p. 1 • Table 2, Thermal Characteristics: changed 2170 to 2140 MHz to reflect recent thermal test results, p. 2 • Table 5, Electrical Characteristics, Load Mismatch: updated VSWR power levels (8 W CW to 14 W CW, 7 W CW to 12 W CW) to reflect recent characterization data test results, p. 3 • Table 5, Electrical Characteristics, Typical Performance: changed P1dB from 7 W to 16.2 W based on P3dB load pull calculations, p. 3 • Figs. 2, 8, 12, Test Circuit Component Layout: added MTL number, pp. 4, 7, 9 • Tables 6, 7, 8, Test Circuit Component Designations and Values: updated PCB description to reflect most current board specifications from Rogers and added MTL part number, pp. 4, 7, 9
2	Apr. 2020	• Package Outline Drawings: TO−270−2 package outline updated to Rev. R, pp. 11−13. TO−270G−2 package outline updated to Rev. D, pp. 14−16. • General updates made to align data sheet to current standard

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