

# TLE7273-2

Low Dropout Voltage Regulator

Automotive Power



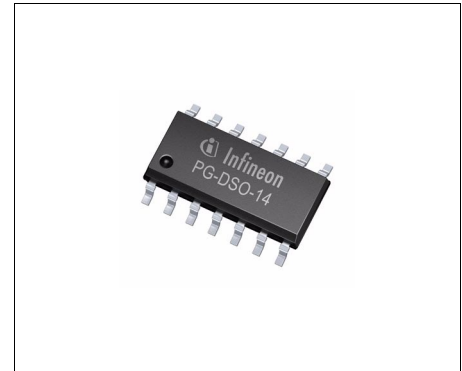
Never stop thinking



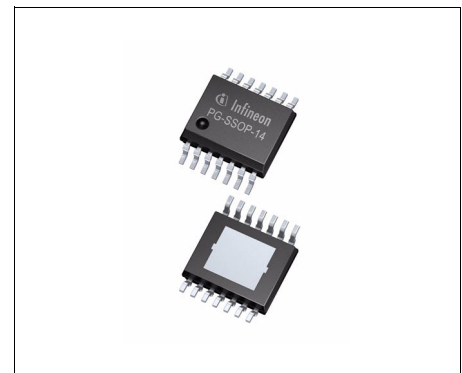
## 1 Overview

### Features

- Output Voltage 5 V, 3.3 V or 2.6 V
- Output Voltage Tolerance  $\pm 2\%$  Up To 180mA
- Ultra Low Quiescent Current Consumption  $< 36 \mu\text{A}$
- Enable Function
- Very Low Dropout Voltage
- Reset With Adjustable Power-On delay
- Window Watchdog With Current Dependent Deactivation
- Output Current Limitation
- Wide Operation Range Up To 45 V
- Wide Temperature Range From  $-40 \text{ }^\circ\text{C}$  To  $150 \text{ }^\circ\text{C}$
- Overtemperature Shutdown
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-14



PG-SSOP-14 Exposed Pad

### Description

The TLE7273-2 is a monolithic voltage regulator with integrated window watchdog and reset dedicated for microcontroller supplies under harsh automotive environment conditions.

Due to its ultra low quiescent current, the TLE7273-2 is perfectly suited for applications that are permanently connected to battery. In addition, the regulator can be shut down via the Enable input causing the current consumption to drop below  $3 \mu\text{A}$ . The TLE7273-2 is equipped with an output current limitation and an overtemperature shutdown, protecting the device against overload, short circuit and over-temperature. It operates in the wide junction temperature range from  $-40 \text{ }^\circ\text{C}$  to  $150 \text{ }^\circ\text{C}$ .

Type	Package	Marking
TLE7273-2GV50	PG-DSO-14	TLE7273-2GV50
TLE7273-2GV33	PG-DSO-14	TLE7273-2GV33
TLE7273-2GV26	PG-DSO-14	TLE7273-2GV26
TLE7273-2EV50	PG-SSOP-14 Exposed Pad	7273 V50

## 2 Block Diagram

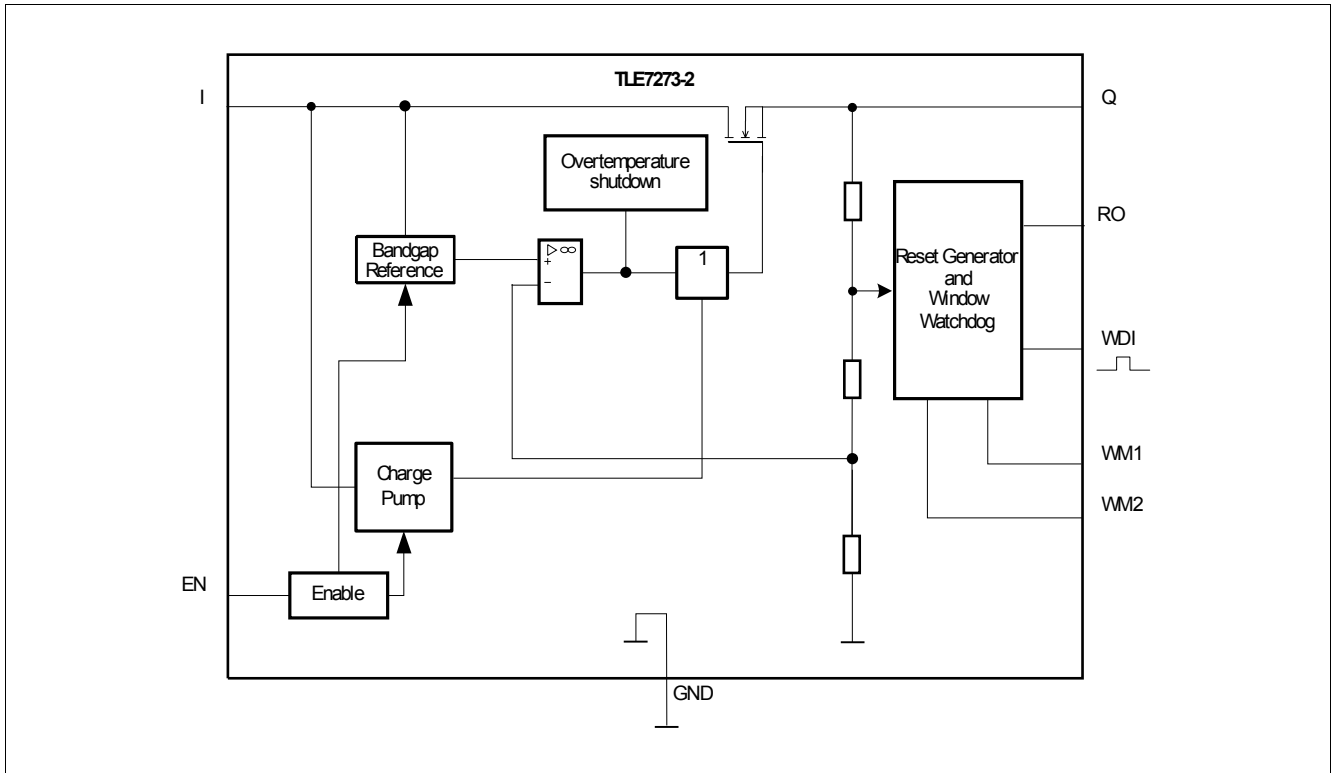


Figure 1 Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment (PG-DSO-14)

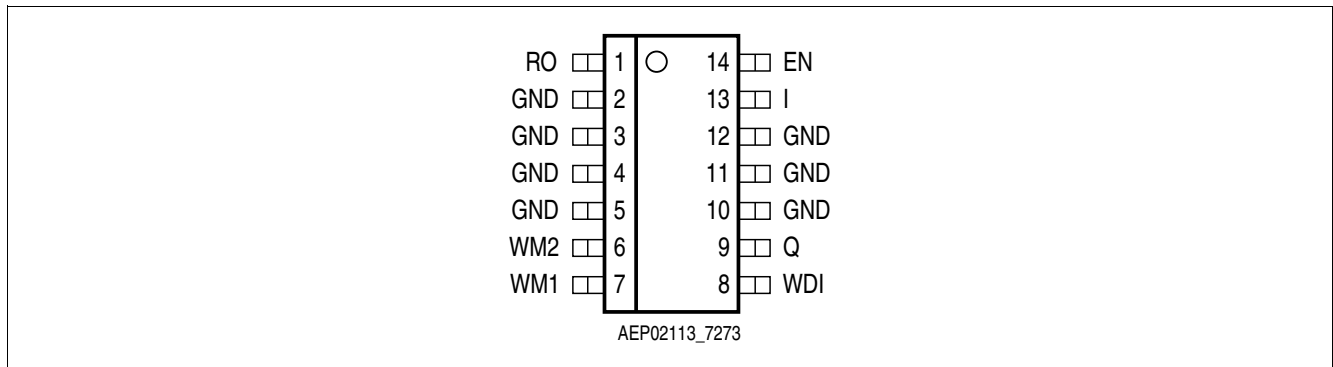


Figure 2 Pin Assignment PG-DSO-14 (top view)

#### 3.2 Pin Definitions and Functions (PG-DSO-14)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	RO	<b>Reset Output</b> TLE7273-2GV33, TLE7273-2GV26: open drain output; TLE7273-2GV50: integrated 20 kΩ pull-up resistor to output Q; leave open if not needed
2-5, 10-12	GND	<b>Ground</b> connect pin 2 and 3 to GND; connect pin 4-5 and 10-12 to heat sink area with GND potential
7	WM1	<b>Watchdog Mode Bit 1</b> watchdog and reset mode selection, see <a href="#">“Window Watchdog State Diagram, Watchdog and Reset Modes” on Page 9</a> ; connect to Q or GND
6	WM2	<b>Watchdog Mode Bit 2</b> watchdog and reset mode selection, see <a href="#">“Window Watchdog State Diagram, Watchdog and Reset Modes” on Page 9</a> ; connect to Q or GND
8	WDI	<b>Watchdog Input</b> trigger input for watchdog pulses; to turn off watchdog connect to GND and connect pin WM1 and WM2 to Q
9	Q	<b>Output Voltage</b> block to GND with a ceramic capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in <a href="#">“Functional Range” on Page 7</a>
13	I	<b>Input Voltage</b> block to ground directly at the IC with a 100 nF ceramic capacitor
14	EN	<b>Enable Input</b> low level disables the IC; integrated pull-down resistor to GND

### 3.3 Pin Assignments (PG-SSOP-14 Exposed Pad)

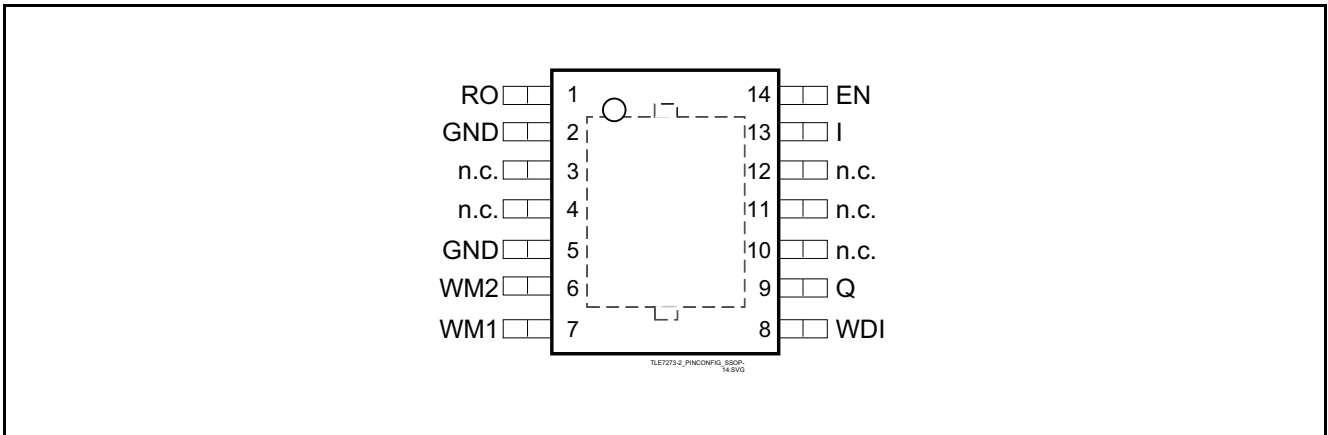


Figure 3 Pin Assignment PG-SSOP-14 Exposed Pad (top view)

### 3.4 Pin Definitions and Functions (PG-SSOP-14 Exposed Pad)

Table 2 Pin Definitions and Functions

Pin No.	Symbol	Function
1	RO	<b>Reset Output</b> integrated 20 kΩ pull-up resistor (TLE7273-2EV50); leave open if not needed
2, 5	GND	<b>Ground</b> connect to GND
3, 4, 10, 11, 12	n.c.	<b>not connected</b> leave open or connect to GND
6	WM2	<b>Watchdog Mode Bit 2</b> watchdog and reset mode selection, see <a href="#">Figure 5</a> ; connect to $V_Q$ or GND
7	WM1	<b>Watchdog Mode Bit 1</b> watchdog and reset mode selection, see <a href="#">Figure 5</a> ; connect to $V_Q$ or GND
8	WDI	<b>Watchdog Input</b> trigger input for watchdog pulses; pull down to GND if not needed and turn off the watchdog with WM1 and WM2 pin
9	Q	<b>Output Voltage</b> block to GND with a ceramic capacitor $C_Q \geq 470$ nF close to IC terminal
13	I	<b>Input Voltage</b> block to ground directly at the IC with a 100 nF ceramic capacitor
14	EN	<b>Enable Input</b> low level disables the IC; integrated pull-down resistor
Pad	–	<b>Exposed Pad</b> connect to heatsink area; connect with GND on PCB

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings<sup>1)</sup>**
 $T_j = -40\text{ °C to }+150\text{ °C}$ 

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
<b>Input I</b>						
4.1.1	Voltage	$V_I$	-0.3	45	V	–
<b>Output Q, Reset Output RO, Watchdog Mode 2</b>						
4.1.2	Voltage	$V_Q$	-0.3	5.5	V	permanent
4.1.3	Voltage	$V_Q$	-0.3	6.2	V	$t < 10\text{ s}^2)$
<b>Enable Input EN</b>						
4.1.4	Voltage	$V_{EN}$	-1	45	V	–
4.1.5	Current	$I_{EN}$	-1	1	mA	–
<b>Watchdog Input WDI</b>						
4.1.6	Voltage	$V_{RO}$	-1	7	V	permanent
<b>Watchdog Mode 1</b>						
4.1.7	Voltage	$V_{WM1}$	-0.3	5.5	V	permanent
4.1.8	Voltage	$V_{WM1}$	-0.3	6.2	V	$t < 10\text{ s}^2)$
4.1.9	Current	$I_{WM1}$	-5	5	mA	–
<b>ESD Susceptibility</b>						
4.1.10	Human Body Model (HBM) <sup>3)</sup>	Voltage	-	3	kV	–
4.1.11	Charged Device Model (CDM) <sup>4)</sup>	Voltage	-	1.5	kV	–
<b>Temperatures</b>						
4.1.12	Junction Temperature	$T_j$	-40	150	°C	–
4.1.13	Storage Temperature	$T_{stg}$	-50	150	°C	–

1) not subject to production test, specified by design

2) exposure to these absolute maximum ratings for extended periods ( $t > 10\text{ s}$ ) may affect device reliability

3) ESD HBM Test according JEDEC JESD22-A114

4) ESD CDM Test according AEC/ESDA ESD-STM5.3.1-1999

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
4.2.1	Input Voltage	$V_I$	5.5	45	V	TLE7273-2GV50, TLE7273-2EV50
4.2.2			4.2	45	V	TLE7273-2GV33
4.2.3			4.5	45	V	TLE7273-2GV26
4.2.4	Output Capacitor's Requirements for	$C_Q$	470	–	nF	– <sup>1)</sup>
4.2.5	Stability	$ESR(C_Q)$	–	3	$\Omega$	– <sup>2)</sup>

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at  $f = 10$  kHz

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistances

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
<b>Package PG-DSO-14</b>							
4.3.1	Junction to Soldering Point <sup>1)</sup>	$R_{thJSP}$	–	30	–	K/W	measured to group of pins 3, 4, 5, 10, 11, 12
4.3.2	Junction to Ambient <sup>1)</sup>	$R_{thJA}$	–	53	–	K/W	<sup>2)</sup>
4.3.3			–	105	–	K/W	footprint only <sup>3)</sup>
4.3.4			–	74	–	K/W	300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>
4.3.5			–	65	–	K/W	600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>
<b>Package PG-SSOP-14 Exposed Pad</b>							
4.3.6	Junction to Case <sup>1)</sup>	$R_{thJSP}$	–	14	–	K/W	measured to exposed pad
4.3.7	Junction to Ambient <sup>1)</sup>	$R_{thJA}$	–	47	–	K/W	<sup>2)</sup>
4.3.8			–	141	–	K/W	footprint only <sup>3)</sup>
4.3.9			–	66	–	K/W	300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>
4.3.10			–	56	–	K/W	600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>

1) not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70 $\mu$ m Cu, 2 x 35 $\mu$ m Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 1 copper layer (1 x 70 $\mu$ m Cu).

## 5 Block Description and Electrical Characteristics

### 5.1 Description

#### 5.1.1 Power On Reset and Reset Output

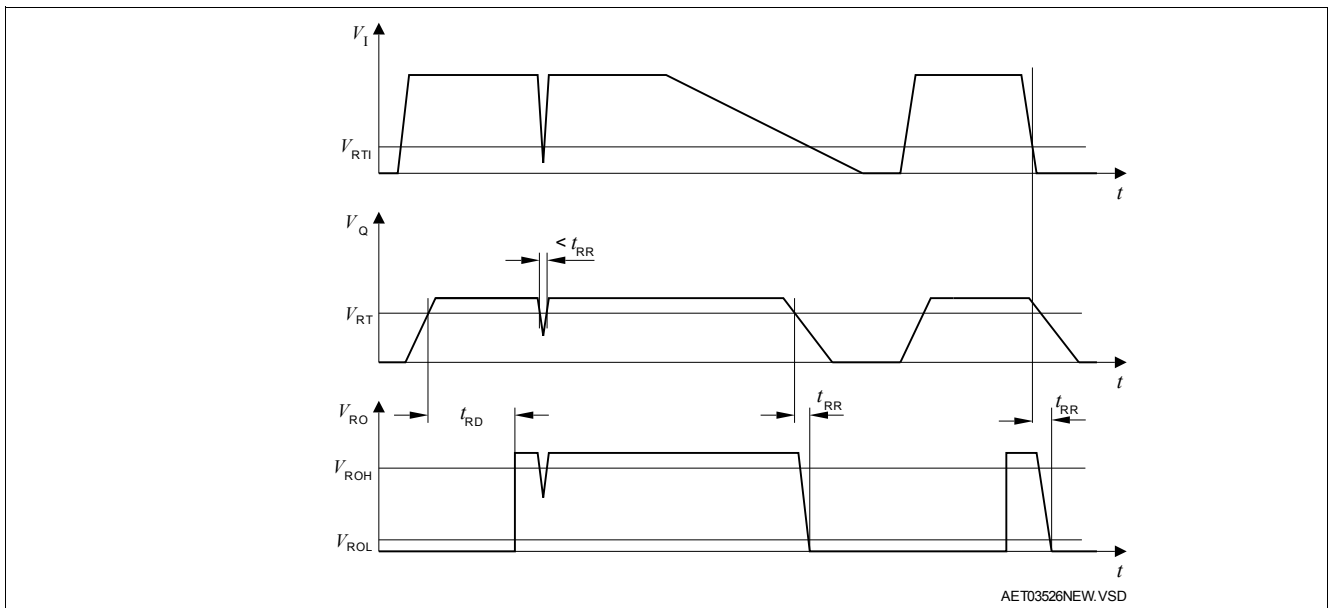
For an output voltage level of  $V_Q \geq 1\text{ V}$ , the reset output is held low. When the level of  $V_Q$  reaches the reset threshold  $V_{RT}$ , the signal at RO remains low for the power-up reset delay time  $t_{RD}$ . The reset function and timing is illustrated in **Figure 4**. The reset reaction time  $t_{RR}$  avoids wrong triggering caused by short “glitches” on the  $V_Q$ -line. In case of  $V_Q$  power down ( $V_Q < V_{RT}$  for  $t > t_{RR}$ ) a logic low signal is generated at the pin RO to reset an external microcontroller.

The TLE7273-2GV50 and TLE7273-2EV50 feature an integrated pull-up resistor on the reset output while the TLE7273-2GV33 and TLE7273-2GV26 have an open drain output requiring an external pull-up resistor. When connected to a voltage level of 5 V, a recommended value for this external resistor is  $\geq 5.6\text{ k}\Omega$ .

But it's also possible calculating its value by using the following formula, based on the reset sink current (Example: external pull-up resistor connected to  $V_{ext} = 5\text{ V}$ ):

$$R_{\text{extmin}} = \Delta V / I_{RO} = (V_{\text{ext}} - V_{RO\text{min}}) / I_{RO} = (5\text{ V} - 0.25\text{ V}) / 1.0\text{ mA} = 4.75\text{ k}\Omega$$

At low output voltage levels  $V_Q < 1\text{ V}$  the integrated pull-up resistor of the TLE7273-2GV50 is switched off setting the reset output high ohmic.



**Figure 4** Reset Function and Timing Diagram

#### 5.1.2 Watchdog Operation

The watchdog uses a fraction of the charge pump oscillator's clock signal as timebase. The watchdog timebase can be adjusted using the pins WM1 and WM2 (see **Figure 5**). The watchdog can be turned off setting WM1 and WM2 to high level. The timing values refer to typ. values with WM1 and WM2 connected to GND (fast watchdog and reset timing).

**Figure 5** shows the state diagram of the window watchdog (WWD) and the watchdog and reset mode selection. After power-on, the reset output signal at the RO pin (microcontroller reset) is kept LOW for the reset delay time  $t_{RD}$  of typ. 16 ms. With the LOW to HIGH transition of the signal at RO the device starts the ignore window time  $t_{CW}$  (32 ms). During this window the signal at the WDI pin is ignored. Next the WWD starts the open window which



**Block Description and Electrical Characteristics**

is in the very first turn after power up a long open window with  $t_{max} = 4 * t_{OW}$ . In the following turns, the timing corresponds to the standard timing setting as described in the specification.

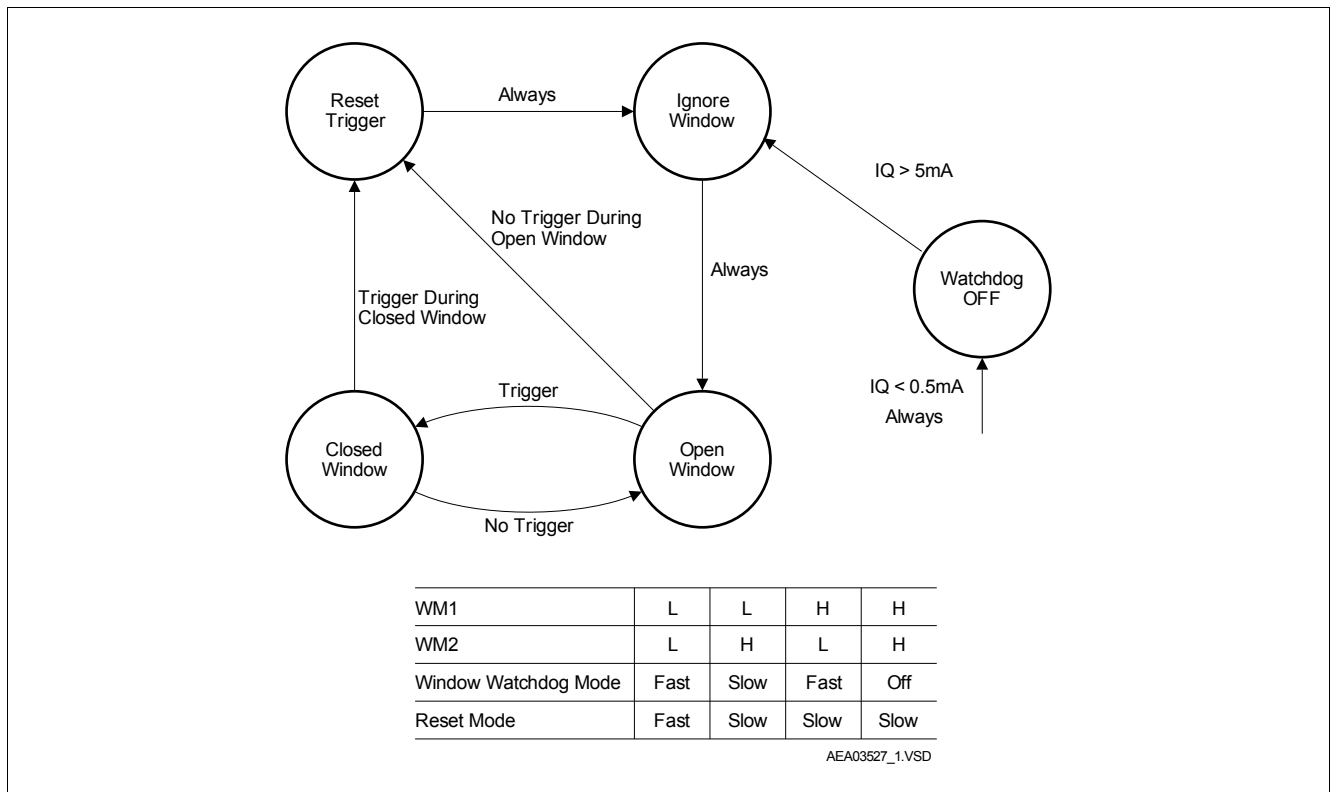
When a valid trigger signal is detected during the open window a closed window is initialized immediately. A trigger signal within the closed window is interpreted as a pretrigger failure and results in a reset. After the closed window the open window with the duration  $t_{OW}$  is started again. The open window lasts at minimum until the trigger process has occurred, at maximum  $t_{OW}$  is 32 ms (typ. value with fast timing).

A HIGH to LOW transition of the watchdog trigger signal at pin WDI is considered as a valid trigger pulse.

See **Figure 7**: To avoid wrong triggering due to parasitic glitches two HIGH samples followed by two LOW samples (sample period  $t_{sam}$  typ. 0.5 ms) are decoded as a valid trigger .

A reset is generated (RO goes LOW) if there is no trigger pulse during the open window or if a pretrigger occurs during the closed window. The triggering is correct also, if the first three samples (two HIGH one LOW) of the trigger pulse at pin WDI are inside the closed window and only the fourth sample (the second LOW sample) is taken in the open window.

After turning OFF the Watchdog by output current reduction, RO remains high. (see also the signal diagram in **Figure 6**). After turning ON the WWD again by exceeding the current threshold, the logic cycle starts again with the Ignore Window and goes then into the "1st. long open window". This 1st long OW is maximum  $4 * t_{OW}$  long and allows the re-synchronisation between the micro controller and the WWD timing. The 1st. long OW is closed by the first valid trigger on WDI from the micro controller. This trigger ensures the synchronisation. As soon as this trigger is done, the micro controller timing must be stable and correspondent to  $t_{WD}$ .



**Figure 5 Window Watchdog State Diagram, Watchdog and Reset Modes**

Block Description and Electrical Characteristics

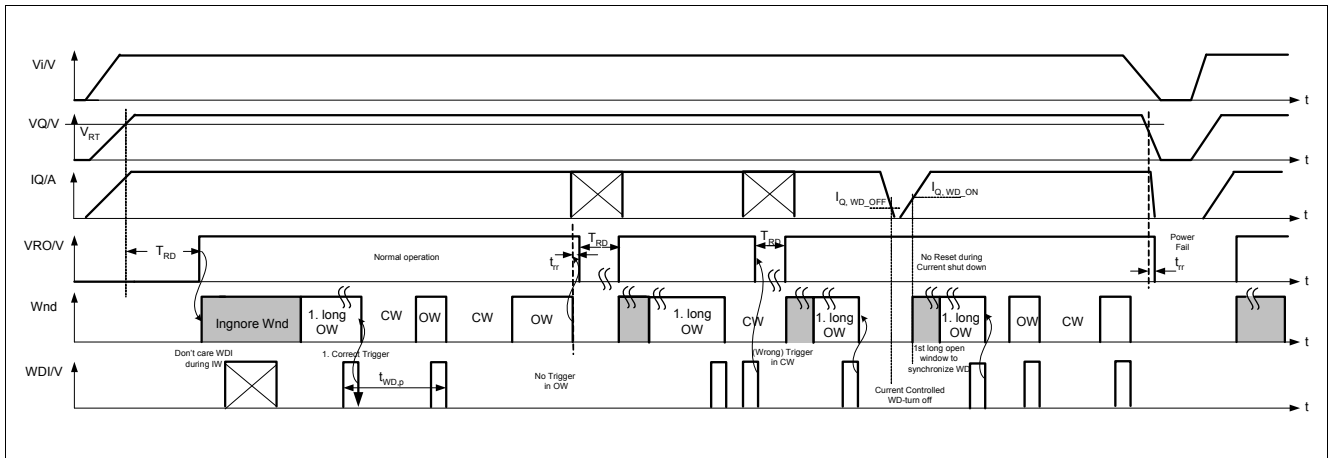


Figure 6 Window Watchdog Signal Diagram

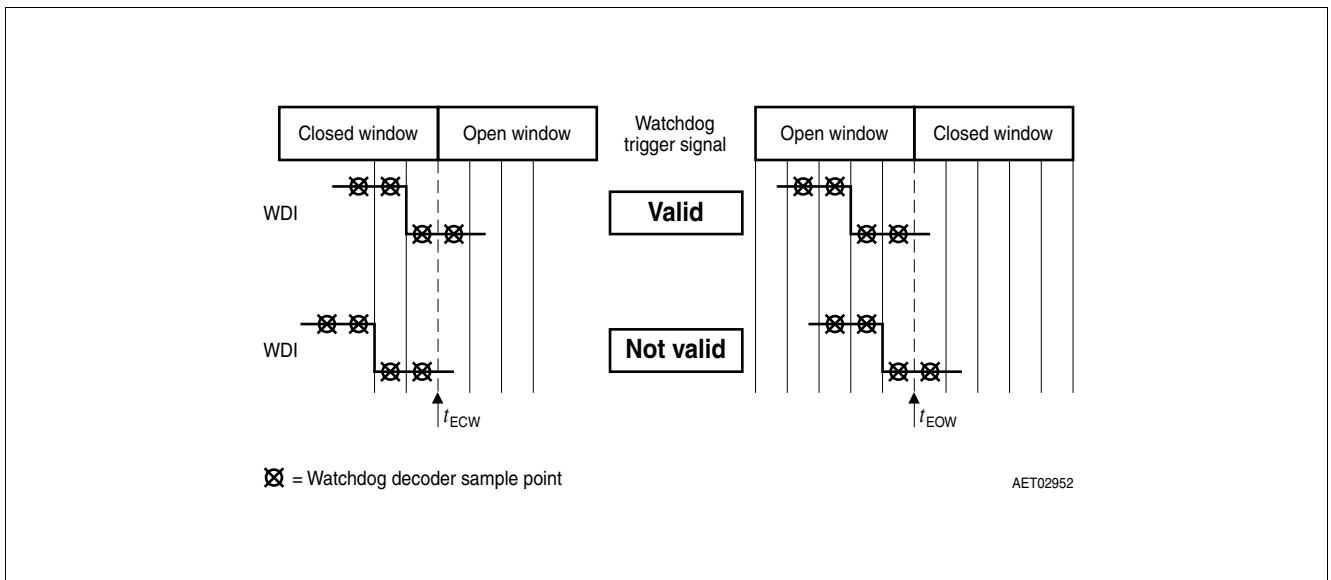


Figure 7 Window Watchdog Definitions

## 5.2 Electrical Characteristics

### Electrical Characteristics

$V_I = 13.5 \text{ V}$ ;  $T_j = -40 \text{ }^\circ\text{C}$  to  $+150 \text{ }^\circ\text{C}$ ; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
<b>Output Q</b>							
5.2.1	Output Voltage	$V_Q$	4.90	5.00	5.10	V	TLE7273-2GV50, TLE7273-2EV50 $1 \text{ mA} < I_Q < 180 \text{ mA}$ $6 \text{ V} < V_I < 16 \text{ V}$
5.2.2	Output Voltage	$V_Q$	4.90	5.00	5.10	V	TLE7273-2GV50, TLE7273-2EV50 $I_Q = 10 \text{ mA}$ $6 \text{ V} < V_I < 45 \text{ V}$
5.2.3	Output Voltage	$V_Q$	3.234	3.30	3.366	V	TLE7273-2GV33 $1 \text{ mA} < I_Q < 180 \text{ mA}$ $4.5 \text{ V} < V_I < 16 \text{ V}$
5.2.4	Output Voltage	$V_Q$	3.234	3.30	3.366	V	TLE7273-2GV33 $I_Q = 10 \text{ mA}$ $4.5 \text{ V} < V_I < 45 \text{ V}$
5.2.5	Output Voltage	$V_Q$	2.548	2.60	2.652	V	TLE7273-2GV26 $1 \text{ mA} < I_Q < 180 \text{ mA}$ $4.5 \text{ V} < V_I < 16 \text{ V}$
5.2.6	Output Voltage	$V_Q$	2.548	2.60	2.652	V	TLE7273-2GV26 $I_Q = 10 \text{ mA}$ $4.5 \text{ V} < V_I < 45 \text{ V}$
5.2.7	Output Current Limitation	$I_Q$	200	–	500	mA	$V_Q = 2.0 \text{ V}$
5.2.8			200	–	600		$V_Q = 0 \text{ V}$
5.2.9	Dropout Voltage <sup>1)</sup> $V_{DR} = V_I - V_Q$	$V_{DR}$	–	250	500	mV	$I_Q = 180 \text{ mA}$ TLE7273-2GV50, TLE7273-2EV50
5.2.10	Load Regulation	$\Delta V_{Q,Lo}$	–	50	90	mV	$1 \text{ mA} < I_Q < 180 \text{ mA}$ ;
5.2.11	Line Regulation	$\Delta V_{Q,Li}$	–	10	50	mV	$I_Q = 1 \text{ mA}$ ; $10 \text{ V} < V_I < 32 \text{ V}$
5.2.12	Power Supply Ripple Rejection	$PSRR$	–	60	–	dB	$f_r = 100 \text{ Hz}$ ; $V_r = 0.5 V_{PP}$
5.2.13	Reverse Output Current Clamping	$V_Q$	–	–	5.5	V	$I_Q = -1 \text{ mA}$ , $V_{EN} = 0 \text{ V}$
<b>Current Consumption</b>							
5.2.14	Quiescent Current $I_q = I_I - I_Q$	$I_q$	–	28	36	$\mu\text{A}$	$I_Q = 100 \mu\text{A}$ ; $T_j < 80^\circ\text{C}$
5.2.15	Quiescent Current Disabled	$I_q$	–	1	3	$\mu\text{A}$	$V_{EN} = 0\text{V}$ ; $T_j < 80^\circ\text{C}$
<b>Enable Input EN</b>							
5.2.16	High Level Input Voltage	$V_{EN,H}$	3.0	–	–	V	$V_Q$ on

**Block Description and Electrical Characteristics**
**Electrical Characteristics**
 $V_I = 13.5 \text{ V}$ ;  $T_j = -40 \text{ °C}$  to  $+150 \text{ °C}$ ; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.2.17	Low Level Input Voltage	$V_{EN,L}$	–	–	0.5	V	$V_Q = 0.02 \text{ V}$ ; $I_Q = 5 \text{ mA}$ ; $T_j < 125 \text{ °C}$
5.2.18			–	–	0.3	V	
5.2.19	High Level Input Current	$I_{EN,H}$	–	3	4	$\mu\text{A}$	$V_{EN} = 5 \text{ V}$

**Watchdog Mode Bit 1**

5.2.20	High Level Input Voltage	$V_{WM1,H}$	4.00	–	–	V	TLE7273-2GV50, TLE7273-2EV50
5.2.21			2.65	–	–	V	TLE7273-2GV33
5.2.22			2.30	–	–	V	TLE7273-2GV26
5.2.23	Low Level Input Voltage	$V_{WM1,L}$	–	–	0.80	V	

**Watchdog Mode Bit 2**

5.2.24	High Level Input Voltage	$V_{WM2,H}$	4.00	–	–	V	TLE7273-2GV50, TLE7273-2EV50
5.2.25			2.65	–	–	V	TLE7273-2GV33
5.2.26			2.30	–	–	V	TLE7273-2GV26
5.2.27	Low Level Input Voltage	$V_{WM2,L}$	–	–	0.80	V	

**Watchdog Input WDI**

5.2.28	High Level Input Voltage	$V_{WDI,H}$	4.00	–	–	V	TLE7273-2GV50, TLE7273-2EV50
5.2.29			2.65	–	–	V	TLE7273-2GV33
5.2.30			2.30	–	–	V	TLE7273-2GV26
5.2.31	Low Level Input Voltage	$V_{WDI,L}$	–	–	0.80	V	
5.2.32	High Level Input Current	$I_{WDI,H}$	–	3	4	$\mu\text{A}$	$V_{WDI} = 5 \text{ V}$
5.2.33	Low Level Input Current	$I_{WD,IL}$	–	0.5	1	$\mu\text{A}$	$V_{WDI} = 0 \text{ V}$ $T_j < 80 \text{ °C}$
5.2.34	Watchdog Sampling Time	$t_{sam}$	0.40	0.50	0.60	ms	Fast Watchdog Timing
5.2.35			0.80	1.00	1.20	ms	Slow Watchdog Timing
5.2.36	Ignore Window Time	$t_{IW}$	25.6	32.0	38.4	ms	Fast Watchdog Timing
5.2.37			51.2	64.0	76.8	ms	Slow Watchdog Timing
5.2.38	Open Window Time	$t_{OW}$	25.6	32.0	38.4	ms	Fast Watchdog Timing
5.2.39			51.2	64.0	76.8	ms	Slow Watchdog Timing
5.2.40	Closed Window Time	$t_{CW}$	25.6	32.0	38.4	ms	Fast Watchdog Timing
5.2.41			51.2	64.0	76.8	ms	Slow Watchdog Timing
5.2.42	Window Watchdog Trigger Time <sup>2)</sup>	$t_{WD}$	–	48	–	ms	Fast Watchdog Timing
5.2.43			–	96	–	ms	Slow Watchdog Timing

**Block Description and Electrical Characteristics**
**Electrical Characteristics**
 $V_I = 13.5\text{ V}$ ;  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.2.44	Watchdog Deactivation Current Threshold	$I_{Q,WD\_off}$	0.50	–	–	mA	$I_Q$ decreasing $V_I > 5.5\text{ V}$ for TLE7273-2GV50, TLE7273-2EV50  $V_I > 4.5\text{ V}$ for TLE7273- 2GV33, TLE7273-2GV26
5.2.45	Watchdog Activating Current Threshold	$I_{Q,WD\_on}$	–	–	5	mA	$I_Q$ increasing $V_I > 5.5\text{ V}$ for TLE7273-2GV50, TLE7273-2EV50  $V_I > 4.5\text{ V}$ for TLE7273- 2GV33, TLE7273-2GV26

**Reset Output RO**

5.2.46	Output Undervoltage Reset Switching Threshold	$V_{RT}$	4.50	4.60	4.70	V	TLE7273-2GV50, TLE7273-2EV50 $V_Q$ decreasing
5.2.47			3.00	3.07	3.13	V	TLE7273-2GV33 <sup>3)</sup> $V_I > 4.5\text{ V}$ ; $V_Q$ decreasing
5.2.48			2.35	2.38	2.45	V	TLE7273-2GV26 <sup>3)</sup> $V_I > 4.5\text{ V}$ ; $V_Q$ decreasing
5.2.49	Input Undervoltage Reset Switching Threshold	$V_{RTI}$	–	3.9	4.0	V	TLE7273-2GV26 <sup>3)</sup> TLE7273-2GV33 <sup>3)</sup> $V_Q > V_{RT}$ ; $V_I$ decreasing
5.2.50							
5.2.51							
5.2.52	Output Undervoltage Reset Hysteresis	$V_{RH}$	–	45	–	mV	TLE7273-2GV26
5.2.53	Output Undervoltage Reset Hysteresis	$V_{RH}$	–	60	–	mV	TLE7273-2GV33
5.2.54			–	90	–	mV	TLE7273-2GV50, TLE7273-2EV50
5.2.55	Maximum Reset Sink Current	$I_{RO,max}$	1.75	–	–	mA	TLE7273-2GV50, TLE7273-2EV50 $V_Q = 4.5\text{ V}$ ; $V_{RO} = 0.25\text{ V}$
5.2.56			1.3	–	–	mA	TLE7273-2GV33 $V_Q = 3.0\text{ V}$ ; $V_{RO} = 0.25\text{ V}$
5.2.57			1.0	–	–	mA	TLE7273-2GV26 $V_Q = 2.35\text{ V}$ ; $V_{RO} = 0.25\text{ V}$

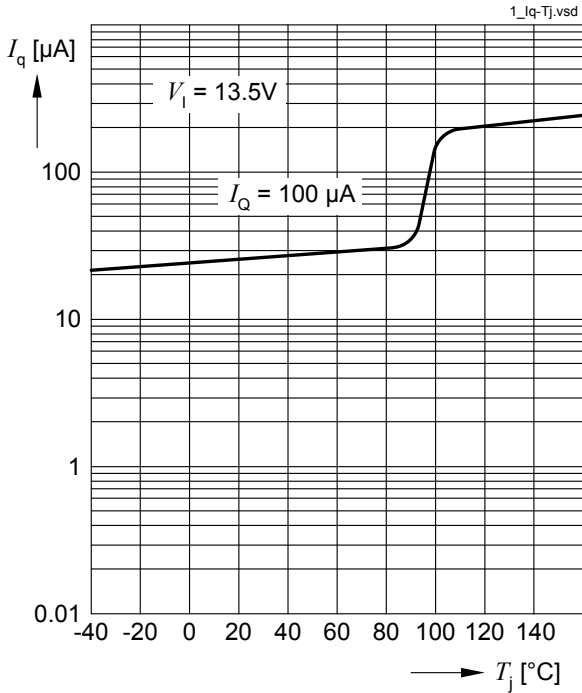
**Block Description and Electrical Characteristics**
**Electrical Characteristics**
 $V_I = 13.5 \text{ V}$ ;  $T_j = -40 \text{ }^\circ\text{C}$  to  $+150 \text{ }^\circ\text{C}$ ; unless otherwise specified

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.2.58	Reset Output Low Level Voltage	$V_{ROL}$	–	0.15	0.25	V	$V_Q \geq 1 \text{ V}$ ; $I_{RO} < 200 \text{ } \mu\text{A}$
5.2.59	Reset Output High Level Voltage	$V_{ROH}$	4.5	–	–	V	TLE7273-2GV50, TLE7273-2EV50
5.2.60	Reset High Level Leakage Current	$I_{ROLK}$	–	–	1	$\mu\text{A}$	TLE7273-2GV33 TLE7273-2GV26
5.2.61	Integrated Reset Pull Up Resistor	$R_{RO}$	10	20	40	k $\Omega$	TLE7273-2GV50, TLE7273-2EV50 internally connected to $V_Q$
5.2.62	Power-On Reset Delay Time	$t_{RD}$	12.8	16.0	19.2	ms	Fast Reset Timing
5.2.63			25.6	32.0	38.4	ms	Slow Reset Timing
5.2.64	Reset Reaction Time	$t_{RR}$	–	4	12	$\mu\text{s}$	

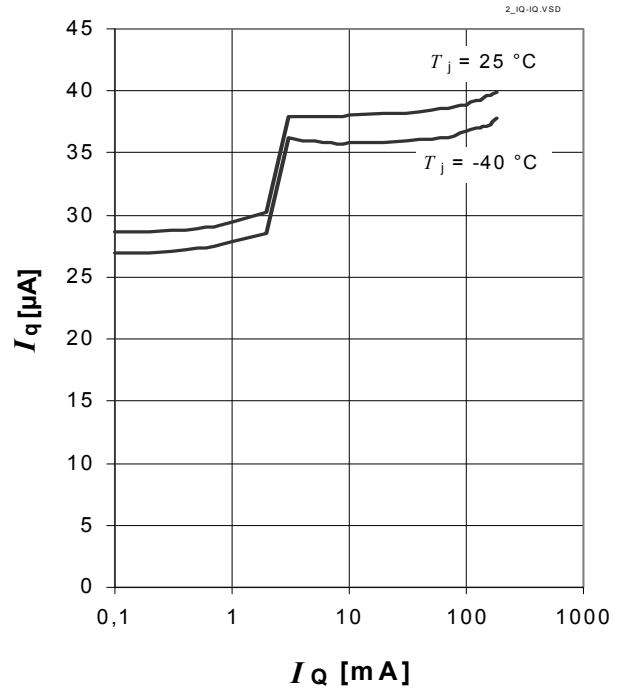
- 1) measured when the output voltage has dropped 100 mV from the nominal value obtained at  $V_I = 13.5 \text{ V}$
- 2) recommendation for typical trigger time;  $t_{WD} = t_{CW} + 1/2 * t_{OW}$
- 3) reset output triggered when output voltage  $V_Q$  is lower than output voltage reset switching threshold  $V_{RT}$  or is also triggered, when input voltage is decreasing to  $V_I < 4.0 \text{ V}$  and  $V_Q > V_{RT}$

Typical Performance Characteristics

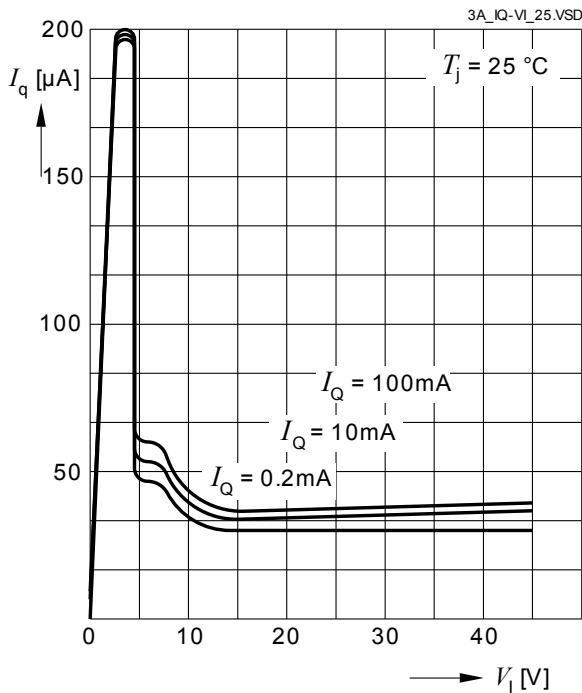
Current Consumption  $I_q$  versus Junction Temperature  $T_j$  (EN=ON)



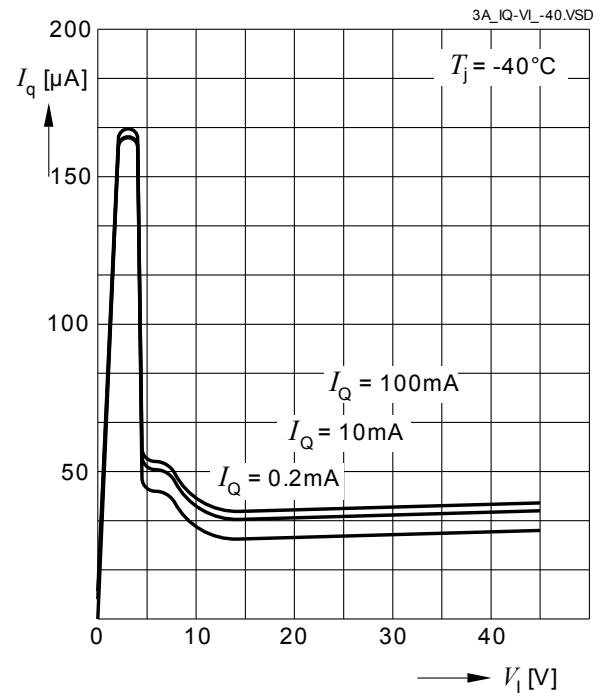
Current Consumption  $I_q$  versus Output Current  $I_Q$  (EN=ON)



Current Consumption  $I_q$  versus Input Voltage  $V_i$  at  $T_j=25^\circ\text{C}$  (EN=ON)

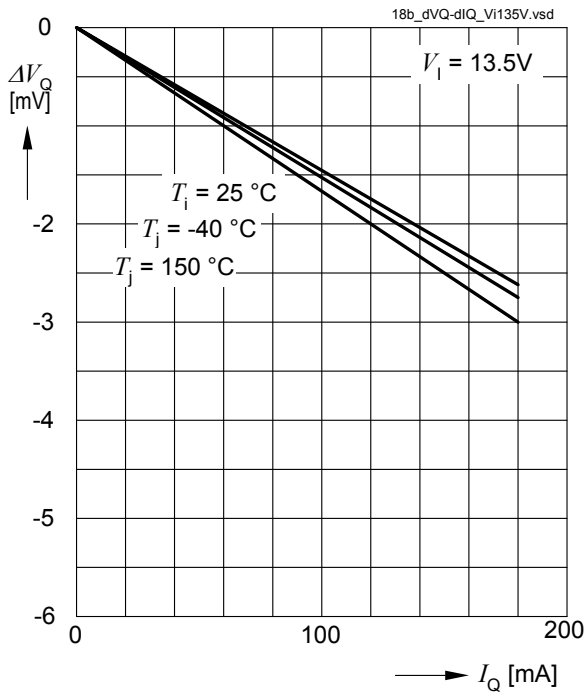


Current Consumption  $I_q$  versus Input Voltage  $V_i$  at  $T_j=-40^\circ\text{C}$  (EN=ON)

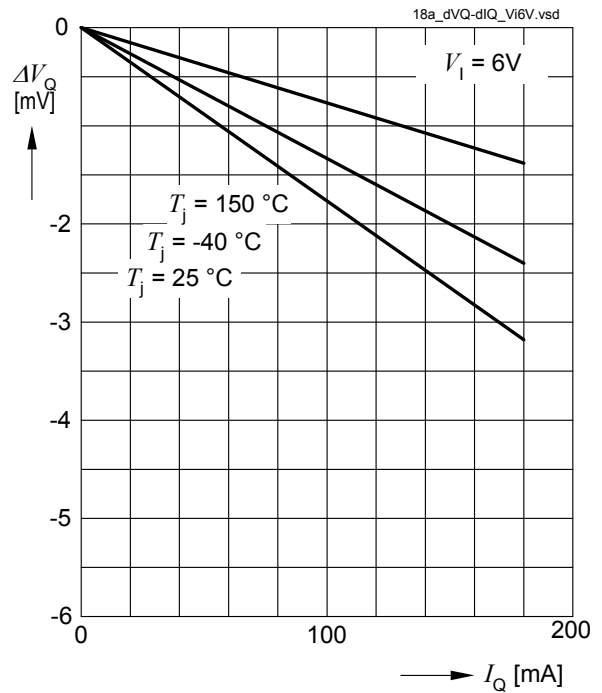


Typical Performance Characteristics (cont'd)

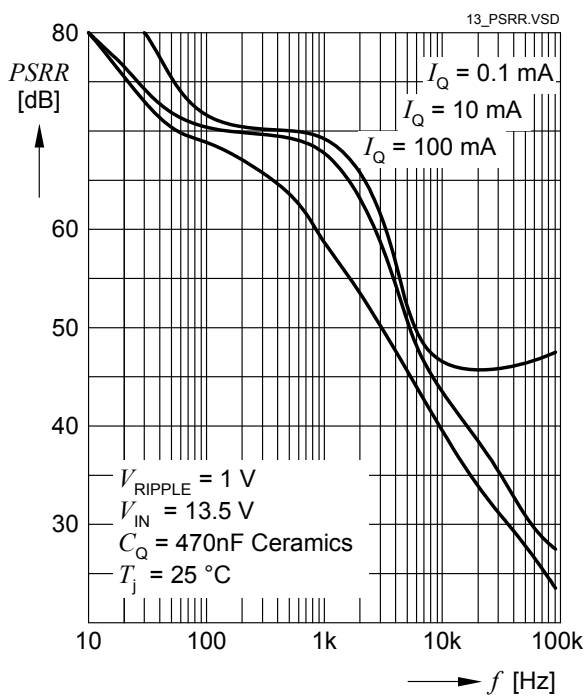
Load Regulation  $dV_Q$  versus Output Current Change  $dI_Q$



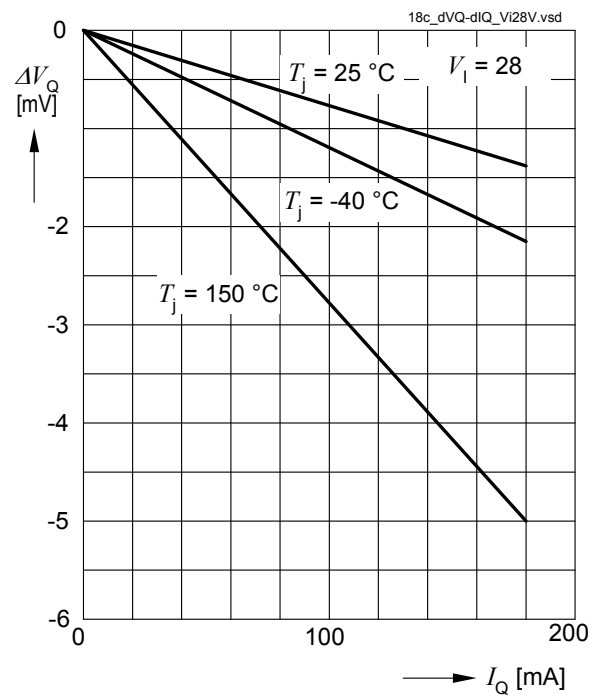
Load Regulation  $dV_Q$  versus Output Current Change  $dI_Q$



Power Supply Ripple Rejection *PSRR*



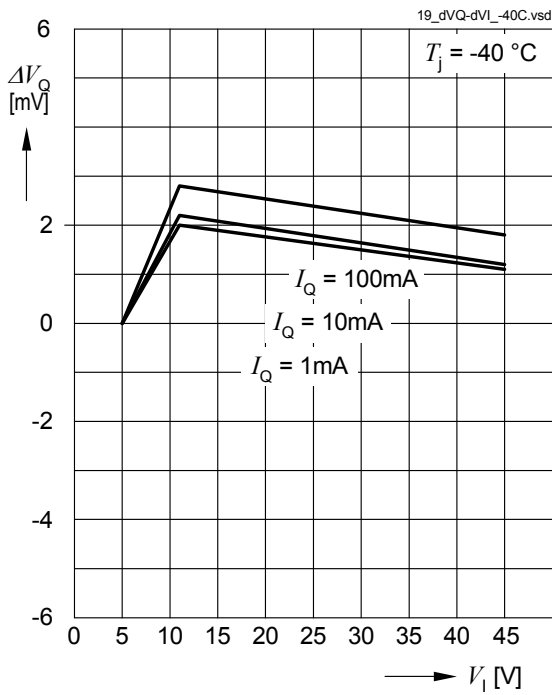
Load Regulation  $dV_Q$  versus Output Current Change  $dI_Q$



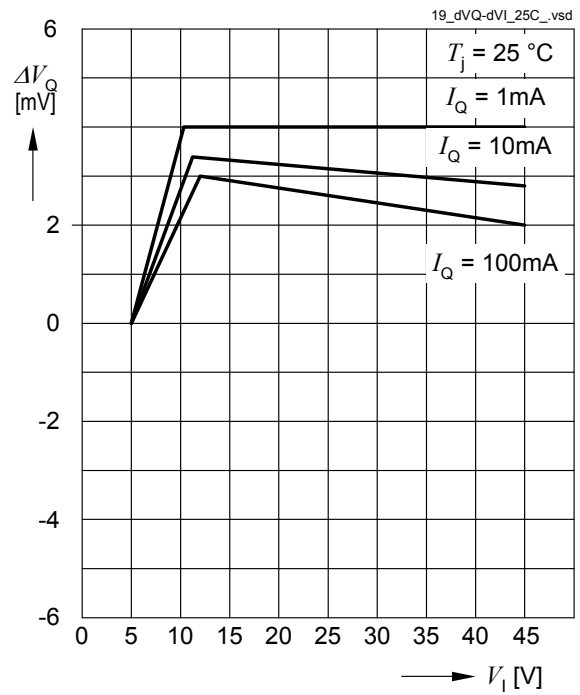


Typical Performance Characteristics (cont'd)

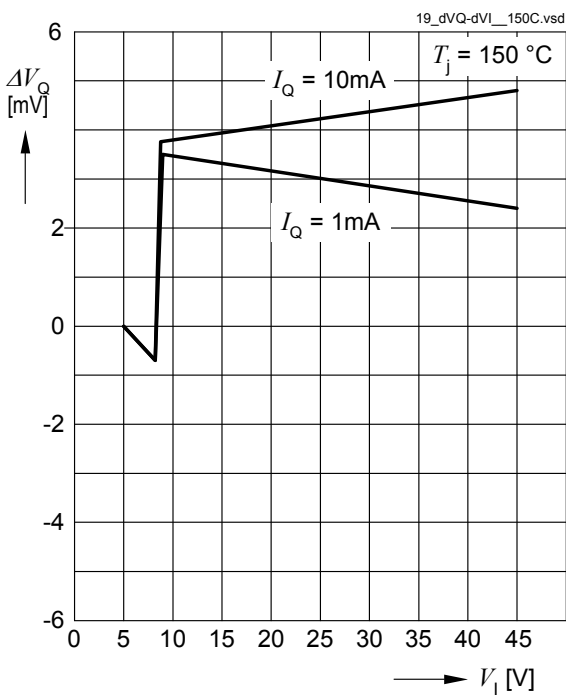
Line Regulation  $dV_Q$  versus Input Voltage Change  $dV_I$



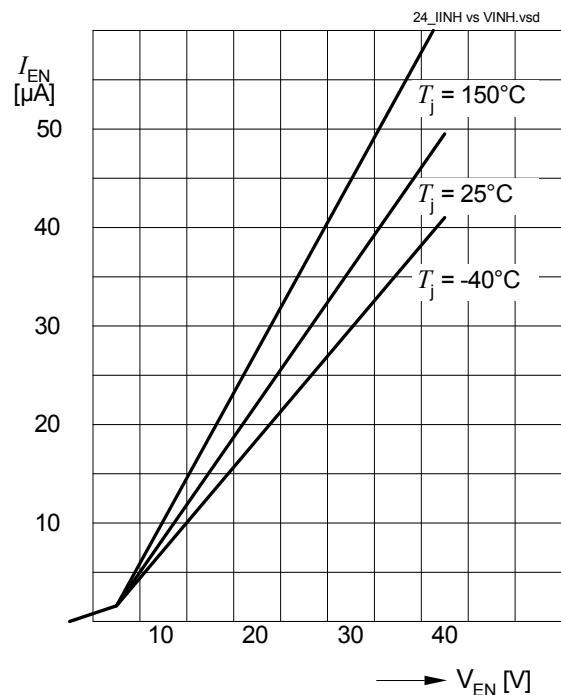
Line Regulation  $dV_Q$  versus Input Voltage Change  $dV_I$



Line Regulation  $dV_Q$  versus Input Voltage Change  $dV_I$

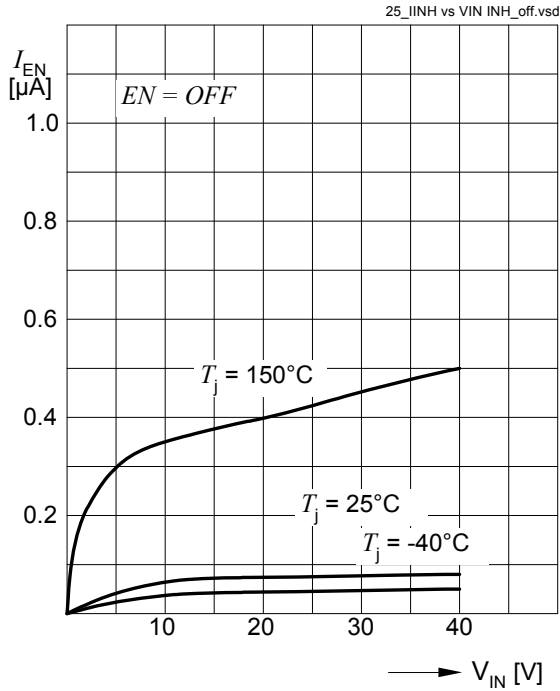


Enable Input Current  $I_{EN}$  versus Enable Input Voltage  $V_{EN}$

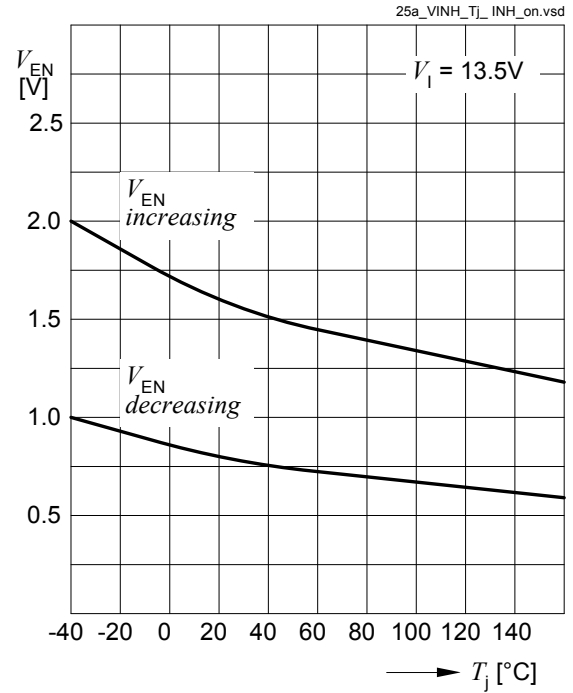


Typical Performance Characteristics (cont'd)

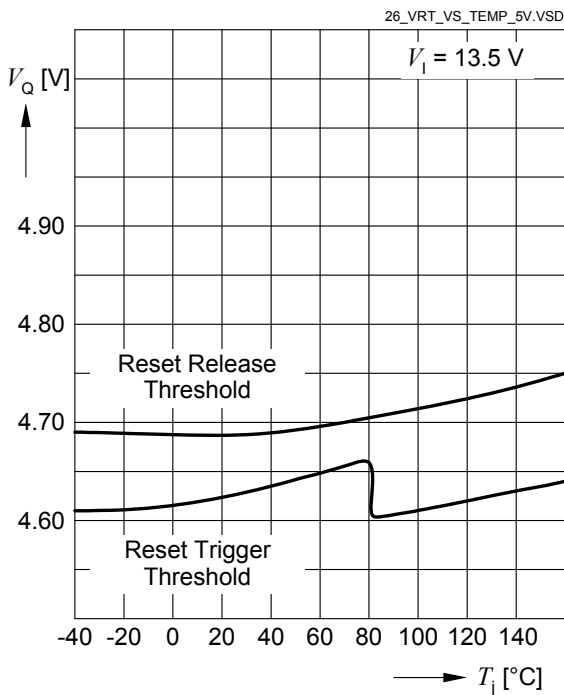
Enable Input Current  $I_{EN}$  versus Input Voltage  $V_I$ , EN=Off



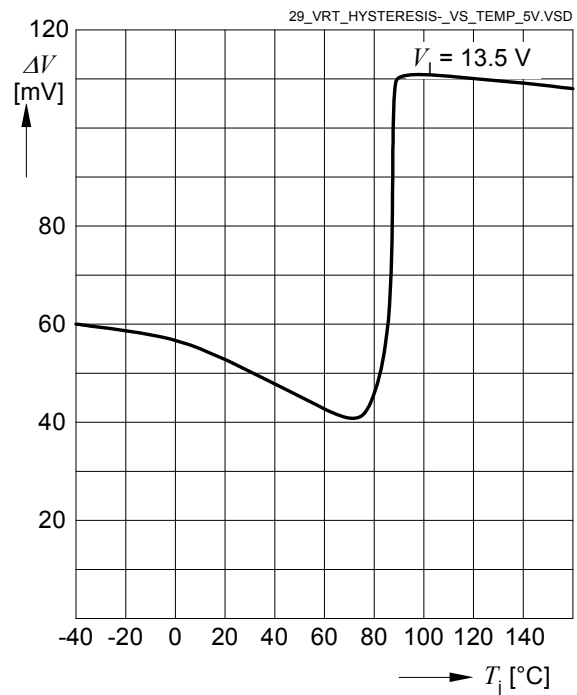
Enable High Level / Low Level Input Voltage  $V_{EN,H} / V_{EN,L}$  versus Junction Temperature  $T_j$



Reset Threshold  $V_{RT}$  versus Junction Temperature  $T_j$  (5V-Version)

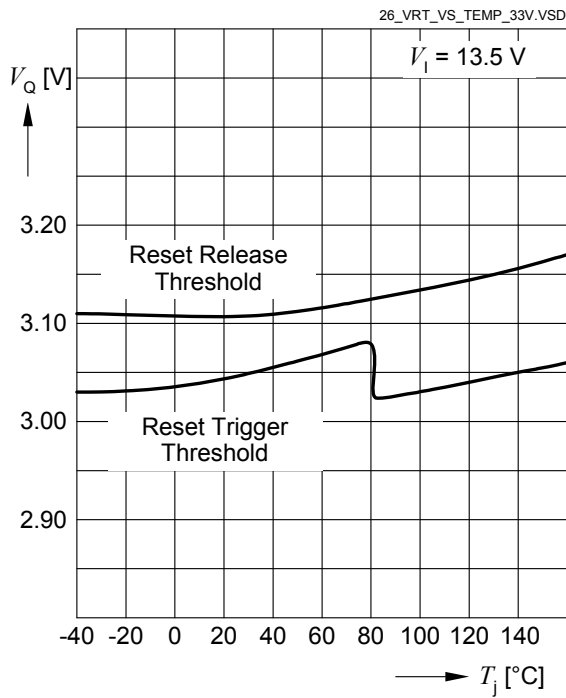


Reset Hysteresis versus Junction Temperature  $T_j$  (5V-Version)

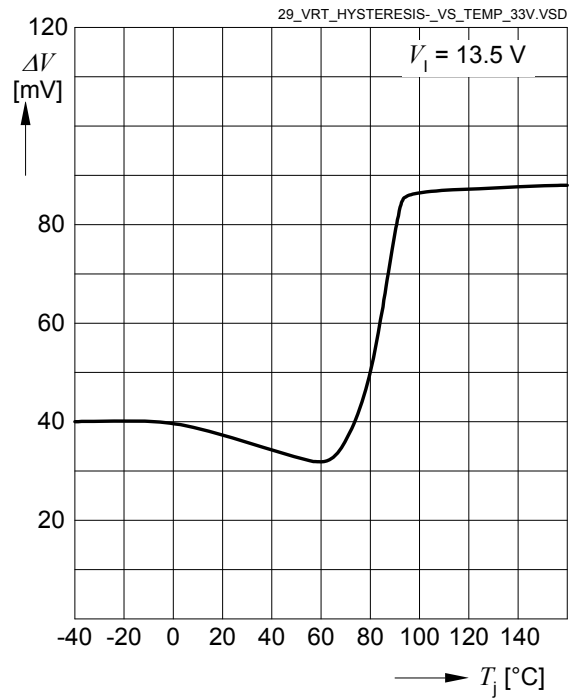


Typical Performance Characteristics (cont'd)

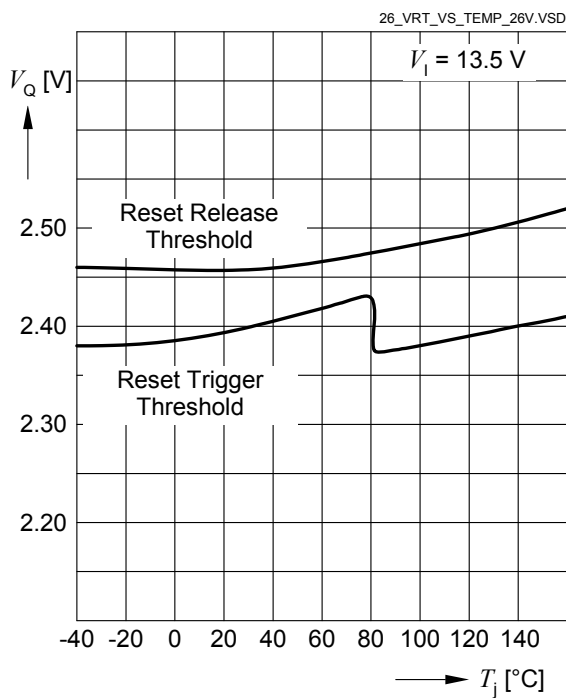
Reset Threshold  $V_{RT}$  versus Junction Temperature  $T_j$  (3.3V-Version)



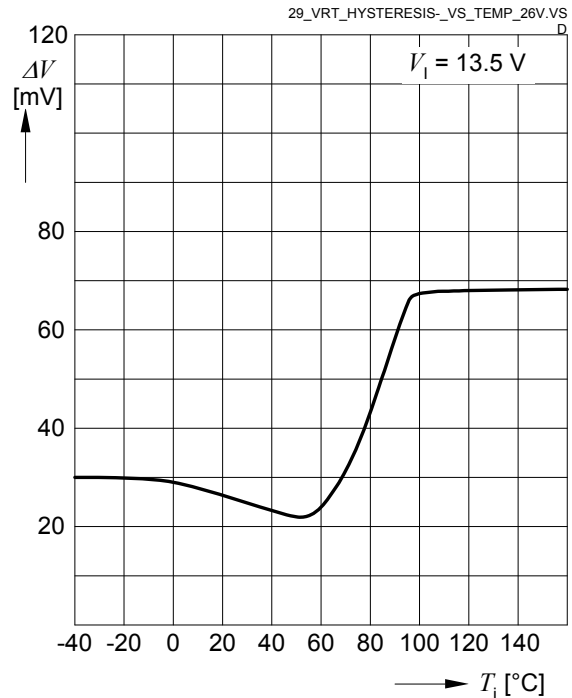
Reset Hysteresis versus Junction Temperature  $T_j$  (3.3V-Version)



Reset Threshold  $V_{RT}$  versus Junction Temperature  $T_j$  (2.6V-Version)

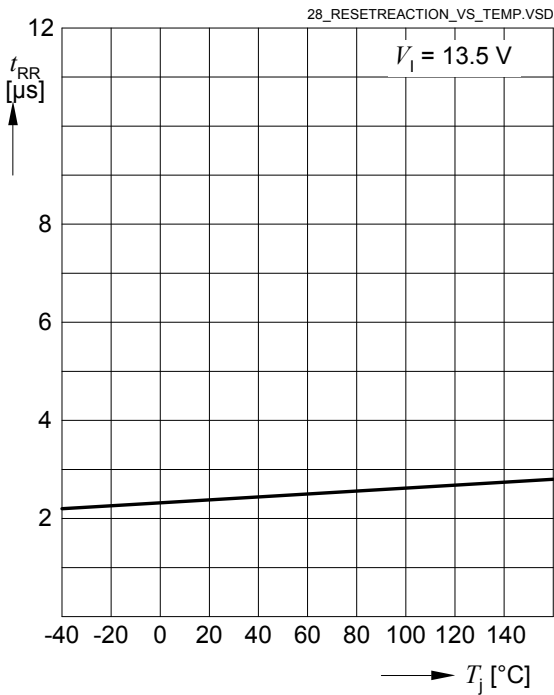


Reset Hysteresis versus Junction Temperature  $T_j$  (2.6V-Version)

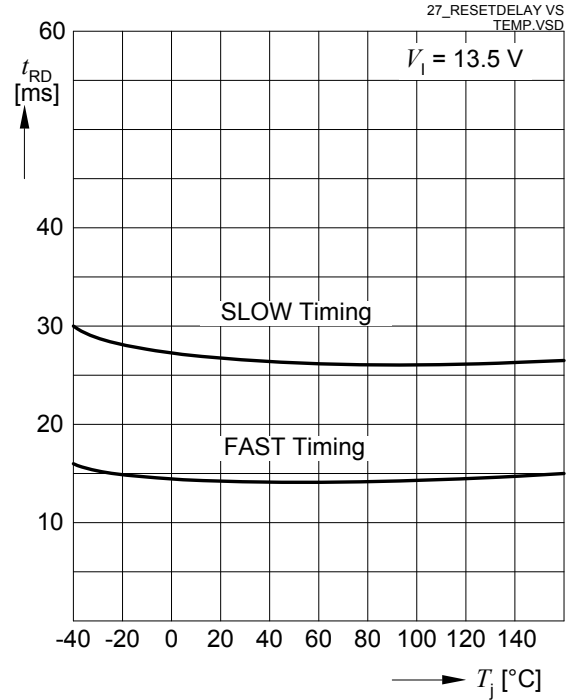


Typical Performance Characteristics (cont'd)

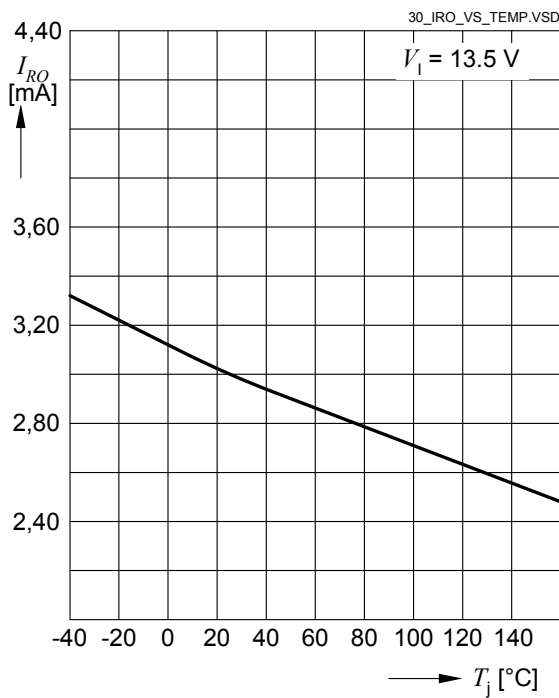
Reset Reaction Time  $t_{RR}$  versus Junction Temperature  $T_j$



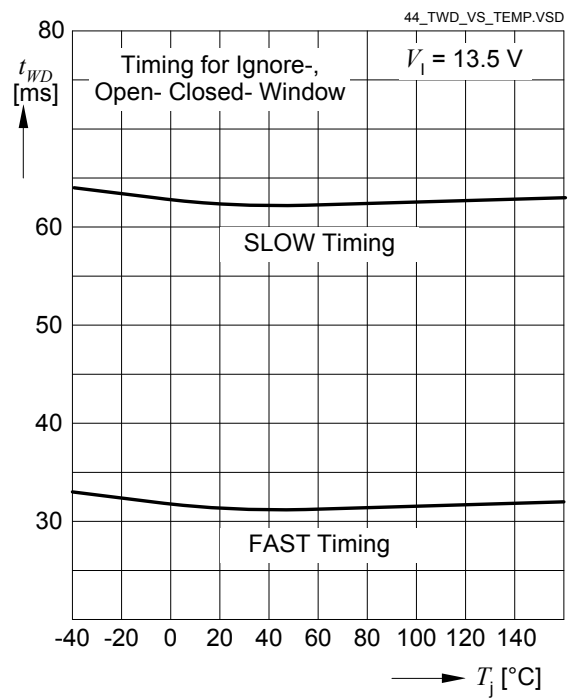
Reset Delay  $t_{RD}$  Time versus Junction Temperature  $T_j$



Reset Output Sink Current  $I_{RO}$  versus Junction Temperature  $T_j$

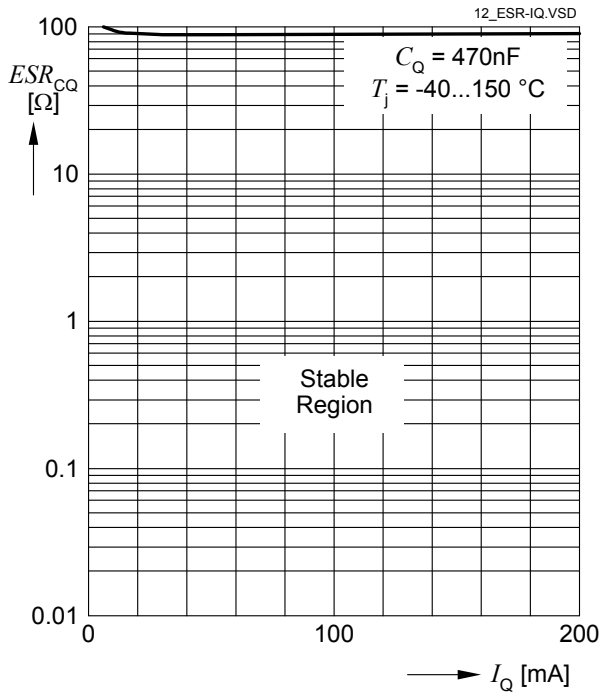


Watchdog Timing  $t_{WD}$  versus Junction Temperature  $T_j$



Typical Performance Characteristics (cont'd)

Region of Stability  $ESR(C_Q)$  versus Output Current  $I_Q$



## 6 Package Outlines

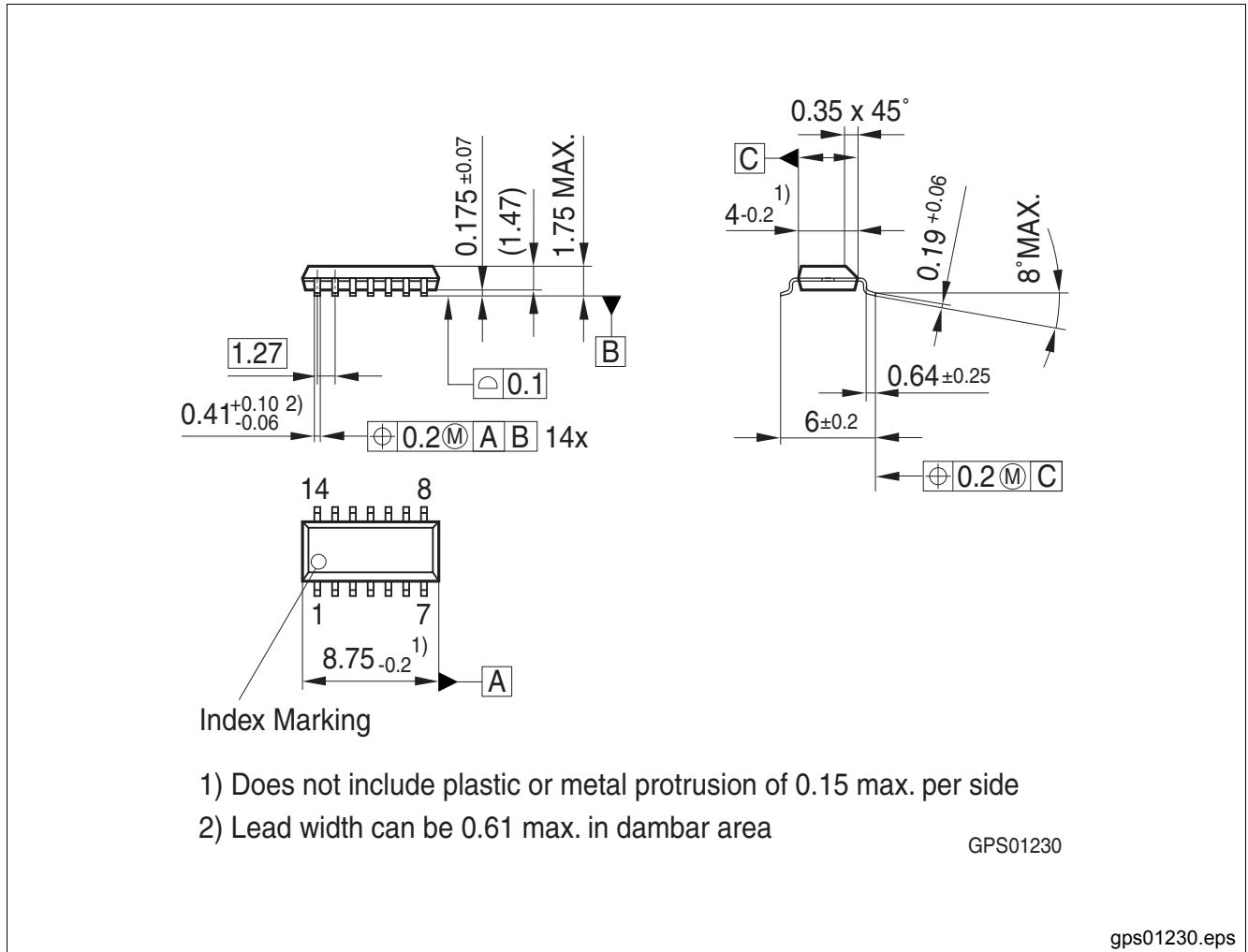


Figure 8 PG-DSO-14

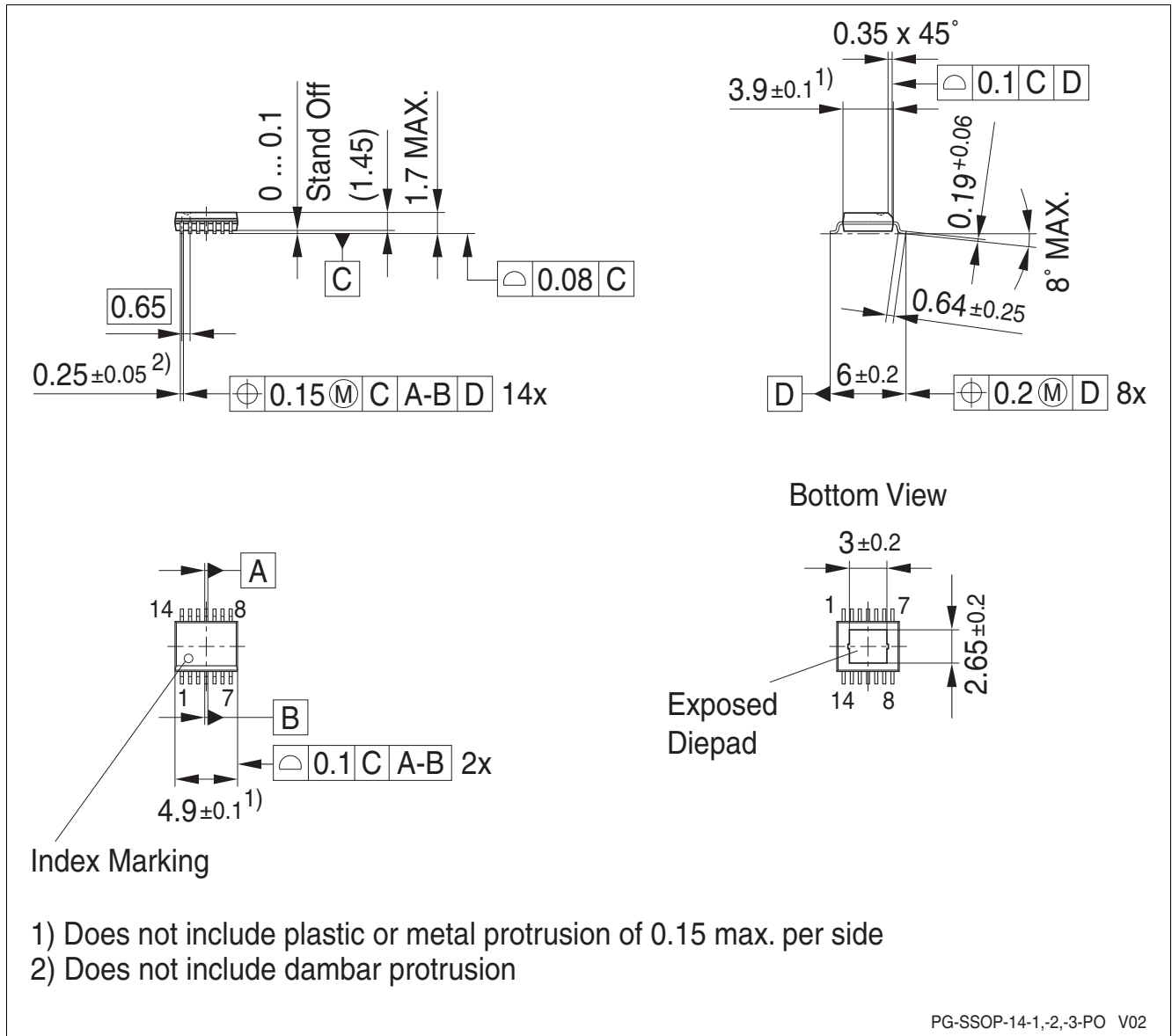


Figure 9 PG-SSOP-14 Exposed Pad

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

Dimensions in mm

## 7 Revision History

Revision	Date	Changes
1.21	2014-11-19	Editorial change in temperature range: “-40 °C < $T_j$ < 150 °C” changed to “ $T_j$ = -40 °C to +150 °C”
1.2	2009-04-28	2.6V version, 5V version in PG-SSOP-14 package and all related description added:
		In <b>“Features” on Page 2</b> “or 2.6 V” added
		In <b>“Features” on Page 2</b> package drawing for PG-DSO-14 updated, package drawing for PG-SSOP-14 added
		In <b>“Overview” on Page 2</b> in table at the bottom type “TLE7273-2GV26” and “TLE7273-2EV50” added
		In <b>“Pin Definitions and Functions (PG-DSO-14)” on Page 4</b> in description for Pin 1 “, TLE7273-2GV26” added
		<b>“Pin Assignments (PG-SSOP-14 Exposed Pad)” on Page 5</b> and <b>“Pin Definitions and Functions (PG-SSOP-14 Exposed Pad)” on Page 5</b> added;
		In <b>“Functional Range” on Page 7</b> <b>Item 4.2.3</b> added, in <b>Item 4.2.1</b> “, TLE7273-2EV50” added;
		In <b>“Thermal Resistances” on Page 7</b> values for PG-SSOP-14 package added: <b>Item 4.3.6</b> , <b>Item 4.3.7</b> , <b>Item 4.3.8</b> , <b>Item 4.3.9</b> and <b>Item 4.3.10</b> added
		In <b>“Power On Reset and Reset Output” on Page 8</b> “TLE7273-2EV50” in description added
		In <b>“Electrical Characteristics” on Page 11</b> all specific Items for 2.6V version added: <b>Item 5.2.5</b> , <b>Item 5.2.6</b> , <b>Item 5.2.22</b> , <b>Item 5.2.26</b> , <b>Item 5.2.30</b> , <b>Item 5.2.48</b> , <b>Item 5.2.52</b> and <b>Item 5.2.57</b> added; In <b>Item 5.2.44</b> , <b>Item 5.2.45</b> , <b>Item 5.2.49</b> , <b>Item 5.2.50</b> , <b>Item 5.2.51</b> and <b>Item 5.2.60</b> Conditions for 2.6V version added; In <b>Item 5.2.1</b> , <b>Item 5.2.2</b> , <b>Item 5.2.9</b> , <b>Item 5.2.20</b> , <b>Item 5.2.24</b> , <b>Item 5.2.28</b> , <b>Item 5.2.44</b> , <b>Item 5.2.45</b> , <b>Item 5.2.46</b> , <b>Item 5.2.54</b> , <b>Item 5.2.55</b> , <b>Item 5.2.59</b> and <b>Item 5.2.61</b> “, TLE7273-2EV50” added
		In <b>“Typical Performance Characteristics” on Page 15</b> Graphs <b>“Reset Threshold VRT versus Junction Temperature Tj (3.3V-Version)” on Page 19</b> , <b>“Reset Threshold VRT versus Junction Temperature Tj (3.3V-Version)” on Page 19</b> , <b>“Reset Threshold VRT versus Junction Temperature Tj (2.6V-Version)” on Page 19</b> and <b>“Reset Hysteresis versus Junction Temperature Tj (3.3V-Version)” on Page 19</b> added
		In <b>“Package Outlines” on Page 22</b> Outlines for PG-SSOP-14 added: <b>Figure 9</b>



Revision History

Revision	Date	Changes
1.1	2008-07-25	<p>3.3V version and all related description added:</p> <p>In <b>“Features” on Page 2</b> “3.3V” added</p> <p>In <b>“Overview” on Page 2</b> in table at the bottom type “TLE7273-2GV33” added</p> <p>In <b>“Pin Definitions and Functions (PG-DSO-14)” on Page 4</b> in description for Pin 1 “TLE7273-2GV33: open drain output;” added</p> <p>In <b>“Functional Range” on Page 7 Item 4.2.2</b> added</p> <p>In <b>“Power On Reset and Reset Output” on Page 8</b> description for dimensioning external pull-up resistor at RO added;</p> <p>In <b>“Electrical Characteristics” on Page 11</b> all specific Items for 3.3V version added: <b>Item 5.2.3, Item 5.2.4, Item 5.2.21, Item 5.2.25, Item 5.2.29, Item 5.2.47, Item 5.2.49, Item 5.2.50, Item 5.2.51, Item 5.2.53, Item 5.2.56</b> and <b>Item 5.2.60</b> added; In <b>Item 5.2.44</b> and <b>Item 5.2.45</b> Conditions for 3.3V version added;</p>
1.0	2008-04-10	final version data sheet

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