



BUK7Y7R0-40H

N-channel 40 V, 7.0 mΩ standard level MOSFET in LFPAK56

30 June 2020

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
 - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
 - Improved SOA and avalanche capability compared to standard TrenchMOS
 - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
 - Improved reliability, with reduced R_{th} and R_{DSon}
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

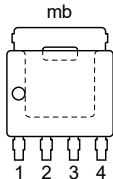
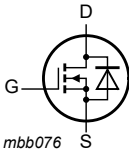
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	[1]	-	-	68	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1		-	-	64	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C};$ Fig. 11		4	5.7	7	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 15\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14	-	3.7	7.4	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 15\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 17	-	10	-	nC
S	softness factor	$I_S = 15\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ °C}$; Fig. 17	-	0.78	-	

[1] 68A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y7R0-40H	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y7R0-40H	77H040

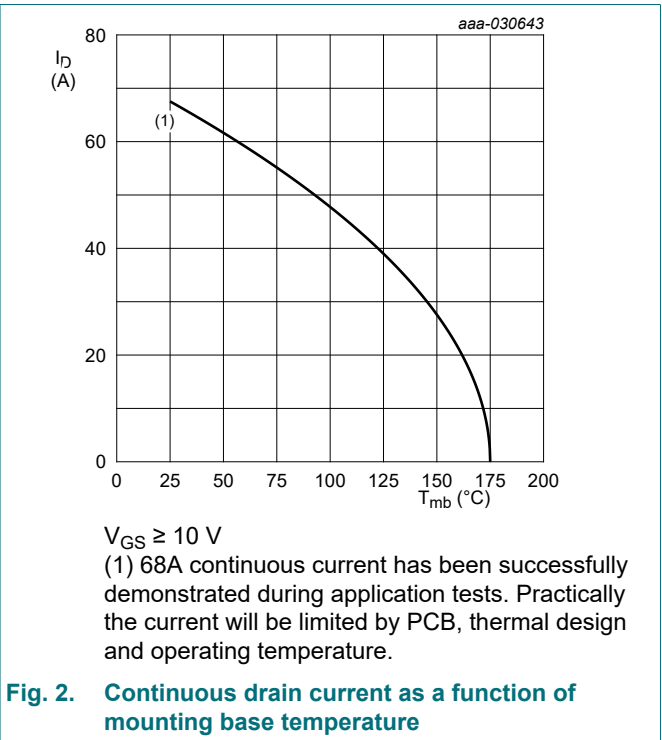
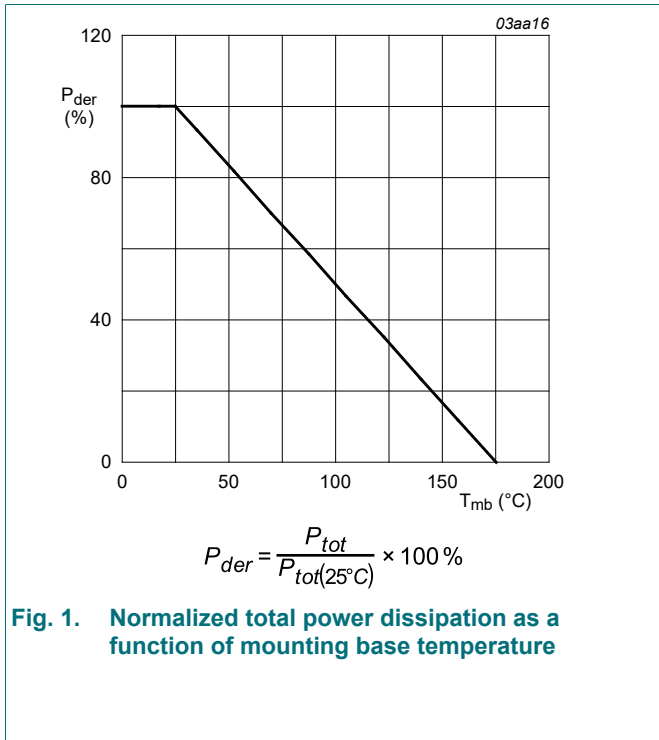
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	64	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	68	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	48	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	272	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	64	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	272	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 68\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped; Fig. 4	[2] [3]	-	19.9	mJ

- [1] 68A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.



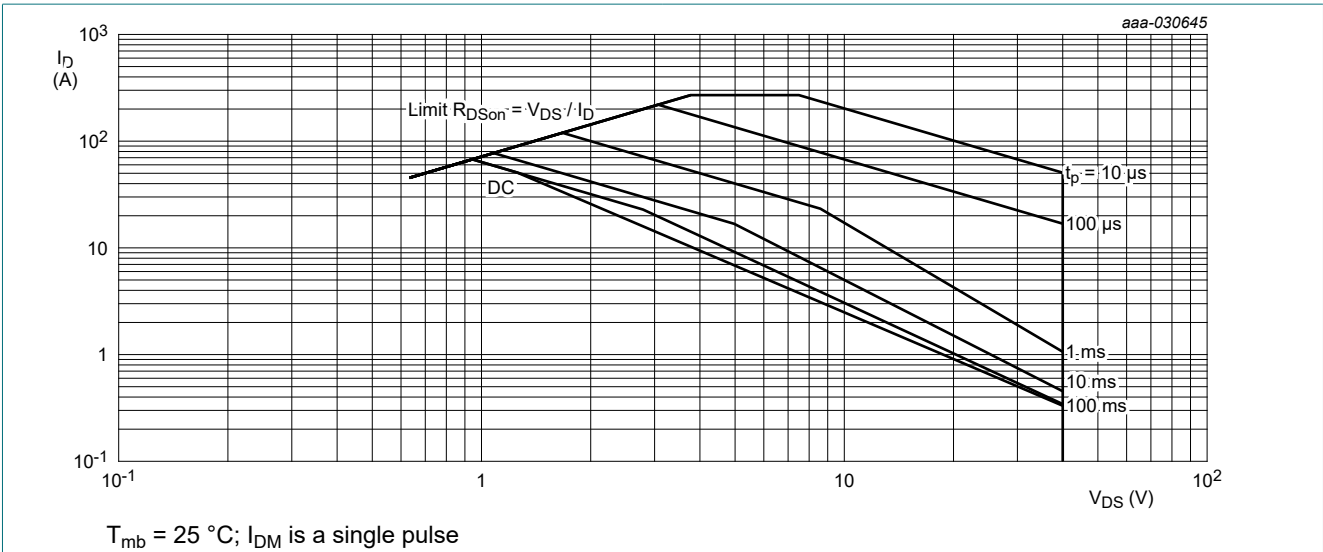


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

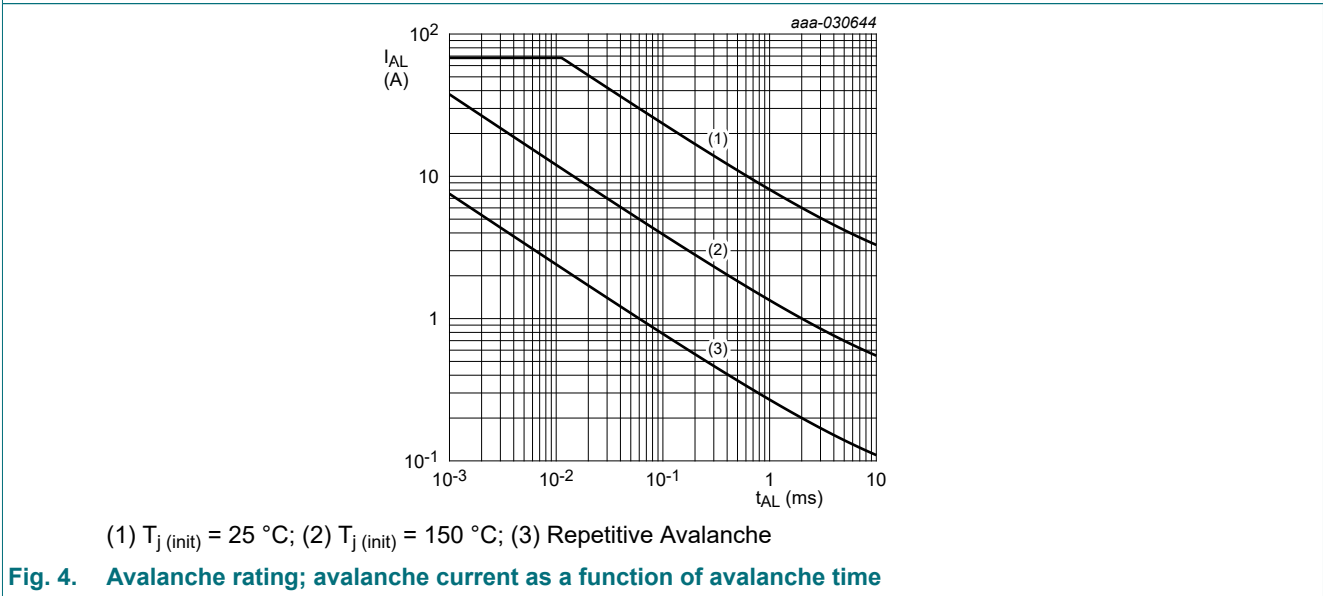


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.17	2.35	K/W

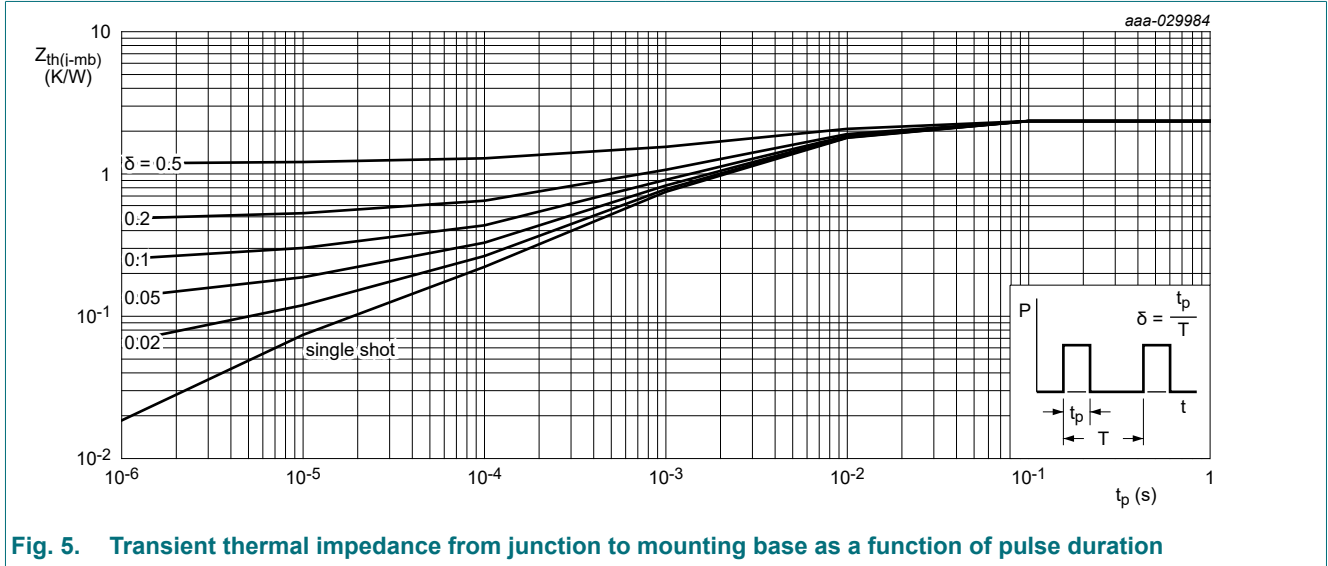


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	40	43	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_J = -40 \text{ }^\circ\text{C}$	-	40.5	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_J = -55 \text{ }^\circ\text{C}$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 9 ; Fig. 10	2.4	3	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_J = -55 \text{ }^\circ\text{C};$ Fig. 10	-	-	4.3	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_J = 175 \text{ }^\circ\text{C};$ Fig. 10	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	0.01	1	μA
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 125 \text{ }^\circ\text{C}$	-	0.51	10	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 175 \text{ }^\circ\text{C}$	-	39	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 11	4	5.7	7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 105 \text{ }^\circ\text{C};$ Fig. 12	5.5	8	10.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 125 \text{ }^\circ\text{C};$ Fig. 12	6	8.7	11.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 175 \text{ }^\circ\text{C};$ Fig. 12	7.3	10.7	13.6	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}; T_J = 25 \text{ }^\circ\text{C}$	0.3	0.7	1.8	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 13 ; Fig. 14	-	18	26	nC
Q_{GS}	gate-source charge		-	5.4	8.1	nC
Q_{GD}	gate-drain charge		-	3.7	7.4	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ Fig. 15 $T_J = 25 \text{ }^\circ\text{C};$	-	1164	1630	pF
C_{oss}	output capacitance		-	408	571	pF
C_{rss}	reverse transfer capacitance		-	63	139	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 30 \text{ V}; R_L = 2 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5 \text{ } \Omega$	-	5.8	-
t_r	rise time	-		4	-	ns
$t_{d(off)}$	turn-off delay time	-		10.5	-	ns
t_f	fall time	-		4.4	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15 \text{ A}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 16	-	0.83	1	V
t_{rr}	reverse recovery time	$I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V};$ Fig. 17	-	20	-	ns
Q_r	recovered charge		-	10	-	nC
S	softness factor	$I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 17	-	0.78	-	
		$I_S = 15 \text{ A}; dI_S/dt = -500 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 17	-	0.66	-	

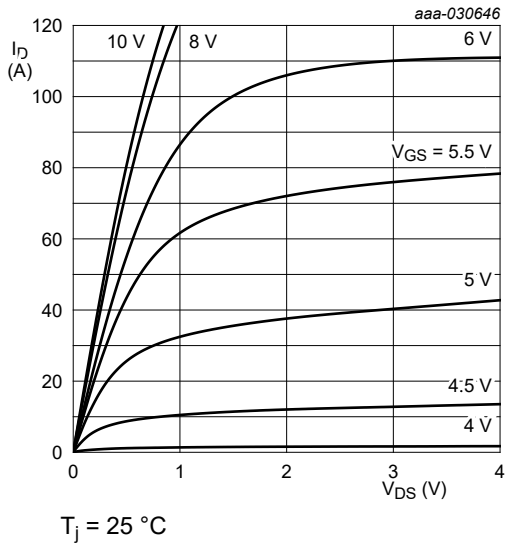


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

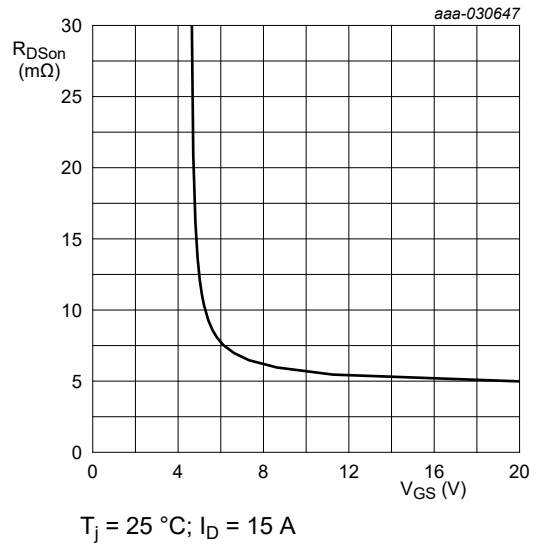


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

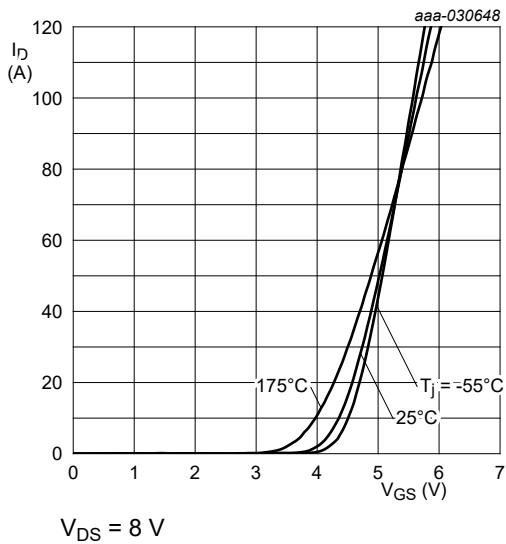


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

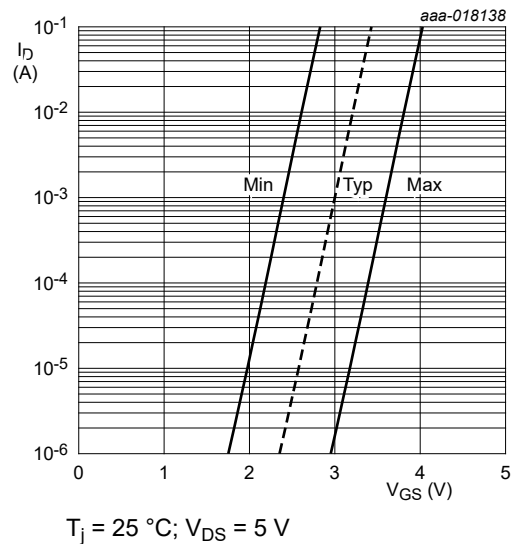


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

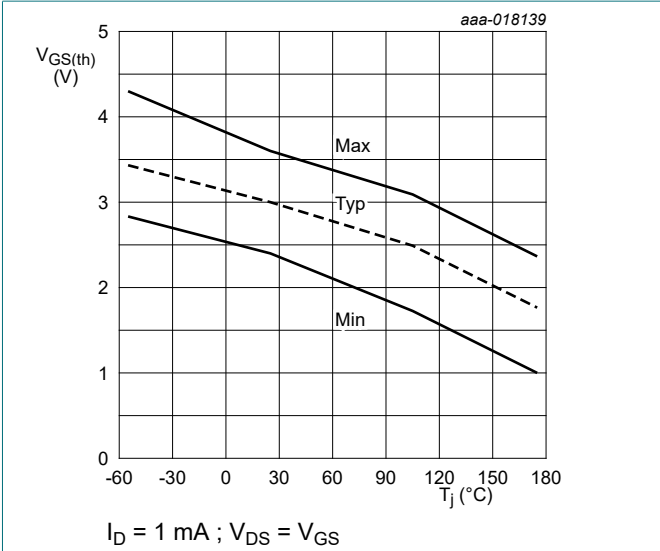


Fig. 10. Gate-source threshold voltage as a function of junction temperature

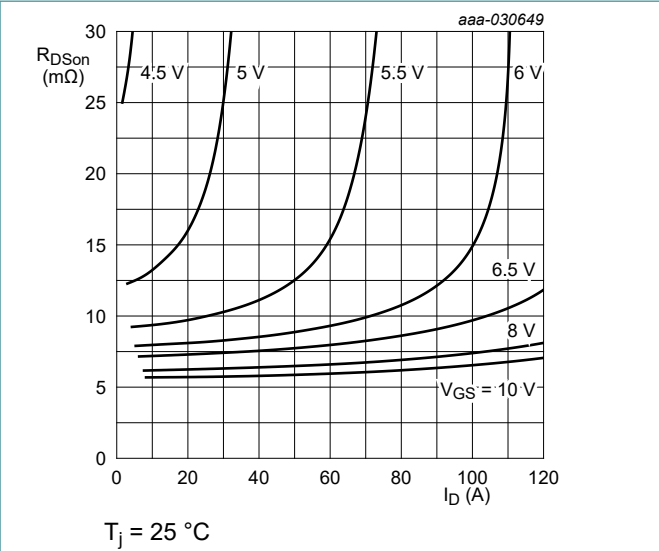


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

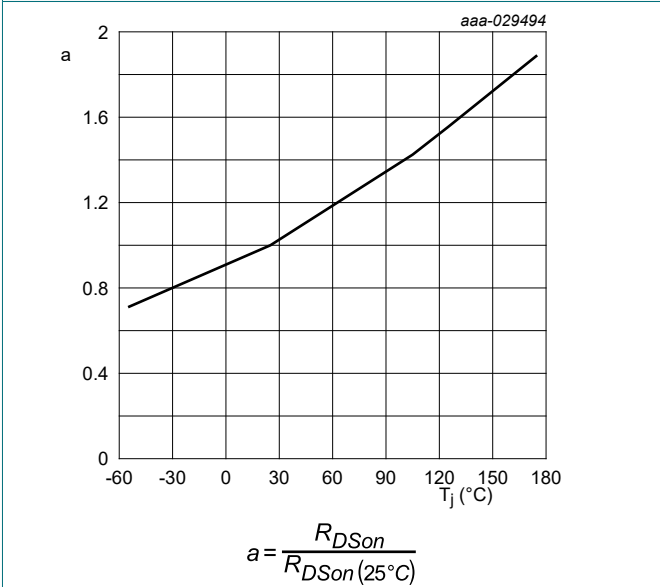


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

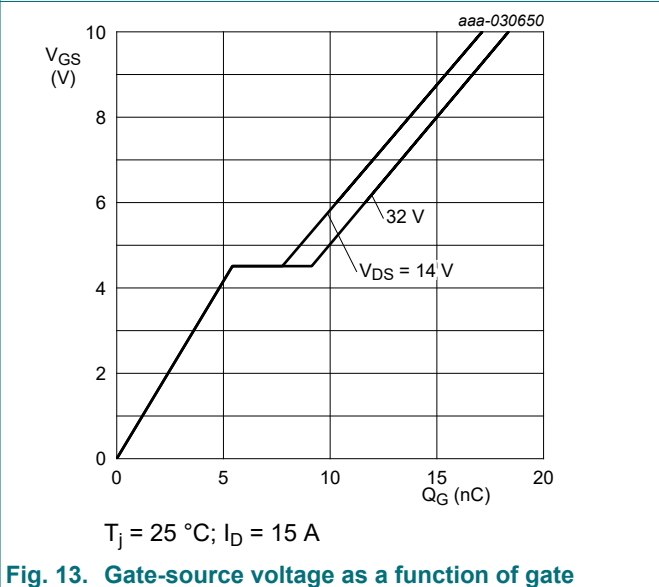


Fig. 13. Gate-source voltage as a function of gate charge; typical values

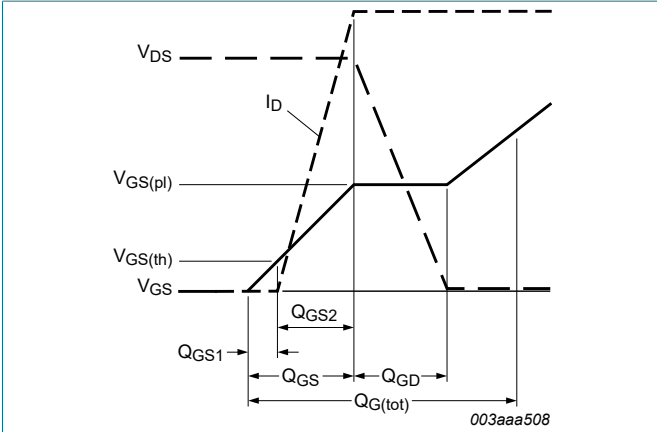
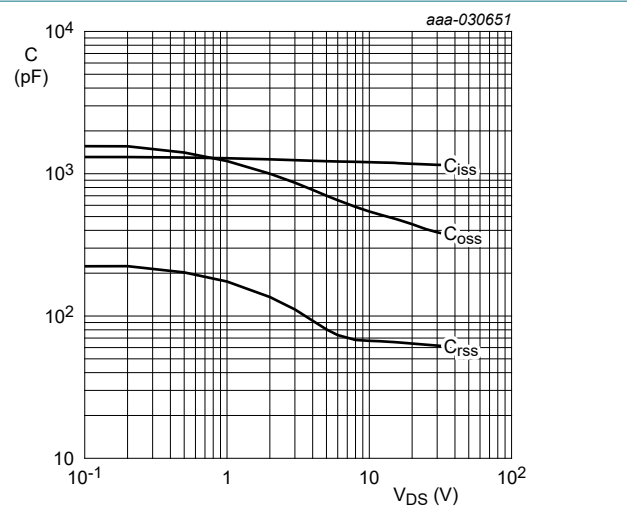
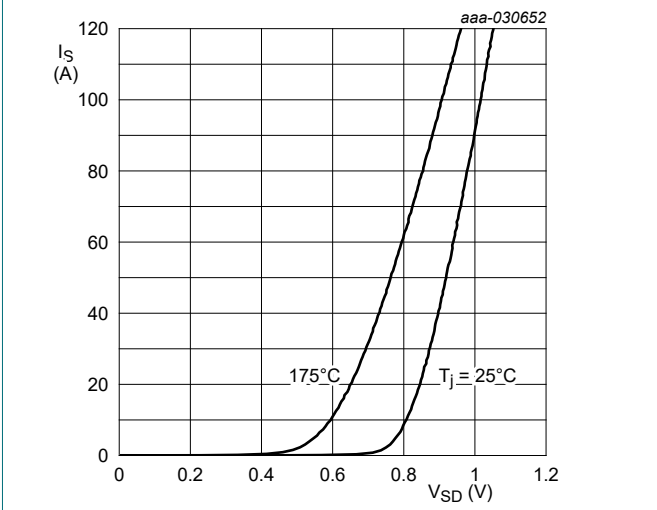


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

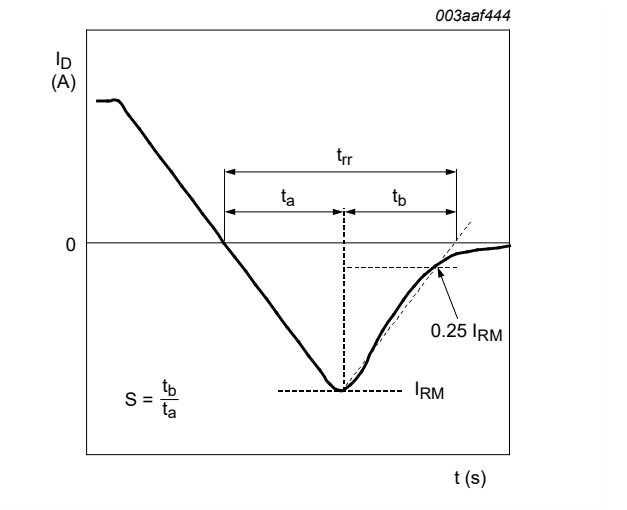


Fig. 17. Reverse recovery timing definition

11. Package outline

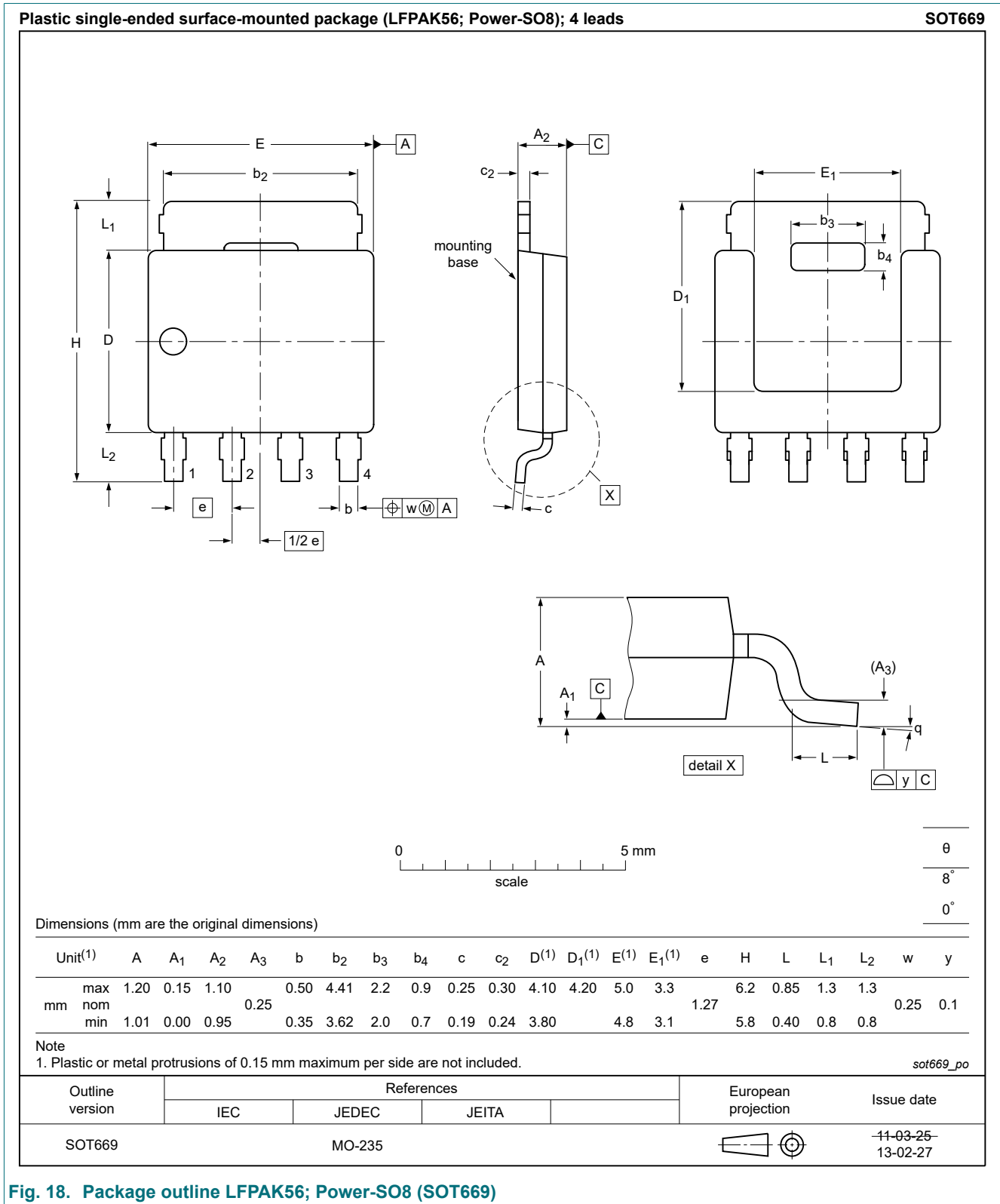


Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

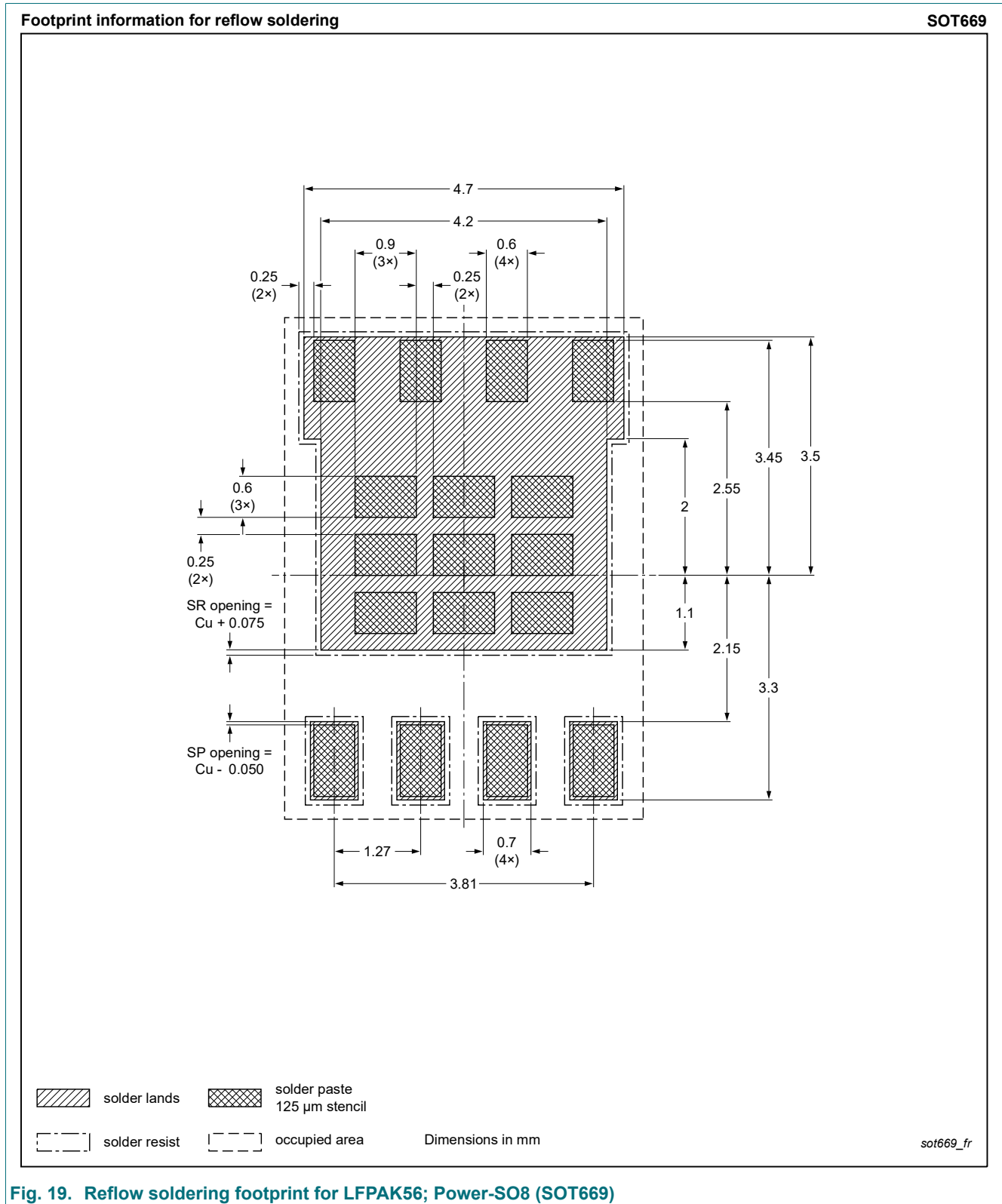
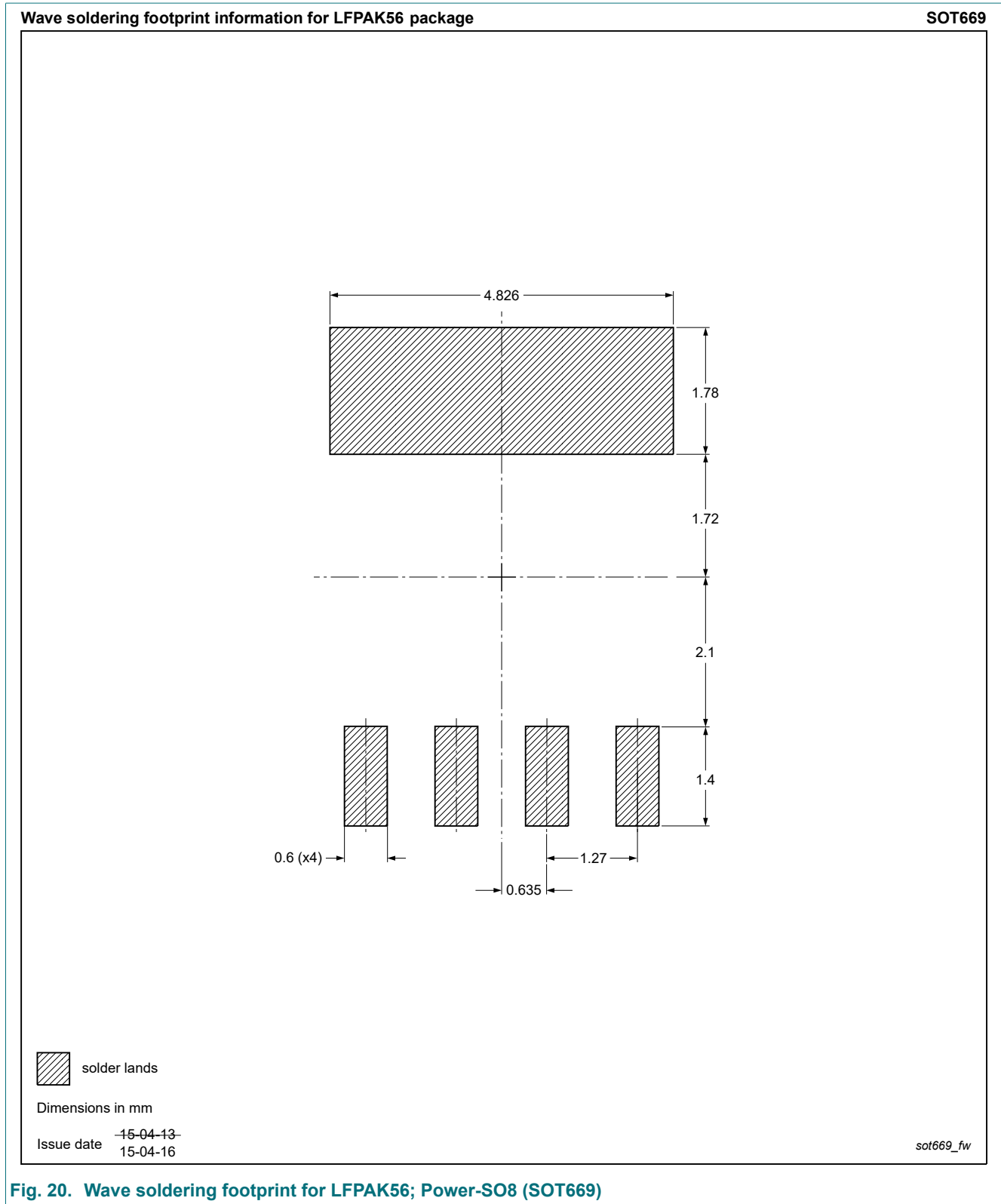


Fig. 19. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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