CLOCK DIVIDER

ICS542

Description

The ICS542 is cost effective way to produce a high-quality clock output divided from a clock input. The chip accepts a clock input up to 156 MHz at 3.3 V and produces a divide by 2, 4, 6, 8, 12, or 16 of the input clock. There are two outputs on the chip, one being a low-skew divide by two of the other.

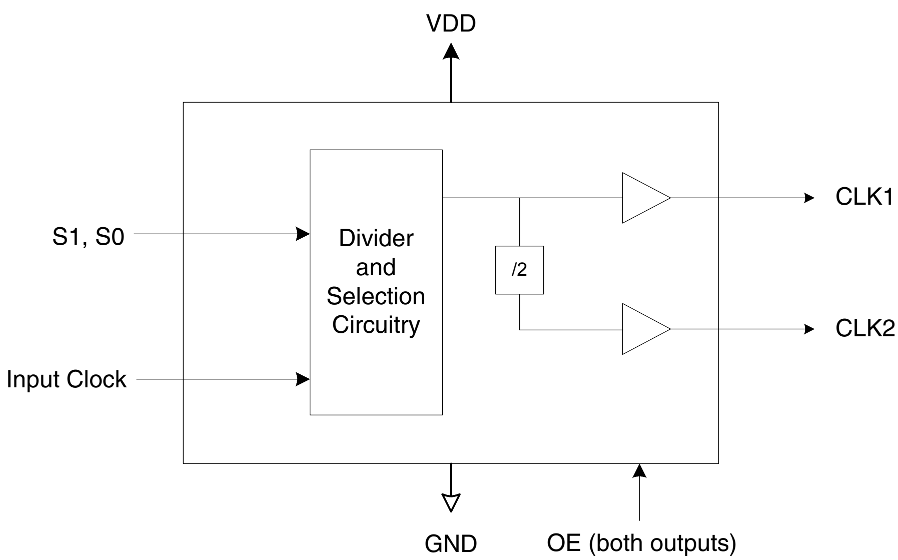
For instance, if an 100 MHz input clock is used, the ICS542 can produce low-skew 50 MHz and 25 MHz clocks, or low skew 25 MHz and 12.5 MHz clocks. The chip has an all-chip power-down mode that stops the outputs low, and an OE pin that tri-states the outputs.

See the ICS541 and ICS543 for other clock dividers, and the ICS501, 502, 511, 512, and 525 for clock multipliers.

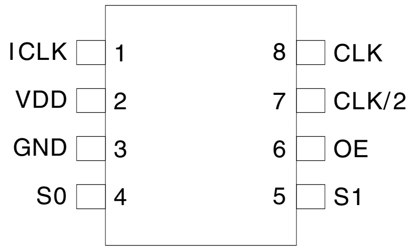
Features

- 8-pin SOIC package, Pb free
- Available in RoHS compliant package
- IDT's lowest cost clock divider
- Low skew (500 ps) outputs. One is /2 of the other
- Easy to use with other generators and buffers
- Input clock frequency up to 156 MHz
- Output clock duty cycle of 45/55
- Power-down turns off chip
- Output Enable
- Advanced, low-power CMOS process
- Operating voltage of 3.3 V or 5 V
- Does not degrade phase noise - no PLL
- Available in industrial and commercial temperature ranges

Block Diagram



Pin Assignment



8-pin (150 mil) SOIC

Clock Decoding Table

S1	S0	CLK	CLK/2
0	0	Power Down All	
0	1	Input/6	Input/12
1	0	Input/8	Input/16
1	1	Input/2	Input/4

0 = connect directly to ground

1 = connect directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	XI	Clock input.
2	VDD	Power	Connect to +3.3 V or +5 V.
3	GND	Power	Connect to ground.
4	S0	Input	Select 0 for output clock. Connect to GND or VDD, per decoding table above. Internal pull-up resistor.
5	S1	Input	Select 1 for output clock. Connect to GND or VDD, per decoding table above. Internal pull-up resistor.
6	OE	Input	Output Enable. Tri-states both output clocks when low. Internal pull-up resistor.
7	CLK/2	Output	Clock output per table above. Low skew divide by two of pin 8 clock.
8	CLK	Output	Clock output per table above.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS542 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the

same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS542. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS542. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	° C
Ambient Operating Temperature (industrial)	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	3.0		5.5	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temp. 0 to +70° C (commercial), -40 to +85° C (industrial)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage,	V_{IH}	ICLK (pin 1)	VDD/2+1	VDD/2		V
Input Low Voltage	V_{IL}	ICLK (pin 1)		VDD/2	VDD/2-1	V
Input High Voltage	V_{IH}	S0, S1, OE	2			V
Input Low Voltage	V_{IL}	S0, S1, OE			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Operating Supply Current	I_{DD}	No Load, 5.0 V, 11 sel		11		mA
Operating Supply Current	I_{DD}	No Load, 3.3 V, 11 sel		7		mA
Short Circuit Current	I_{OS}			±40		mA
Input Capacitance	C_{IN}	S0, S1, OE		4		pF
Nominal Output Impedance	Z_O	at VDD/2		20		Ω

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temp. 0 to +70° C (commercial), -40 to +85° C (industrial)

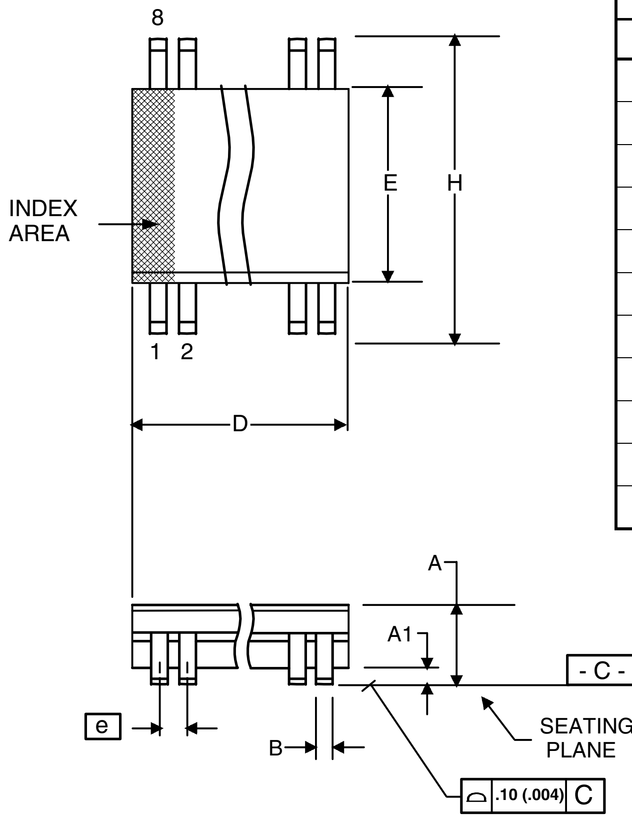
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, clock input		VDD = 5 V	0		156	MHz
Input Frequency, clock input		VDD = 3.3 V	0		156	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V		1		ns
Output Fall Time	t_{OF}	2.0 to 0.8 V		1		ns
Duty Cycle		at VDD/2	45	49 to 51	55	%
Skew of Output Clocks		rising edges at VDD/2			500	ps
Propagation Delay		ICLK to CLK			15	ns

Thermal Characteristics

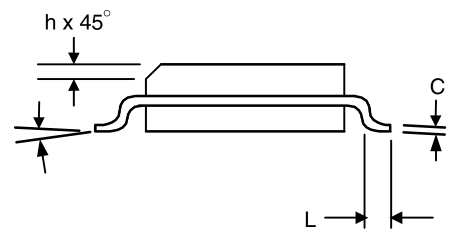
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
542MLF	542MLF	Tubes	8-pin SOIC	0 to +70° C
542MLFT	542MLF	Tape and Reel	8-pin SOIC	0 to +70° C
542MILF	542MILF	Tubes	8-pin SOIC	-40 to +85° C
542MILFT	542MILF	Tape and Reel	8-pin SOIC	-40 to +85° C

Parts that are ordered with a “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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