

# 64-pin CK505 Compatible Clock w/Fully Integrated Voltage Regulator + Integrated Series Resistor

9LRS3165B

### Recommended Application:

CK505 compatible clock with fully integrated voltage regulator and internal series resistor on differential outputs

### Output Features:

- 2 - CPU differential low power push-pull pairs
- 9 - SRC differential low power push-pull pairs
- 1 - CPU/SRC selectable differential low power push-pull pair
- 1 - SRC/DOT selectable differential low power push-pull pair
- 5 - PCI, 33MHz
- 1 - PCI\_F, 33MHz free running
- 1 - USB, 48MHz
- 1 - REF, 14.318MHz

### Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 100ppm frequency accuracy on CPU & SRC clocks

### Features/Benefits:

- Does not require external pass transistor for voltage regulator
- Integrated 33ohm series resistors on differential outputs,  $Z_0=50\Omega$
- Supports spread spectrum modulation, default is 0.5% down spread
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Selectable between one SRC differential push-pull pair and two single-ended outputs
- Meets PCIEX Gen2 specification on dedicated SRC outputs. Muxed SRC outputs meet PCIEX Gen1 specification, except SRC1.
- Single-ended programmable slew rate control for RFI reduction
- Meets PCIEX <85ps cycle-to-cycle jitter for SRC[11:1]

### Pin Configuration

PCI0/CR#_A	1	64	SCLK
VDDPCI	2	63	SDATA
PCI1/CR#_B	3	62	REF/FSLC/TEST_SEL
PCI2/TME	4	61	VDDREF
PCI3	5	60	X1
PCI4/27_SEL	6	59	X2
PCI5_F/ITP_EN	7	58	GNDREF
GNDPCI	8	57	FSLB/TEST_MODE
VDD48	9	56	CK_PWRGD/PD#
USB48M/FSLA	10	55	VDDCPU
GND48	11	54	CPUT_LR0
VDDI/O96MHz	12	53	CPUC_LR0
DOT96T/SRCT_LR0	13	52	GNDCPU
DOT96C/SRCC_LR0	14	51	CPUT_F_LR1
GND	15	50	CPUC_F_LR1
VDD	16	49	VDDCPU_IO
27FIX/LCDT/SRCT_LR1/SE1	17	48	NC
27SS/LCDC/SRCC_LR1/SE2	18	47	CPUT_ITP_LR2/SRCT8
GND	19	46	CPUC_ITP_LR2/SRCC8
VDDPLL3I/O	20	45	VDDSRCI/O
SRCT_LR2/SATACLKT	21	44	SRCT_LR7/CR#_F
SRCC_LR2/SATACLKC	22	43	SRCC_LR7/CR#_E
GNDSRC	23	42	GNDSRC
SRCT_LR3/CR#_C	24	41	SRCT_LR6
SRCC_LR3/CR#_D	25	40	SRCC_LR6
VDDSRCI/O	26	39	VDDSRC
SRCT_LR4	27	38	PCL_STOP#
SRCC_LR4	28	37	CPU_STOP#
GNDSRC	29	36	VDDSRCI/O
SRCT_LR9	30	35	SRCC_LR10
SRCC_LR9	31	34	SRCT_LR10
SRCC_LR11/CR#_G	32	33	SRCT_LR11/CR#_H

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64-TSSOP

Table 1: CPU Frequency Select Table

FS <sub>L</sub> C <sup>2</sup> B0b7	FS <sub>L</sub> B <sup>1</sup> B0b6	FS <sub>L</sub> A <sup>1</sup> B0b5	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266.66	100.00	33.33	14.318	48.00	96.00
0	0	1	133.33					
0	1	0	200.00					
0	1	1	166.66					
1	0	0	333.33					
1	0	1	100.00					
1	1	0	400.00					
1	1	1	Reserved					

1. FS<sub>L</sub>A and FS<sub>L</sub>B are low-threshold inputs. Please see V<sub>IL,FS</sub> and V<sub>IH,FS</sub> specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.

2. FS<sub>L</sub>C is a three-level input. Please see the V<sub>IL,FS</sub> and V<sub>IH,FS</sub> specifications in the Input/Supply/Common Output Parameters Table for correct values.

## TSSOP Pin Description

Pin#	Pin Name	Type	DESCRIPTION
1	PCI0/CR#_A	I/O	3.3V PCI clock output or Clock Request control A for either SRC0 or SRC2 pair The power-up default is PCI0 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 0 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_A_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
2	VDDPCI	PWR	Power supply pin for the PCI outputs, 3.3V nominal
3	PCI1/CR#_B	I/O	3.3V PCI clock output/Clock Request control B for either SRC1 or SRC4 pair The power-up default is PCI1 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 1 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_B_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 4 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
4	PCI2/TME	I/O	3.3V PCI clock output / Trusted Mode Enable (TME) Latched Input. This pin is sampled on power-up as follows 0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed After being sampled on power-up, this pin becomes a 3.3V PCI Output
5	PCI3	OUT	3.3V PCI clock output.
6	PCI4/27_SEL	I/O	3.3V PCI clock output / 27MH mode select for pin17, 18 strap. On powerup, the logic value on this pin determines the power-up default of DOT_96/SRC0 and 27MHz/SRC1 output and the function table for the pin17 and pin18.
7	PCI5_F/ITP_EN	I/O	Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 46 and 47 are an ITP or SRC pair. 0 =SRC8/SRC8# 1 = ITP/ITP#
8	GNDPCI	PWR	Ground for PCI clocks.
9	VDD48	PWR	Power supply for USB clock, nominal 3.3V.
10	USB48M/FSLA	I/O	Fixed 48MHz USB clock output. 3.3V / 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for V <sub>il_FS</sub> and V <sub>ih_FS</sub> values.
11	GND48	PWR	Ground pin for the 48MHz outputs.
12	VDDI/O96MHz	PWR	1.05V to 3.3V from external power supply
13	DOT96T/SRCT_LR0	OUT	True clock of SRC or DOT96. The power-up default function depends on 27_Select,1= SRC0, 0=DOT96
14	DOT96C/SRCC_LR0	OUT	Complement clock of SRC or DOT96. The power-up default function depends on 27_Select,1= SRC0, 0=DOT96
15	GND	PWR	Ground pin for the DOT96 clocks.
16	VDD	PWR	Power supply for SRC / SE1 and SE2 clocks, 3.3V nominal.

## TSSOP Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
17	27FIX/LCDT/SRCT_LR1/SE1	OUT	Single-ended 3.3V 27MHz fix clock output / True clock of differential SRC1 or LCD clock pair / Single ended 3.3V peripheral clock output. The default output selection is determined by the SEL_27 default latch value. See below: <b>27_SEL=0:</b> LCD100 with -0.5% down spread is selected as default. LCD100 spread percentage can be adjusted OR output can be changed to SRC or 3.3V single-ended peripheral clock output via SMBUS B1b[4:1]. <b>27_SEL=1:</b> Single-ended 27FIX output is selected.
18	27SS/LCDC/SRCC_LR1/SE2	OUT	Single-ended 3.3V 27MHz fix clock output / Complementary clock of differential SRC1 or LCD clock pair / Single ended 3.3V peripheral clock output. The default output selection is determined by the SEL_27 default latch value. See below: <b>27_SEL=0:</b> LCD100 with -0.5% down spread is selected as default. LCD100 spread percentage can be adjusted OR output can be changed to SRC or 3.3V single-ended peripheral clock output via SMBUS B1b[4:1]. <b>27_SEL=1:</b> Single-ended 27SS output is selected with -0.5% down spread as default. Spread percentage can be adjusted via SMBUS B1b[4:1].
19	GND	PWR	Ground pin for SRC / SE1 and SE2 clocks, PLL3.
20	VDDPLL3/O	PWR	1.05V to 3.3V from external power supply
21	SRCT_LR2/SATACLKT	OUT	True clock of differential SRC/SATA clock pair.
22	SRCC_LR2/SATACLKC	OUT	Complement clock of differential SRC/SATA clock pair.
23	GNDSRC	PWR	Ground pin for SRC clocks.
24	SRCT_LR3/CR#_C	I/O	True clock of differential SRC clock pair/ Clock Request control C for either SRC0 or SRC2 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_C_EN bit located in byte 5 of SMBUS address space. Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair
25	SRCC_LR3/CR#_D	I/O	Complementary clock of differential SRC clock pair/ Clock Request control D for either SRC1 or SRC4 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_D_EN bit located in byte 5 of SMBUS address space. Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default), 1= CR#_D controls SRC4 pair
26	VDDSRCI/O	PWR	1.05V to 3.3V from external power supply
27	SRCT_LR4	I/O	True clock of differential SRC clock pair 4
28	SRCC_LR4	I/O	Complement clock of differential SRC clock pair 4
29	GNDSRC	PWR	Ground pin for SRC clocks.
30	SRCT_LR9	OUT	True clock of differential SRC clock pair.
31	SRCC_LR9	OUT	Complement clock of differential SRC clock pair.
32	SRCC_LR11/CR#_G	I/O	SRC11 complement /Clock Request control for SRC9 pair The power-up default is SRC11#, but this pin may also be used as a Clock Request control of SRC9 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBUS configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC9 pair using byte 6, bit 5 of SMBUS configuration space Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9

## TSSOP Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
33	SRCT_LR11/CR#_H	I/O	SRC11 true or Clock Request control H for SRC10 pair The power-up default is SRC11, but this pin may also be used as a Clock Request control of SRC10 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC10 pair using byte 6, bit 4 of SMBus configuration space Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10.
34	SRCT_LR10	OUT	True clock of differential SRC clock pair.
35	SRCC_LR10	OUT	Complement clock of differential SRC clock pair.
36	VDDSRCI/O	PWR	1.05V to 3.3V from external power supply
37	CPU_STOP#	IN	Stops all CPU Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values
38	PCI_STOP#	IN	Stops all PCI Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values
39	VDDSRC	PWR	VDD pin for SRC Pre-drivers. 3.3V nominal
40	SRCC_LR6	OUT	Complement clock of low power differential SRC clock pair.
41	SRCT_LR6	OUT	True clock of low power differential SRC clock pair.
42	GNDSRC	PWR	Ground for SRC clocks
43	SRCC_LR7/CR#_E	I/O	SRC7 complement or Clock Request control E for SRC6 pair The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC6 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space . After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC6 pair using byte 6, bit 7 of SMBus configuration space Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_E controls SRC6.
44	SRCT_LR7/CR#_F	I/O	SRC7 true or Clock Request control 8 for SRC8 pair The power-up default is SRC7, but this pin may also be used as a Clock Request control of SRC8 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC8 pair using byte 6, bit 6 of SMBus configuration space Byte 6, bit 6 0 = SRC7# enabled (default) 1 = CR#_F controls SRC8.
45	VDDSRCI/O	PWR	1.05V to 3.3V from external power supply
46	CPUC_ITP_LR2/SRCC8	OUT	Complement clock of low power differential CPU2/Complement clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8# 1 = ITP#
47	CPUT_ITP_LR2/SRCT8	OUT	True clock of low power differential CPU2/True clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8 1 = ITP
48	NC	N/A	No Connect
49	VDDCPU_IO	PWR	1.05V to 3.3V from external power supply
50	CPUC_F_LR1	OUT	Complement clock of low power differential CPU clock pair. This clock will be free-running during iAMT.
51	CPUT_F_LR1	OUT	True clock of low power differential CPU clock pair. This clock will be free-running during iAMT.
52	GNDCPU	PWR	Ground Pin for CPU Outputs
53	CPUC_LR0	OUT	Complement clock of low power differential CPU clock pair.
54	CPUT_LR0	OUT	True clock of low power differential CPU clock pair.
55	VDDCPU	PWR	Power Supply 3.3V nominal.
56	CK_PWRGD/PD#	IN	Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode
57	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for $V_{il\_FS}$ and $V_{ih\_FS}$ values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
58	GNDREF	PWR	Ground pin for crystal oscillator circuit
59	X2	OUT	Crystal output, nominally 14.318MHz.
60	X1	IN	Crystal input, Nominally 14.318MHz.
61	VDDREF	PWR	Power pin for the REF outputs, 3.3V nominal.
62	REF/FSLC/TEST_SEL	I/O	3.3V 14.318MHz reference clock/3.3V tolerant low threshold input for CPU frequency selection. Refer to input electrical characteristics for $V_{il\_FS}$ and $V_{ih\_FS}$ values/ TEST_SEL: 3-level latched input to enable test mode. Refer to Test Clarification Table.
63	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
64	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.



## MLF Pin Description

Pin#	Pin Name	TYPE	DESCRIPTION
1	GNDREF	PWR	Ground pin for crystal oscillator circuit
2	X2	OUT	Crystal output, nominally 14.318MHz.
3	X1	IN	Crystal input, Nominally 14.318MHz.
4	VDDREF	PWR	Power pin for the REF outputs, 3.3V nominal.
5	REF/FSLC/TEST_SEL	I/O	3.3V 14.318MHz reference clock/3.3V tolerant low threshold input for CPU frequency selection. Refer to input electrical characteristics for $V_{il\_FS}$ and $V_{ih\_FS}$ values/TEST_SEL: 3-level latched input to enable test mode. Refer to Test Clarification Table.
6	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
7	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
8	PCI0/CR#_A	I/O	3.3V PCI clock output or Clock Request control A for either SRC0 or SRC2 pair The power-up default is PCI0 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 0 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_A_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
9	VDDPCI	PWR	Power supply pin for the PCI outputs, 3.3V nominal
10	PCI1/CR#_B	I/O	3.3V PCI clock output/Clock Request control B for either SRC1 or SRC4 pair The power-up default is PCI1 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 1 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_B_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 4 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
11	PCI2/TME	I/O	3.3V PCI clock output / Trusted Mode Enable (TME) Latched Input. This pin is sampled on power-up as follows 0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed After being sampled on power-up, this pin becomes a 3.3V PCI Output
12	PCI3	OUT	3.3V PCI clock output.
13	PCI4/27_SEL	I/O	3.3V PCI clock output / 27MH mode select for pin24, 25 strap. On powerup, the logic value on this pin determines the power-up default of DOT_96/SRC0 and 27MHz/SRC1 output and the function table for the pin24 and pin25.
14	PCI5_F/ITP_EN	I/O	Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 53 and 54 are an ITP or SRC pair. 0 = SRC8/SRC8# 1 = ITP/ITP#
15	GNDPCI	PWR	Ground for PCI clocks.
16	VDD48	PWR	Power supply for USB clock, nominal 3.3V.
17	USB48M/FSLA	I/O	Fixed 48MHz USB clock output. 3.3V./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for $V_{il\_FS}$ and $V_{ih\_FS}$ values.
18	GND48	PWR	Ground pin for the 48MHz outputs.
19	VDD/O96MHz	PWR	1.05V to 3.3V from external power supply
20	DOT96T/SRCT_LR0	OUT	True clock of SRC or DOT96. The power-up default function depends on 27_Select, 1= SRC0, 0=DOT96
21	DOT96C/SRCC_LR0	OUT	Complement clock of SRC or DOT96. The power-up default function depends on 27_Select, 1= SRC0, 0=DOT96
22	GND	PWR	Ground pin for the DOT96 clocks.
23	VDD	PWR	Power supply for SRC / SE1 and SE2 clocks, 3.3V nominal.



## MLF Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
24	27FIX/LCDT/SRCT_LR1/SE1	OUT	Single-ended 3.3V 27MHz fix clock output / True clock of differential SRC1 or LCD clock pair / Single ended 3.3V peripheral clock output. The default output selection is determined by the SEL_27 default latch value. See below: <b>27_SEL=0:</b> LCD100 with -0.5% down spread is selected as default. LCD100 spread percentage can be adjusted OR output can be changed to SRC or 3.3V single-ended peripheral clock output via SMBUS B1b[4:1]. <b>27_SEL=1:</b> Single-ended 27FIX output is selected.
25	27SS/LCDC/SRCC_LR1/SE2	OUT	Single-ended 3.3V 27MHz fix clock output / Complementary clock of differential SRC1 or LCD clock pair / Single ended 3.3V peripheral clock output. The default output selection is determined by the SEL_27 default latch value. See below: <b>27_SEL=0:</b> LCD100 with -0.5% down spread is selected as default. LCD100 spread percentage can be adjusted OR output can be changed to SRC or 3.3V single-ended peripheral clock output via SMBUS B1b[4:1]. <b>27_SEL=1:</b> Single-ended 27SS output is selected with -0.5% down spread as default. Spread percentage can be adjusted via SMBUS B1b[4:1].
26	GND	PWR	Ground pin for SRC / SE1 and SE2 clocks, PLL3.
27	VDDPLL3/O	PWR	1.05V to 3.3V from external power supply
28	SRCT_LR2/SATACLKT	OUT	True clock of differential SRC/SATA clock pair.
29	SRCC_LR2/SATACLKC	OUT	Complement clock of differential SRC/SATA clock pair.
30	GNDSRC	PWR	Ground pin for SRC clocks.
31	SRCT_LR3/CR#_C	I/O	True clock of differential SRC clock pair/ Clock Request control C for either SRC0 or SRC2 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CR#_C_EN bit located in byte 5 of SMBUS address space. Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair
32	SRCC_LR3/CR#_D	I/O	Complementary clock of differential SRC clock pair/ Clock Request control D for either SRC1 or SRC4 pair The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC3 output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC3 output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CR#_D_EN bit located in byte 5 of SMBUS address space. Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default), 1 = CR#_D controls SRC4 pair
33	VDDSRCI/O	PWR	1.05V to 3.3V from external power supply
34	SRCT_LR4	I/O	True clock of differential SRC clock pair 4
35	SRCC_LR4	I/O	Complement clock of differential SRC clock pair 4
36	GNDSRC	PWR	Ground pin for SRC clocks.
37	SRCT_LR9	OUT	True clock of differential SRC clock pair.
38	SRCC_LR9	OUT	Complement clock of differential SRC clock pair.
39	SRCC_LR11/CR#_G	I/O	SRC11 complement /Clock Request control for SRC9 pair The power-up default is SRC11#, but this pin may also be used as a Clock Request control of SRC9 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC9 pair using byte 6, bit 5 of SMBus configuration space Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9

## MLF Pin Description (Continued)

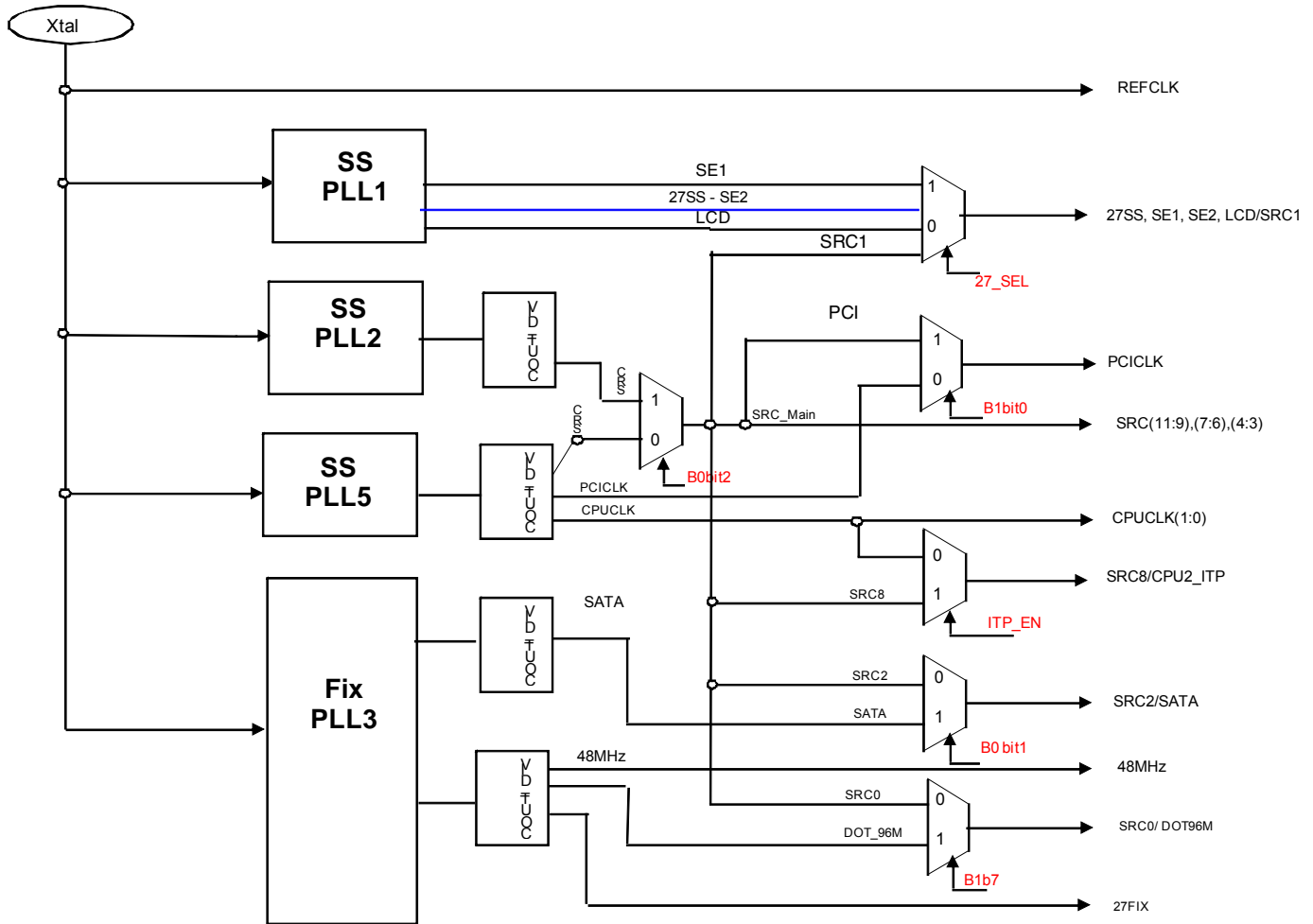
PIN #	PIN NAME	TYPE	DESCRIPTION
40	SRCT_LR11/CR#_H	I/O	SRC11 true or Clock Request control H for SRC10 pair The power-up default is SRC11, but this pin may also be used as a Clock Request control of SRC10 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC11 output pair must first be disabled in byte 3, bit 7 of SMBus configuration space After the SRC11 output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC10 pair using byte 6, bit 4 of SMBus configuration space Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10.
41	SRCT_LR10	OUT	True clock of differential SRC clock pair.
42	SRCC_LR10	OUT	Complement clock of differential SRC clock pair.
43	VDDSRC/I/O	PWR	1.05V to 3.3V from external power supply
44	CPU_STOP#	IN	Stops all CPU Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values
45	PCI_STOP#	IN	Stops all PCI Clocks, except those set to be free running clocks. In AMT mode 3 bits are shifted in from the ICH to set the FSC, FSB, FSA values
46	VDDSRC	PWR	VDD pin for SRC Pre-drivers, 3.3V nominal
47	SRCC_LR6	OUT	Complement clock of low power differential SRC clock pair.
48	SRCT_LR6	OUT	True clock of low power differential SRC clock pair.
49	GNDSRC	PWR	Ground for SRC clocks
50	SRCC_LR7/CR#_E	I/O	SRC7 complement or Clock Request control E for SRC6 pair The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC6 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space . After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC6 pair using byte 6, bit 7 of SMBus configuration space Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_E controls SRC6.
51	SRCT_LR7/CR#_F	I/O	SRC7 true or Clock Request control 8 for SRC8 pair The power-up default is SRC7, but this pin may also be used as a Clock Request control of SRC8 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC8 pair using byte 6, bit 6 of SMBus configuration space Byte 6, bit 6 0 = SRC7# enabled (default) 1 = CR#_F controls SRC8.
52	VDDSRC/I/O	PWR	1.05V to 3.3V from external power supply
53	CPUC_ITP_LR2/SRCC8	OUT	Complement clock of low power differential CPU2/Complement clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 14, PCIF5/ITP_EN on powerup. The function is as follows: Pin 14 latched input Value 0 = SRC8# 1 = ITP#
54	CPUT_ITP_LR2/SRCT8	OUT	True clock of low power differential CPU2/True clock of differential SRC pair. The function of this pin is determined by the latched input value on pin 14, PCIF5/ITP_EN on powerup. The function is as follows: Pin 14 latched input Value 0 = SRC8 1 = ITP
55	NC	N/A	No Connect
56	VDDCPU_IO	PWR	1.05V to 3.3V from external power supply
57	CPUC_F_LR1	OUT	Complement clock of low power differential CPU clock pair. This clock will be free-running during iAMT.
58	CPUT_F_LR1	OUT	True clock of low power differential CPU clock pair. This clock will be free-running during iAMT.
59	GNDCPU	PWR	Ground Pin for CPU Outputs
60	CPUC_LR0	OUT	Complement clock of low power differential CPU clock pair.
61	CPUT_LR0	OUT	True clock of low power differential CPU clock pair.
62	VDDCPU	PWR	Power Supply 3.3V nominal.
63	CK_PWRGD/PD#	IN	Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode
64	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for ViL_FS and ViH_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.



### General Description

ICS9LRS3165B follows Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for Intel processors and Intel based systems. ICS9LRS3165B is driven with a 14.318MHz crystal. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support.

### Block Diagram



### Power Groups

TSSOP Pin Number		Description
VDD	GND	
2	8	PCICLK
9	11	USB 48 & Core, FIX PLL Analog/Digital
12	15	DOT96 Output
16	19	27FIX, 27SS, LCD, SE Outputs & Core, 27SS/LCD/SE PLL Analog/Digital
20	19	SRC1 Output
26,36,45	29,42	All SRC Outputs except SRC1
39	23	SATA Output, FIX PLL Analog/Digital
39	29,42	SRC Outputs, CPU/PCIEX PLL Analog/Digital
49	52	CPU Outputs
55	52	CPU Outputs & Core
61	58	Crystal, REF Output & Core

MLF Pin Number		Description
VDD	GND	
9	15	PCICLK
16	18	USB 48 & Core, FIX PLL Analog/Digital
19	22	DOT96 Output
23	26	27FIX, 27SS, LCD, SE Outputs & Core, 27SS/LCD/SE PLL Analog/Digital
27	26	SRC1 Output
33,43,52	36,49	All SRC Outputs except SRC1
46	30	SATA Output, FIX PLL Analog/Digital
46	36,49	SRC Outputs, CPU/PCIEX PLL Analog/Digital
56	59	CPU Outputs
62	59	CPU Outputs & Core
4	1	Crystal, REF Output & Core

## Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Supply Voltage		4.6	V	1,7
Maximum Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply		3.8	V	1,7
Maximum Input Voltage	V <sub>IH</sub>	3.3V LVCMOS Inputs		4.6	V	1,7,8
Minimum Input Voltage	V <sub>IL</sub>	Any Input	GND - 0.5		V	1,7
Storage Temperature	T <sub>s</sub>	-	-65	150	°C	1,7
Case Temperature	T <sub>case</sub>			115	°C	1
Input ESD protection	ESD prot	Human Body Model	2000		V	1,7

## Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYPICAL	MAX	UNITS	Notes
Ambient Operating Temp	T <sub>ambient</sub>	-	0		70	°C	1
Supply Voltage	VDDxxx	Supply Voltage	3.135		3.465	V	1
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	1		3.465	V	1
Input High Voltage	V <sub>IHSE</sub>	Single-ended inputs	2		V <sub>DD</sub> + 0.3	V	1
Input Low Voltage	V <sub>ILSE</sub>	Single-ended inputs	V <sub>SS</sub> - 0.3		0.8	V	1
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND	-5		5	uA	1
Input Leakage Current	I <sub>INRES</sub>	Inputs with pull or pull down resistors V <sub>IN</sub> = V <sub>DD</sub> , V <sub>IN</sub> = GND	-200		200	uA	1
Output High Voltage	V <sub>OHSE</sub>	Single-ended outputs, I <sub>OH</sub> = -1mA	2.4			V	1
Output Low Voltage	V <sub>OLSE</sub>	Single-ended outputs, I <sub>OL</sub> = 1 mA			0.4	V	1
Output High Voltage	V <sub>OHDIF</sub>	Differential Outputs, I <sub>OH</sub> = TBD mA	0.7		0.9	V	1
Output Low Voltage	V <sub>OLDIF</sub>	Differential Outputs, I <sub>OL</sub> = TBD mA			0.4	V	1
Low Threshold Input-High Voltage (Test Mode)	V <sub>IH_FS_TEST</sub>	3.3 V +/-5%	2		V <sub>DD</sub> + 0.3	V	1
Low Threshold Input-High Voltage	V <sub>IH_FS</sub>	3.3 V +/-5%	0.7		1.5	V	1
Low Threshold Input-Low Voltage	V <sub>IL_FS</sub>	3.3 V +/-5%	V <sub>SS</sub> - 0.3		0.35	V	1
Operating Supply Current	I <sub>DD_DEFAULT</sub>	3.3V supply, PLL1,2 off		95	250	mA	1
	I <sub>DD_PLL3DIF</sub>	3.3V supply, PLL1,2 Differential Out		106	250	mA	1
	I <sub>DD_PLL3SE</sub>	3.3V supply, PLL1,2 Single-ended Out		101	250	mA	1
	I <sub>DD_IO</sub>	0.8V supply, Differential IO current, all outputs enabled	25	32	80	mA	1
Power Down Current	I <sub>DD_PD3.3</sub>	3.3V supply, Power Down Mode		26	30	mA	1
	I <sub>DD_PDIO</sub>	0.8V IO supply, Power Down Mode		0.23	0.5	mA	1
iAMT Mode Current	I <sub>DD_iAMT3.3</sub>	3.3V supply, iAMT Mode		47	80	mA	1
	I <sub>DD_iAMT0.8</sub>	0.8V IO supply, iAMT Mode		5	10	mA	1
Input Frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V			14.318	MHz	2
Pin Inductance	L <sub>pin</sub>				7	nH	1
Input Capacitance	C <sub>IN</sub>	Logic Inputs	1.5		5	pF	1
	C <sub>OUT</sub>	Output pin capacitance			6	pF	1
	C <sub>INX</sub>	X1 & X2 pins			5	pF	1
Spread Spectrum Modulation Frequency	f <sub>SSMOD</sub>	Triangular Modulation	30		33	kHz	1

**Electrical Characteristics - SMBus Interface**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	$V_{DD}$		2.7	5.5	V	1
Low-level Output Voltage	$V_{OL\text{SMB}}$	@ $I_{PULLUP}$		0.4	V	1
Current sinking at $V_{OL\text{SMB}} = 0.4\text{ V}$	$I_{PULLUP}$	SMB Data Pin	4		mA	1
SCLK/SDATA Clock/Data Rise Time	$T_{RI2C}$	(Max $V_{IL} - 0.15$ ) to (Min $V_{IH} + 0.15$ )		1000	ns	1
SCLK/SDATA Clock/Data Fall Time	$T_{FI2C}$	(Min $V_{IH} + 0.15$ ) to (Max $V_{IL} - 0.15$ )		300	ns	1
Maximum SMBus Operating Frequency	$F_{SMBUS}$	Block Mode		100	kHz	1

**AC Electrical Characteristics - Low Power Differential Outputs**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	$t_{SLR}$	Differential Measurement	2.5	8	V/ns	1,2
Falling Edge Slew Rate	$t_{FLR}$	Differential Measurement	2.5	8	V/ns	1,2
Slew Rate Variation	$t_{SLVAR}$	Single-ended Measurement		20	%	1
Maximum Output Voltage	$V_{HIGH}$	Includes overshoot		1150	mV	1
Minimum Output Voltage	$V_{LOW}$	Includes undershoot	-300		mV	1
Differential Voltage Swing	$V_{SWING}$	Differential Measurement	300		mV	1
Crossing Point Voltage	$V_{XABS}$	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	$V_{XABS\text{VAR}}$	Single-ended Measurement		140	mV	1,3,5
Duty Cycle	$D_{CYC}$	Differential Measurement	45	55	%	1
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		85	ps	1
SRC0 Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		125	ps	1
SRC[11:1] Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		85	ps	1
SATA Jitter - Cycle to Cycle	$SATAJ_{C2C}$	Differential Measurement		125	ps	1
DOT Jitter - Cycle to Cycle	$DOTJ_{C2C}$	Differential Measurement		250	ps	1
CPU[1:0] Skew	$CPU_{SKEW10}$	Differential Measurement		100	ps	1
CPU[2:ITP:0] Skew	$CPU_{SKEW20}$	Differential Measurement		150	ps	1
SRC[11,7,4,2,0] Skew	$SRC_{SKEW}$	Differential Measurement	0 nominal		ps	1
SRC[10,9,8,6,3] Skew	$SRC_{SKEW}$	Differential Measurement		3	ns	1

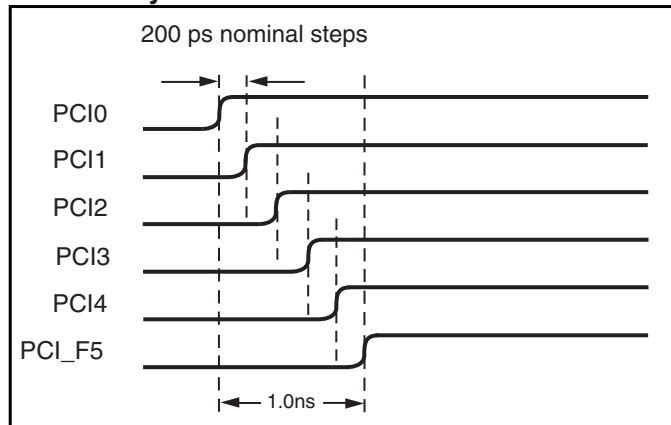
\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs= 0Ω, CL = 2pF

**AC Electrical Characteristics - Input/Common Parameters**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	$T_{STAB}$	From VDD Power-Up or de-assertion of PD# to 1st clock		1.8	ms	1
Tdrive_SRC	$T_{DRSRC}$	SRC output enable after PCI_STOP# de-assertion		15	ns	1
Tdrive_PD#	$T_{DRPD}$	Differential output enable after PD# de-assertion		300	us	1
Tdrive_CPU	$T_{DRSRC}$	CPU output enable after CPU_STOP# de-assertion		10	ns	1
Tfall_PD#	$T_{FALL}$	Fall/rise time of PD#, PCI_STOP# and CPU_STOP# inputs		5	ns	1
Trise_PD#	$T_{RISE}$			5	ns	1

**Electrical Characteristics - PCICLK/PCICLK\_F**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-300	300	ppm	1,6
Clock period	$T_{\text{period}}$	33.33MHz output nominal	29.99100	30.00900	ns	6
		33.33MHz output spread		30.15980	ns	6
Absolute min/max period	$T_{\text{abs}}$	33.33MHz output nominal/spread	29.49100	30.65980	ns	6
Output High Voltage	$V_{\text{OH}}$	$I_{\text{OH}} = -1 \text{ mA}$	2.4		V	1
Output Low Voltage	$V_{\text{OL}}$	$I_{\text{OL}} = 1 \text{ mA}$		0.4	V	1
Output High Current	$I_{\text{OH}}$	$V_{\text{OH}} @ \text{MIN} = 1.0 \text{ V}$	-33		mA	1
		$V_{\text{OH}} @ \text{MAX} = 3.135 \text{ V}$		-33	mA	1
Output Low Current	$I_{\text{OL}}$	$V_{\text{OL}} @ \text{MIN} = 1.95 \text{ V}$	30		mA	1
		$V_{\text{OL}} @ \text{MAX} = 0.4 \text{ V}$		38	mA	1
Rising Edge Slew Rate	$t_{\text{SLR}}$	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	$t_{\text{FLR}}$	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	$d_{\text{t1}}$	$V_{\text{T}} = 1.5 \text{ V}$	45	55	%	1
Skew	$t_{\text{skew}}$	$V_{\text{T}} = 1.5 \text{ V}$		250	ps	1
Intentional PCI-PCI delay	$t_{\text{delay}}$	$V_{\text{T}} = 1.5 \text{ V}$	200 nominal		ps	1,9
Jitter, Cycle to cycle	$t_{\text{jyc-cyc}}$	$V_{\text{T}} = 1.5 \text{ V}$		500	ps	1

**Intentional PCI Clock to Clock Delay****Electrical Characteristics - USB48MHz**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	1,6
Clock period	$T_{\text{period}}$	48.00MHz output nominal	20.83125	20.83542	ns	6
Absolute min/max period	$T_{\text{abs}}$	48.00MHz output nominal	20.48130	21.18540	ns	6
Output High Voltage	$V_{\text{OH}}$	$I_{\text{OH}} = -1 \text{ mA}$	2.4		V	1
Output Low Voltage	$V_{\text{OL}}$	$I_{\text{OL}} = 1 \text{ mA}$		0.4	V	1
Output High Current	$I_{\text{OH}}$	$V_{\text{OH}} @ \text{MIN} = 1.0 \text{ V}$	-29		mA	1
		$V_{\text{OH}} @ \text{MAX} = 3.135 \text{ V}$		-23	mA	1
Output Low Current	$I_{\text{OL}}$	$V_{\text{OL}} @ \text{MIN} = 1.95 \text{ V}$	29		mA	1
		$V_{\text{OL}} @ \text{MAX} = 0.4 \text{ V}$		27	mA	1
Rising Edge Slew Rate	$t_{\text{SLR}}$	Measured from 0.8 to 2.0 V	1	2	V/ns	1
Falling Edge Slew Rate	$t_{\text{FLR}}$	Measured from 2.0 to 0.8 V	1	2	V/ns	1
Duty Cycle	$d_{\text{t1}}$	$V_{\text{T}} = 1.5 \text{ V}$	45	55	%	1
Jitter, Cycle to cycle	$t_{\text{jyc-cyc}}$	$V_{\text{T}} = 1.5 \text{ V}$		350	ps	1

**Electrical Characteristics - 27MHz\_Spread / 27MHz\_NonSpread**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50		50	ppm	1,6
			-15		15		6
Clock period	$T_{period}$	27.000MHz output nominal	37.0365		37.0376	ns	6
Output High Voltage	$V_{OH}$	$I_{OH} = -1 \text{ mA}$	2.4			V	1
Output Low Voltage	$V_{OL}$	$I_{OL} = 1 \text{ mA}$			0.55	V	1
Output High Current	$I_{OH}$	$V_{OH} @ \text{MIN} = 1.0 \text{ V}$	-29			mA	1
		$V_{OH} @ \text{MAX} = 3.135 \text{ V}$			-23	mA	1
Output Low Current	$I_{OL}$	$V_{OL} @ \text{MIN} = 1.95 \text{ V}$	29			mA	1
		$V_{OL} @ \text{MAX} = 0.4 \text{ V}$			27	mA	1
Edge Rate	$t_{slew/f}$	Rising/Falling edge rate	1		4	V/ns	1
Rise Time	$t_{r1}$	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$	0.5		2	ns	1
Fall Time	$t_{f1}$	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$	0.5		2	ns	1
Duty Cycle	$d_{11}$	$V_T = 1.5 \text{ V}$	45		55	%	1
Jitter	$t_{tj}$	Long Term (10us), $V_T = 1.5 \text{ V}$			800	ps	1
	$t_{pk-pk}$	$V_T = 1.5 \text{ V}$	-200		200	ps	1
	$t_{cyc-cyc}$	$V_T = 1.5 \text{ V}$			200	ps	1

**Electrical Characteristics - REF-14.318MHz**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300	300	ppm	1,6
Clock period	$T_{period}$	14.318MHz output nominal	69.8203	69.8622	ns	6
Absolute min/max period	$T_{abs}$	14.318MHz output nominal	69.8203	70.86224	ns	6
Output High Voltage	$V_{OH}$	$I_{OH} = -1 \text{ mA}$	2.4		V	1
Output Low Voltage	$V_{OL}$	$I_{OL} = 1 \text{ mA}$		0.4	V	1
Output High Current	$I_{OH}$	$V_{OH} @ \text{MIN} = 1.0 \text{ V},$ $V_{OH} @ \text{MAX} = 3.135 \text{ V}$	-33	-33	mA	1
Output Low Current	$I_{OL}$	$V_{OL} @ \text{MIN} = 1.95 \text{ V},$ $V_{OL} @ \text{MAX} = 0.4 \text{ V}$	30	38	mA	1
Rising Edge Slew Rate	$t_{SLR}$	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	$t_{FLR}$	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	$d_{11}$	$V_T = 1.5 \text{ V}$	45	55	%	1
Jitter	$t_{jyc-cyc}$	$V_T = 1.5 \text{ V}$		1000	ps	1

**Electrical Characteristics - Differential Jitter Parameters**

PARAMETER	Symbol	Conditions	Min	TYP	Max	Units	Notes
Jitter, Phase	$t_{jphasePLL}$	PCIe Gen 1			86	ps (p-p)	1,11
	$t_{jphaseLo}$	PCIe Gen 2 10kHz < f < 1.5MHz			3	ps (RMS)	1,11
	$t_{jphaseHigh}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)			3.1	ps (RMS)	1,11

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs= 0Ω, CL = 2pF

**Notes on Electrical Characteristics:**

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Slew rate measured through Vswing centered around differential zero

<sup>3</sup>Vxabs is defined as the voltage where CLK = CLK#

<sup>4</sup>Only applies to the differential rising edge (CLK rising and CLK# falling)

<sup>5</sup>Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#. The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>6</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

<sup>7</sup>Operation under these conditions is neither implied, nor guaranteed.

<sup>8</sup>Maximum input voltage is not to exceed maximum VDD

<sup>9</sup>See PCI Clock-to-Clock Delay Figure

<sup>10</sup>At nominal voltage and temperature



Table 1: CPU Frequency Select Table

FS <sub>L</sub> C <sup>2</sup> B0b7	FS <sub>L</sub> B <sup>1</sup> B0b6	FS <sub>L</sub> A <sup>1</sup> B0b5	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266.66	100.00	33.33	14.318	48.00	96.00
0	0	1	133.33					
0	1	0	200.00					
0	1	1	166.66					
1	0	0	333.33					
1	0	1	100.00					
1	1	0	400.00					
1	1	1	Reserved					

1. FS<sub>L</sub>A and FS<sub>L</sub>B are low-threshold inputs. Please see V<sub>IL\_FS</sub> and V<sub>IH\_FS</sub> specifications in the Input/Supply/Common Output Parameters Table for correct values.

Also refer to the Test Clarification Table.

2. FS<sub>L</sub>C is a three-level input. Please see the V<sub>IL\_FS</sub> and V<sub>IH\_FS</sub> specifications in the Input/Supply/Common Output Parameters Table for correct values.

Table 2: 27FIX/LCDT/SRCT\_LR1/SE1, 27SS/LCDC/SRCC\_LR1/SE2 Configuration

27_SEL	B1b4	B1b3	B1b2	B1b1	27FIX/LCDT/SRCT_LR1/SE1	27SS/LCDC/SRCC_LR1/SE2	Spread %	Comment
					MHz	MHz		
0	0	0	0	0				PLL1 & PLL2 disabled
0	0	0	0	1	100.00	100.00		SRCCLK1 from SRC_MAIN
0	0	0	1	0	100.00	100.00	-0.50%	LCDCLK from PLL1
0	0	0	1	1	100.00	100.00	-1%	LCDCLK from PLL1
0	0	1	0	0	100.00	100.00	-1.50%	LCDCLK from PLL1
0	0	1	0	1	100.00	100.00	+/-0.25%	LCDCLK from PLL1
0	0	1	1	0	100.00	100.00	+/-0.5%	LCDCLK from PLL1
0	0	1	1	1	N/A	N/A	N/A	N/A
0	1	0	0	0	24.576	24.576	None	24.576Mhz on SE1 and SE2
0	1	0	0	1	24.576	98.304	None	24.576Mhz on SE1, 98.304Mhz on SE2
0	1	0	1	0	98.304	98.304	None	98.304Mhz on SE1 and SE2
0	1	0	1	1	27.000	27.000	None	27Mhz on SE1 and SE2
0	1	1	0	0	25.000	25.000	None	25Mhz on SE1 and SE2
0	1	1	0	1				N/A
0	1	1	1	0	N/A	N/A	N/A	N/A
0	1	1	1	1	N/A	N/A	N/A	N/A
1	0	0	0	0	N/A	N/A	N/A	
1	0	0	0	1	N/A	N/A	N/A	
1	0	0	1	0	27MHz_nonSS	27MHz_SS	-0.5%	
1	0	0	1	1	27MHz_nonSS	27MHz_SS	-1%	
1	0	1	0	0	27MHz_nonSS	27MHz_SS	-1.5%	
1	0	1	0	1	27MHz_nonSS	27MHz_SS	-2%	
1	0	1	1	0	27MHz_nonSS	27MHz_SS	-0.75%	
1	0	1	1	1	27MHz_nonSS	27MHz_SS	-1.25%	
1	1	0	0	0	27MHz_nonSS	27MHz_SS	-1.75%	
1	1	0	0	1	27MHz_nonSS	27MHz_SS	+0.5%	
1	1	0	1	0	27MHz_nonSS	27MHz_SS	+0.75%	
1	1	0	1	1	N/A	N/A		
1	1	1	0	0	N/A	N/A		
1	1	1	0	1	N/A	N/A		
1	1	1	1	0	N/A	N/A		
1	1	1	1	1	N/A	N/A		

Note: Mode 00000 ~ 00110 on Table 2 only applies when SRC\_MAIN source is from PLL5.

Table 3: IO\_Vout select table

B9b2	B9b1	B9b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

Table 4: Device ID table

B8b7	B8b6	B8b5	B8b4	Comment
0	0	0	0	64 pin MLF
0	0	0	1	64 pin TSSOP
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

CPU Power Management Table

PD#	CPU_STOP#	PCI_STOP#	PEREQ#	SMBus Register OE	CPU0	CPU0#	CPU1	CPU1#	CPU2	CPU2#
1	1	1	X	Enable	Running	Running	Running	Running	Running	Running
0	X	X	X	Enable	Low/20K	Low	Low/20K	Low	Low/20K	Low
1	0	X	X	Enable	High	Low	High	Low	High	Low
1	X	X	X	Disable	Low/20K	Low	Low/20K	Low	Low/20K	Low
M1					Low/20K	Low	Running	Running	Low/20K	Low

PCIEX, LCD Power Management Table

PD#	CPU_STOP#	PCI_STOP#	PEREQ#	SMBus Register OE	PCIeT	PCIeC	PCIeT	PCIeC	LCD	LCD #	LCD	LCD #	SATA	SATA#	SATA	SATA#
					Free-Run		Stoppable		Free-Run		Stoppable		Free-Run		Stoppable	
1	X	1	0	Enable	Running	Running	Running	Running	Running	Running	Running	Running	Running	Running	Running	Running
0	X	X	X	Enable	Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low
1	X	0	0	Enable	Running	Running	High	Low	Running	Running	High	Low	Running	Running	High	Low
1	X	X	1	Enable	Running	Running	Low/20K	Low	Running	Running	Running	Running	Running	Running	Running	Running
1	X	X	X	Disable	Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low
M1					Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low	Low/20K	Low

DOT, SATA Power Management Table

PD#	CPU_STOP#	PCI_STOP#	PEREQ#	SMBus Register OE	DOT	DOT#
1	X	1	X	Enable	Running	Running
0	X	X	X	Enable	Low/20K	Low
1	X	0	X	Enable	Running	Running
1	X	X	X	Enable	Running	Running
1	X	X	X	Disable	Low/20K	Low
M1					Low/20K	Low

Single-ended Power Management Table

PD#	CPU_STOP#	PCI_STOP#	PEREQ#	SMBus Register OE	PCIF/PCI	PCIF/PCI	USB48	REF	27M	SE
					Free-Run	Stoppable				
1	X	1	X	Enable	Running	Running	Running	Running	Running	Running
0	X	X	X	Enable	Low	Low	Low	Low	Low	Low
1	X	0	X	Enable	Running	Low	Running	Running	Running	Running
1	X	X	X	Disable	Low	Low	Low	Low	Low	Low
M1					Low	Low	Low	Low	Low	Low

## General SMBus serial interface information for the ICS9LRS3165B

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $D2_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $D2_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $D3_{(H)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if  $X_{(H)}$  was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation		
Controller (Host)		ICS (Slave/Receiver)
T	start bit	
Slave Address $D2_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N		X Byte
○		
○		
○		
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation		
Controller (Host)		ICS (Slave/Receiver)
T	start bit	
Slave Address $D2_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat start	
Slave Address $D3_{(H)}$		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		X Byte
ACK		
○		
○		
○		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

**Byte 0 FS Readback & PLL Selection Register**

Bit	Name	Description	Type	0	1	Default	
7	FSLC	CPU Freq. Sel. Bit (Most Significant)	R	See Table 1 : CPU Frequency Select Table		Latch	
6	FSLB	CPU Freq. Sel. Bit	R				Latch
5	FSLA	CPU Freq. Sel. Bit (Least Significant)	R				Latch
4	iAMT_EN	Set via SMBus or dynamically by CK505 if detects dynamic M1	R	Legacy Mode	iAMT Enabled	iAMT power on status	
3	Reserved	Reserved	RW			0	
2	SRC_Main_SEL	Select source for SRC Main	RW	SRC Main = PLL5	SRC Main = PLL2	0	
1	SATA_SEL	Select source for SATA clock	RW	SATA = SRC_Main	SATA = PLL3	0	
0	PD_Restore	1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at '1' if device is in iAMT mode.	RW	Configuration Not Saved	Configuration Saved	1	

**Byte 1 PLL1 Quick Config Register**

Note 1 : When 27\_Select pin = 0, B1b7 PWD = 1; When 27\_Select pin = 1, PWD = 0

Bit	Name	Description	Type	0	1	Default
7	SRC0_SEL	Select SRC0 or DOT96	RW	SRC0	DOT96	Note 1
6	PLL5_SSC_SEL	Select 0.5% down or center SSC	RW	Down spread	Center spread	0
5	PLL2_SSC_SEL	Select 0.5% center or down SSC	RW	Down	Center	0
4	PLL1_CF3	PLL1 Quick Config Bit 3	RW	See Table 2: pin 27FIX/LCDT/SRCT_LR1/SE1, 27SS/LCDC/SRCC_LR1/SE2 Configuration Only applies if Byte 0, bit 2 = 0.		0
3	PLL1_CF2	PLL1 Quick Config Bit 2	RW			0
2	PLL1_CF1	PLL1 Quick Config Bit 1	RW			1
1	PLL1_CF0	PLL1 Quick Config Bit 0	RW			0
0	PCI_SEL	PCI_SEL	RW	PCI from PLL5	PCI from SRC_MAIN	1

**Byte 2 Single Ended Output Enable Register**

Bit	Name	Description	Type	0	1	Default
7	REF_OE	Output enable for REF	RW	Output Disabled	Output Enabled	1
6	USB_OE	Output enable for USB	RW	Output Disabled	Output Enabled	1
5	PCIF5_OE	Output enable for PCIF5	RW	Output Disabled	Output Enabled	1
4	PCI4_OE	Output enable for PCI4	RW	Output Disabled	Output Enabled	1
3	PCI3_OE	Output enable for PCI3	RW	Output Disabled	Output Enabled	1
2	PCI2_OE	Output enable for PCI2	RW	Output Disabled	Output Enabled	1
1	PCI1_OE	Output enable for PCI1	RW	Output Disabled	Output Enabled	1
0	PCI0_OE	Output enable for PCI0	RW	Output Disabled	Output Enabled	1

**Byte 3 SRC Output Enable Register**

Bit	Name	Description	Type	0	1	Default
7	SRC11_OE	Output enable for SRC11	RW	Output Disabled	Output Enabled	1
6	SRC10_OE	Output enable for SRC10	RW	Output Disabled	Output Enabled	1
5	SRC9_OE	Output enable for SRC9	RW	Output Disabled	Output Enabled	1
4	SRC8/ITP_OE	Output enable for SRC8 or ITP	RW	Output Disabled	Output Enabled	1
3	SRC7_OE	Output enable for SRC7	RW	Output Disabled	Output Enabled	1
2	SRC6_OE	Output enable for SRC6	RW	Output Disabled	Output Enabled	1
1	Reserved	Reserved	RW	-	-	1
0	SRC4_OE	Output enable for SRC4	RW	Output Disabled	Output Enabled	1

**Byte 4 SRC/CPU/DOT Output Enable & Spread Spectrum Disable Register**

Bit	Name	Description	Type	0	1	Default
7	SRC3_OE	Output enable for SRC3	RW	Output Disabled	Output Enabled	1
6	SATA/SRC2_OE	Output enable for SATA/SRC2	RW	Output Disabled	Output Enabled	1
5	SRC1_OE	Output enable for SRC1	RW	Output Disabled	Output Enabled	1
4	SRC0/DOT96_OE	Output enable for SRC0/DOT96	RW	Output Disabled	Output Enabled	1
3	CPU1_OE	Output enable for CPU1	RW	Output Disabled	Output Enabled	1
2	CPU0_OE	Output enable for CPU0	RW	Output Disabled	Output Enabled	1
1	PLL5_SSC_ON	Enable PLL5's spread modulation	RW	Spread Disabled	Spread Enabled	1
0	PLL2_SSC_ON	Enable PLL2's spread modulation	RW	Spread Disabled	Spread Enabled	1

**Byte 5 Clock Request Enable/Configuration Register**

Bit	Name	Description	Type	0	1	Default
7	CR#_A_EN	Enable CR#_A (clk req) for SRC0 or SRC2	RW	Disable CR#_A	Enable CR#_A	0
6	CR#_A_SEL	Sets CR#_A to control either SRC0 or SRC2	RW	CR#_A -> SRC0	CR#_A -> SRC2	0
5	CR#_B_EN	Enable CR#_B (clk req) for SRC1 or SRC4	RW	Disable CR#_B	Enable CR#_B	0
4	CR#_B_SEL	Sets CR#_B to control either SRC1 or SRC4	RW	CR#_B -> SRC1	CR#_B -> SRC4	0
3	CR#_C_EN	Enable CR#_C (clk req) for SRC0 or SRC2	RW	Disable CR#_C	Enable CR#_C	0
2	CR#_C_SEL	Sets CR#_C to control either SRC0 or SRC2	RW	CR#_C -> SRC0	CR#_C -> SRC2	0
1	CR#_D_EN	Enable CR#_D (clk req) for SRC1 or SRC4	RW	Disable CR#_D	Enable CR#_D	0
0	CR#_D_SEL	Sets CR#_D to control either SRC1 or SRC4	RW	CR#_D -> SRC1	CR#_D -> SRC4	0

## Byte 6 Clock Request Enable/Configuration Register

Bit	Name	Description	Type	0	1	Default
7	CR#_E_EN	Enable CR#_E (clk req) for SRC6	RW	Disable CR#_E	Enable CR#_E	0
6	CR#_F_EN	Enable CR#_F (clk req) for SRC8	RW	Disable CR#_F	Enable CR#_F	0
5	CR#_G_EN	Enable CR#_G (clk req) for SRC9	RW	Disable CR#_G	Enable CR#_G	0
4	CR#_H_EN	Enable CR#_H (clk req) for SRC10	RW	Disable CR#_H	Enable CR#_H	0
3	Reserved	Reserved	RW	-	-	0
2	Reserved	Reserved	RW	-	-	0
1	LCD/SRC1_STP_CTRL*	If set, LCD_SS/SRC1 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
0	SRC0_STP_CTRL	If set, SRC0 stop with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0

## Byte 7 Vendor ID/ Revision ID Register

Bit	Name	Description	Type	0	1	Default
7	Rev Code Bit 3	Revision ID	R	Vendor specific		0
6	Rev Code Bit 2		R			0
5	Rev Code Bit 1		R			0
4	Rev Code Bit 0		R			1
3	Vendor ID bit 3	Vendor ID ICS is 0001, binary	R			0
2	Vendor ID bit 2		R			0
1	Vendor ID bit 1		R			0
0	Vendor ID bit 0		R			1

## Byte 8 Device ID &amp; Output Enable Register

Bit	Name	Description	Type	0	1	Default (TSSOP)	Default (MLF)
7	Device_ID3	Table of Device identifier codes, used for differentiating between CK505 package options, etc.	R	See Device ID Table 4		0	0
6	Device_ID2		R			0	0
5	Device_ID1		R			0	0
4	Device_ID0		R			1	0
3	Reserved	Reserved	RW	-	-	0	0
2	Reserved	Reserved	RW	-	-	0	0
1	27MHz_nonSS/SE1_OE	Output enable for SE1	RW	Disabled	Enabled	1	1
0	27MHz_SS/SE2_OE	Output enable for SE2	RW	Disabled	Enabled	1	1

## Byte 9 Test and Output Control Register

Bit	Name	Description	Type	0	1	Default
7	PCIF5_STOP_EN	Allows control of PCIF5 with assertion of PCI_STOP#	RW	Free running	Stops with PCI_STOP# assertion	0
6	TME_Readback	Trusted Mode Enable (TME) strap status	R	normal operation	no overclocking	TME latch
5	Reserved	Reserved	RW	-	-	1
4	Test Mode Select	Allows test select, ignores REF/FSC/TestSel	RW	Outputs HI-Z	Outputs = REF/N	0
3	Test Mode Entry	Allows entry into test mode, ignores FSB/TestMode	RW	Normal operation	Test mode	0
2	CPU_IO_VOUT2	CPU IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
1	CPU_IO_VOUT1	CPU IO Output Voltage Select	RW			0
0	CPU_IO_VOUT0	CPU IO Output Voltage Select (Least Significant Bit)	RW			1

## Byte 10 Output Control Register

Bit	Name	Description	Type	0	1	Default
7	27_SEL_Latch_Readback	Readback of 27_Select latch	R	Dot96/ LCD_SS/SE	SRC0/ 27MHz	27_SEL latch
6	PCI4_STOP_EN	Allows control of PCI4 with assertion of PCI_STOP#	RW	Free running	Stops with PCI_STOP# assertion	1
5	PCI3_STOP_EN	Allows control of PCI3 with assertion of PCI_STOP#	RW	Free running	Stops with PCI_STOP# assertion	1
4	PCI2_STOP_EN	Allows control of PCI2 with assertion of PCI_STOP#	RW	Free running	Stops with PCI_STOP# assertion	1
3	PCI1_STOP_EN	Allows control of PCI1 with assertion of PCI_STOP#	RW	Free running	Stops with PCI_STOP# assertion	1
2	PCI0_STOP_EN	Allows control of PCI0 with assertion of PCI_STOP#	RW	Free running	Stops with PCI_STOP# assertion	1
1	CPU1 Stop Enable	Enables control of CPU1 with CPU_STOP#	RW	Free Running	Stoppable	1
0	CPU0 Stop Enable	Enables control of CPU0 with CPU_STOP#	RW	Free Running	Stoppable	1



## Byte 11 iAMT/CPU2 Control Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	0
6	Reserved	Reserved	RW	-	-	0
5	Reserved	Reserved	RW	-	-	0
4	Reserved	Reserved	RW	-	-	0
3	CPU2_AMT_EN	M1 mode clk enable, only if ITP_EN=1	RW	Disable	Enable	0
2	CPU1_AMT_EN	M1 mode clk enable	RW	Disable	Enable	1
1	Reserved	Reserved	RW	-	-	0
0	CPU2 Stop Enable	Enables control of CPU2 with CPU_STOP#	RW	Free Running	Stoppable	1

## Byte 12 Byte Count Register

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	0
6	Reserved	Reserved	RW	-	-	0
5	BC5	Read Back byte count register, max bytes = 32	RW	-	-	0
4	BC4		RW	-	-	0
3	BC3		RW	-	-	1
2	BC2		RW	-	-	1
1	BC1		RW	-	-	0
0	BC0		RW	-	-	1

## Byte 13 Single Ended Output Slew Rate Control Register

Bit	Name	Description	RW	0	1	Default
7	REF	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
6	REF		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
5	27M_FIX	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
4	27M_FIX		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
3	27M_SS	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
2	27M_SS		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
1	Reserved	Reserved	RW	-	-	0
0	Reserved	Reserved	RW	-	-	0

## Byte 14 Reserved

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	X
6	Reserved	Reserved	RW	-	-	X
5	Reserved	Reserved	RW	-	-	X
4	Reserved	Reserved	RW	-	-	X
3	Reserved	Reserved	RW	-	-	X
2	Reserved	Reserved	RW	-	-	X
1	Reserved	Reserved	RW	-	-	X
0	Reserved	Reserved	RW	-	-	X

## Byte 15 Reserved

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	X
6	Reserved	Reserved	RW	-	-	X
5	Reserved	Reserved	RW	-	-	X
4	Reserved	Reserved	RW	-	-	X
3	Reserved	Reserved	RW	-	-	X
2	Reserved	Reserved	RW	-	-	X
1	Reserved	Reserved	RW	-	-	X
0	Reserved	Reserved	RW	-	-	X

## Byte 16 Reserved

Bit	Name	Description	Type	0	1	Default
7	Reserved	Reserved	RW	-	-	X
6	Reserved	Reserved	RW	-	-	X
5	Reserved	Reserved	RW	-	-	X
4	Reserved	Reserved	RW	-	-	X
3	Reserved	Reserved	RW	-	-	X
2	Reserved	Reserved	RW	-	-	X
1	Reserved	Reserved	RW	-	-	X
0	Reserved	Reserved	RW	-	-	X

**Byte 17 SRC Output Control Register**

Bit	Name	Description	RW	0	1	Default
7	SATA/SRC2_STP_CTRL	If set, SATA/SRC2 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
6	SRC3_STP_CTRL	If set, SRC3 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
5	SRC4_STP_CTRL	If set, SRC4 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
4	SRC6_STP_CTRL	If set, SRC6 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
3	SRC7_STP_CTRL	If set, SRC7 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
2	Reserved	Reserved	RW	-	-	0
1	SRC8_STP_CTRL	If set, SRC8 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
0	SRC9_STP_CTRL	If set, SRC9 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0

**Byte 18 Differential Output Control Register**

Bit	Name	Description	RW	0	1	Default
7	SRC10_STP_CTRL	If set, SRC10 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
6	SRC11_STP_CTRL	If set, SRC11 stops with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0
5	SRC/CPUITP_SRC8 IO_VOUT2	SRC & CPUITP_SRC8 IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
4	SRC/CPUITP_SRC8 IO_VOUT1	SRC IO & CPUITP_SRC8 Output Voltage Select	RW			0
3	SRC/CPUITP_SRC8 IO_VOUT0	SRC & CPUITP_SRC8 IO Output Voltage Select (Least Significant Bit)	RW			1
2	SATA/SRC2 IO_VOUT2	SATA_SRC2 IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
1	SATA/SRC2 IO_VOUT1	SATA_SRC2 IO Output Voltage Select	RW			0
0	SATA/SRC2 IO_VOUT0	SATA_SRC2 IO Output Voltage Select (Least Significant Bit)	RW			1

**Byte 19 Differential Output Control Register**

Bit	Name	Description	RW	0	1	Default
7	LCD_SS (SRC1) IO_VOUT2	LCD_SS IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
6	LCD_SS (SRC1) IO_VOUT1	LCD_SS IO Output Voltage Select	RW			0
5	LCD_SS (SRC1) IO_VOUT0	LCD_SS IO Output Voltage Select (Least Significant Bit)	RW			1
4	SRC0/DOT96 IO_VOUT2	SRC0_DOT96 IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
3	SRC0/DOT96 IO_VOUT1	SRC0_DOT96 IO Output Voltage Select	RW			0
2	SRC0/DOT96 IO_VOUT0	SRC0_DOT96 IO Output Voltage Select (Least Significant Bit)	RW			1
1	Reserved	Reserved	RW	-	-	0
0	Reserved	Reserved	RW	-	-	0

**Byte 20 Single Ended Slew Rate Control Register**

Bit	Name	Description	Type	0	1	Default
7	48MHz	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
6	48MHz		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
5	PCI5	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
4	PCI5		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
3	PCI4	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
2	PCI4		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
1	PCI3	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
0	PCI3		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1

**Byte 21 Single Ended Slew Rate & M/N Enable Control Register**

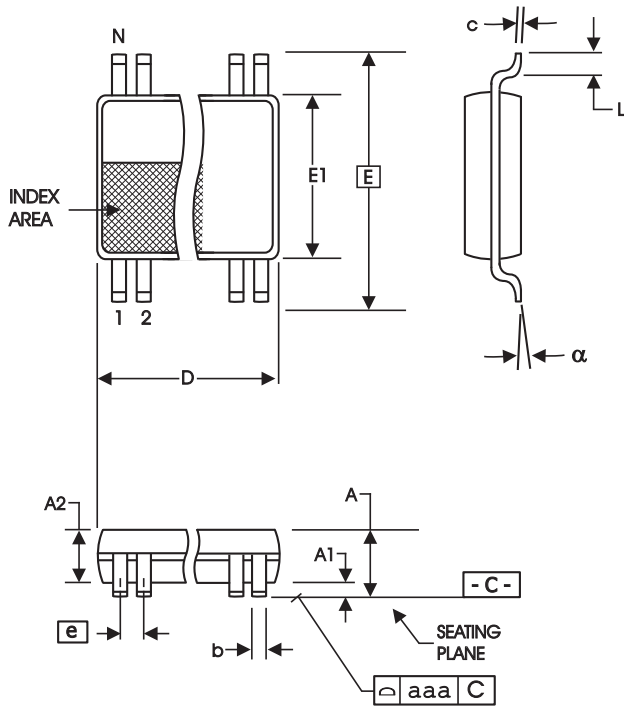
Bit	Name	Description	Type	0	1	Default
7	PCI2	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
6	PCI2		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
5	PCI1	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
4	PCI1		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
3	PCI0	Slew Rate Control	RW	00 = Hi-Z	01 = 1.4 V/ns	0
2	PCI0		RW	10 = 2.0 V/ns	11 = 2.4 V/ns	1
1	Reserved	Reserved	RW	-	-	0
0	Reserved	Reserved	RW	-	-	0

**Test Clarification Table**

Comments	HW		SW		OUTPUT
	FSLC/ TEST_SEL HW PIN	FSLB/ TEST_MODE HW PIN	TEST ENTRY BIT B9b3	REF/N or HI-Z B9b4	
	<2.0V	X	0	0	NORMAL
CK_PWRG=1 w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode FSLC./TEST_SEL -->3-level latched input If CK_PWRG=1 w/ V>2.0V then use TEST_SEL If CK_PWRG=1 w/ V<2.0V then use FSLC FSLB/TEST_MODE -->low Vth input TEST_MODE is a real time input	>2.0V	0	X	0	HI-Z
	>2.0V	0	X	1	REF/N
	>2.0V	1	X	0	REF/N
	>2.0V	1	X	1	REF/N
If TEST_SEL HW pin is 0 after CK_PWRG=1, test mode can be invoked through B9b3. If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N FSLB/TEST_Mode pin is not used. Cycle power to disable test mode, one shot control	<2.0V	X	1	0	HI-Z
	<2.0V	X	1	1	REF/N

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B9b4: 1= REF/N, Default = 0 (HI-Z)



6.10 mm. Body, 0.50 mm. Pitch TSSOP  
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
alpha	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

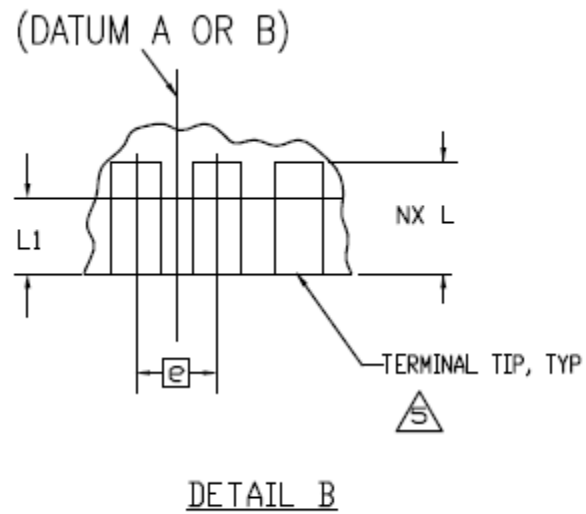
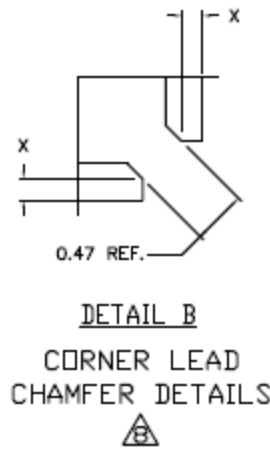
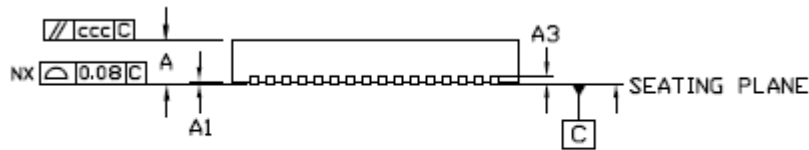
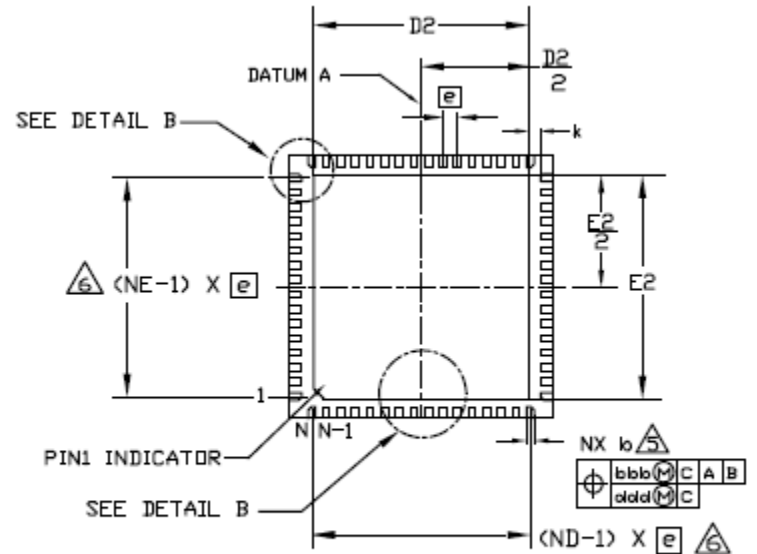
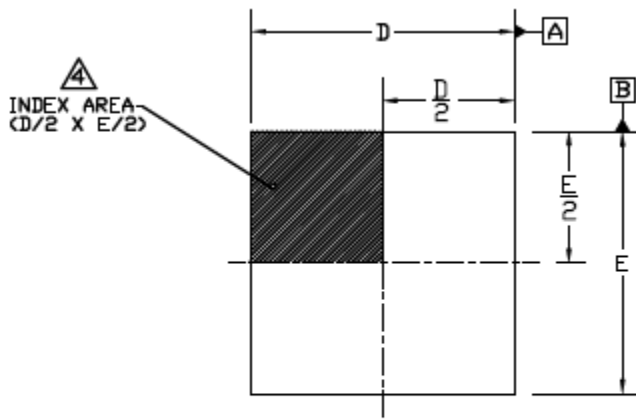
N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

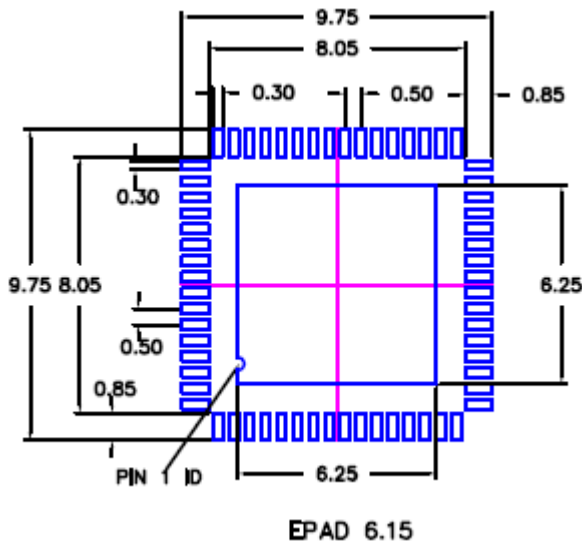


MLF Package Drawing and Dimensions (cont.)





## MLF Package Drawing and Dimensions (cont.)



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	1.00	31	33	39
A1	0.00	0.02	0.05	0	1	2
A2	–	0.65	1.00	–	26	39
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	9.00 BSC			354 BSC		
D1	8.75 BSC			344 BSC		
D2	6.0	6.15	6.25	236	242	246
E	9.00 BSC			354 BSC		
E1	8.75 BSC			344 BSC		
E2	6.0	6.15	6.25	236	242	246
e	0.50 BSC			20 BSC		
L	0.30	0.40	0.50	12	16	20
θ	0°	–	14°	0°	–	14°

## NOTE :

1. REFER TO JEDEC STD: MO-220.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

## Ordering Information

Part/Order Number	Shipping Packaging	Package	Temperature
9LRS3165BKLF	Trays	64-pin MLF	0 to +70° C
9LRS3165BKLF	Tape and Reel	64-pin MLF	0 to +70° C
9LRS3165BGLF	Tubes	64-pin TSSOP	0 to +70° C
9LRS3165BGLFT	Tape and Reel	64-pin TSSOP	0 to +70° C

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“B” is the device revision designator (will not correlate with the datasheet revision).

Due to package size constraints, actual top-side marking may differ from the full orderable part number.

**Revision History**

<b>Rev.</b>	<b>Issue Date</b>	<b>Issuer</b>	<b>Description</b>	<b>Page #</b>
A	08/21/12	D. Chan	Move to final.	
B	01/06/15	D. Chan	Changed package drawing from PUNCH to SAWN version	25, 26, 27

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
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