ISL8488E, ISL8489E, ISL8490E, ISL8491E

±15kV ESD Protected, 5V, Low Power, High Speed and Slew Rate Limited, Full Duplex, RS-485/RS-422 Transceivers

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The ISL8488E, ISL8489E, ISL8490E, ISL8491E devices are ESD protected, BiCMOS, 5V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. Each driver output and receiver input is protected against ±15kV ESD strikes, without latch-up. Unlike competitive versions, these devices are specified for 10% tolerance supplies (4.5V to 5.5V).

These devices are configured for full duplex (separate Rx input and Tx output pins) applications, so they are ideal for RS-422 networks requiring high ESD tolerance on the bus pins. The ISL8488E, ISL8490E are 8 Ld versions without Rx and Tx output enables. The other two versions include Rx and Tx output enable pins in a standard 14 Ld pinout.

The ISL8488E, ISL8489E utilize slew rate limited drivers which reduce EMI, and minimize reflections from improperly terminated transmission lines, or unterminated stubs in multidrop and multipoint applications.

Data rates up to 10Mbps are achievable by using the ISL8490E, ISL8491E, which feature higher slew rates.

The devices present a “single unit load” to the RS-485 bus, which allows a total of 32 transmitters and receivers on the network. For “1/8 unit load” versions (256 devices on the bus), please refer to the ISL4489E, ISL4491E data sheet.

Receiver (Rx) inputs feature a “fail-safe if open” design, which ensures a logic high Rx output if Rx inputs are floating.

Driver (Tx) outputs are short circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

Features

- RS-485 I/O Pin ESD Protection . . . . . ±15kV HBM
  - Class 3 ESD Level on all Other Pins . . . . . >7kV HBM
- High Data Rates (ISL8490E, ISL8491E) . . up to 10Mbps
- Slew Rate Limited for Error Free Data Transmission (ISL8488E, ISL8489E)
- Single Unit Load Allows up to 32 Devices on the Bus (See ISL4489E, ISL4491E for 256 Devices on Bus)
- Low Quiescent Current:
  - 120µA (ISL8488E)
  - 140µA (ISL8489E)
  - 370µA (ISL8490E, ISL8491E)
- -7V to +12V Common Mode Input Voltage Range
- Three-State Rx and Tx Outputs (Except ISL8488E, ISL8490E)
- Full Duplex Pinout
- Operates from a Single +5V Supply (10% Tolerance)
- Current Limiting and Thermal Shutdown for Driver Overload Protection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Factory Automation
- Security Networks
- Building Environmental Control Systems
- Industrial/Process Control Networks
- Level Translators (e.g., RS-232 to RS-422)
- RS-232 “Extension Cords”

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	HIGH ESD?	NO. OF DEVICES ALLOWED ON BUS	DATA RATE (Mbps)	SLEW-RATE LIMITED?	RECEIVER/ DRIVER ENABLE?	QUIESCENT I_{CC} (µA)	PIN COUNT
ISL8488E	Full	Yes	32	0.25	Yes	No	120	8
ISL8489E	Full	Yes	32	0.25	Yes	Yes	140	14
ISL8490E	Full	Yes	32	10	No	No	370	8
ISL8491E	Full	Yes	32	10	No	Yes	370	14

Ordering Information

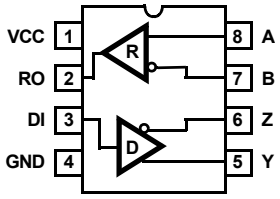
PART NUMBER (Notes 2)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE
ISL8488EIBZA	8488 EIBZ	8 Ld SOIC	M8.15	Tube	-40 to +85°C
ISL8488EIBZA-T				Reel, 2.5k	
ISL8489EIBZ	8489EIBZ	14 Ld SOIC	M14.15	Tube	
ISL8489EIBZ-T				Reel, 2.5k	
ISL8490EIBZ	8490E IBZ	8 Ld SOIC	M8.15	Tube	
ISL8490EIBZ-T				Reel, 2.5k	
ISL8491EIBZ	8491EIBZ	14 Ld SOIC	M14.15	Tube	
ISL8491EIBZ-T				Reel, 2.5k	

NOTES:

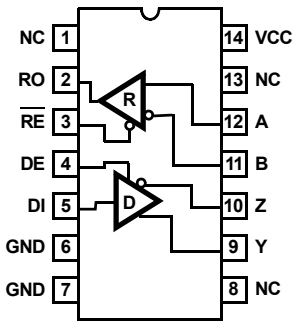
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL8488E, ISL8489E, ISL8490E, and ISL8491E device pages. For more information about MSL, see TB363.

Pinouts

ISL8488E, ISL8490E
(8 LD SOIC)
TOP VIEW



ISL8489E, ISL8491E
(14 LD SOIC)
TOP VIEW



Truth Tables (For ISL8488E, ISL8490E, only the DE = 1 and $\overline{RE}$ = 0 entries are valid)

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
X	0	X	High-Z	High-Z

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	X	≥ +0.2V	1
0	X	≤ -0.2V	0
0	X	Inputs Open	1
1	X	X	High-Z

Pin Descriptions

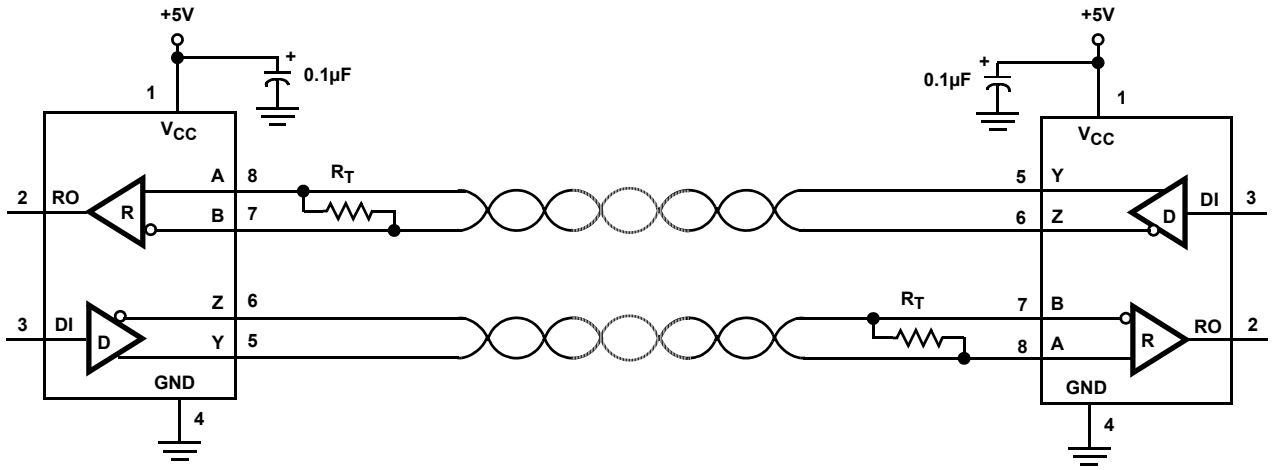
PIN	FUNCTION
RO	Receiver output: If A > B by at least 0.2V, RO is high; If A < B by 0.2V or more, RO is low; RO = High if A and B are unconnected (floating).
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low.

Pin Descriptions

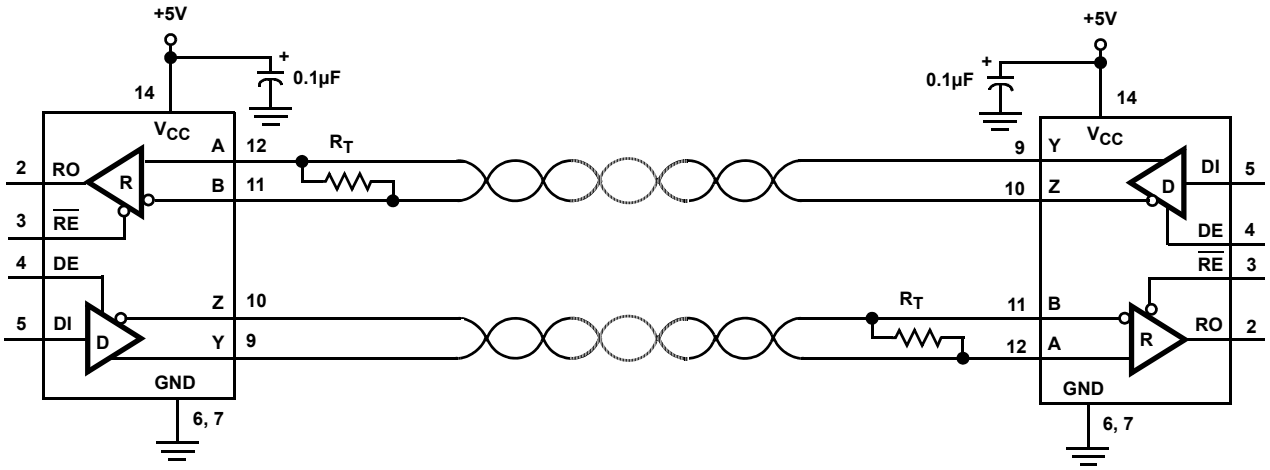
PIN	FUNCTION
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A	±15kV HBM ESD Protected, Non-inverting receiver input.
B	±15kV HBM ESD Protected, Inverting receiver input.
Y	±15kV HBM ESD Protected, Non-inverting driver output.
Z	±15kV HBM ESD Protected, Inverting driver output.
VCC	System power supply input (4.5V to 5.5V).
NC	No Connection.

Typical Operating Circuit

ISL8488E, ISL8490E



ISL8489E, ISL8491E



Absolute Maximum Ratings

V_{CC} to GND 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . . -0.5V to (V_{CC} + 0.5V)
Input/Output Voltages
A, B, Y, Z . . . . . -8V to + 12.5V
RO . . . . . -0.5V to (V_{CC} + 0.5V)
Short Circuit Duration
Y, Z . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
8 Ld SOIC Package (Note 4)	170
14 Ld SOIC Package (Note 4)	128

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C, (Note 5).

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 10)	TYP	MAX (NOTE 10)	UNITS
DC CHARACTERISTICS							
Driver Differential V_{OUT} (no load)	V_{OD1}		Full	-	-	V_{CC}	V
Driver Differential V_{OUT} (with load)	V_{OD2}	R = 50Ω (RS-422) (Figure 1)	Full	2	3	-	V
		R = 27Ω (RS-485) (Figure 1)	Full	1.5	2.3	5	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω (Figure 1)	Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R = 27Ω or 50Ω (Figure 1)	Full	-	-	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R = 27Ω or 50Ω (Figure 1)	Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$	Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$	Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DI	Full	-2	-	2	µA
		DE, $\overline{RE}$ (Note 9)	Full	-40	-	40	µA
Input Current (A, B) (Note 8)	I_{IN2}	DE = 0V, V_{CC} = 0V or 4.5V to 5.5V; V_{IN} = 12V	Full	-	-	1	mA
		DE = 0V, V_{CC} = 0V or 4.5V to 5.5V; V_{IN} = -7V	Full	-0.8	-	-	mA
Driver Three-State Output Current (Y, Z)	I_{OZD}	DE = 0V, -7V ≤ V_O ≤ 12V (Note 9)	Full	-100	-	100	µA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V	Full	-0.2	-	0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V	25	-	70	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV	Full	3.5	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = 200mV	Full	-	-	0.4	V
Receiver Three-State Output Current	I_{OZR}	$\overline{RE}$ = V_{CC}, 0.4V ≤ V_O ≤ 2.4V (Note 9)	Full	-	-	±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V	Full	12	-	-	kΩ
No-Load Supply Current (Note 6)	I_{CC}	ISL8488E, DI = 0V or V_{CC}	Full	-	120	140	µA
		ISL8489E, DE, DI, $\overline{RE}$ = 0V or V_{CC}	Full	-	140	190	µA
		ISL8490E/ISL8491E, DE, DI, $\overline{RE}$ = 0V or V_{CC}	Full	-	370	460	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (Note 7)	Full	35	-	250	mA

Electrical Specifications Test Conditions: V_{CC} = 4.5V to 5.5V; Unless Otherwise Specified. Typicals are at V_{CC} = 5V, T_A = +25°C, (Note 5). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 10)	TYP	MAX (NOTE 10)	UNITS
Receiver Short-Circuit Current	I_{OSR}	$0V \le V_O \le V_{CC}$	Full	7	-	85	mA
SWITCHING CHARACTERISTICS (ISL8488E, ISL8489E)							
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	250	400	2000	ns
Driver Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	160	800	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	250	600	2000	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF, SW = GND (Figure 3, Note 9)	Full	250	1000	2000	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, SW = V_{CC} (Figure 3, Note 9)	Full	250	860	2000	ns
Driver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND (Figure 3, Note 9)	Full	300	660	3000	ns
Driver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC} (Figure 3, Note 9)	Full	300	640	3000	ns
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 4)	Full	250	500	2000	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 4)	25	-	60	-	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND (Figure 5, Note 9)	Full	-	10	50	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC} (Figure 5, Note 9)	Full	-	10	50	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND (Figure 5, Note 9)	Full	-	10	50	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC} (Figure 5, Note 9)	Full	-	10	50	ns
Maximum Data Rate	f_{MAX}		Full	250	-	-	kbps
SWITCHING CHARACTERISTICS (ISL8490E, ISL8491E)							
Driver Input to Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	13	24	50	ns
Driver Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	-	3	10	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_L = 100pF (Figure 2)	Full	5	12	25	ns
Driver Enable to Output High	t_{ZH}	C_L = 100pF, SW = GND (Figure 3, Note 9)	Full	-	14	70	ns
Driver Enable to Output Low	t_{ZL}	C_L = 100pF, SW = V_{CC} (Figure 3, Note 9)	Full	-	14	70	ns
Driver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND (Figure 3, Note 9)	Full	-	44	70	ns
Driver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC} (Figure 3, Note 9)	Full	-	21	70	ns
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 4)	Full	30	90	150	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 4)	25	-	5	-	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND (Figure 5, Note 9)	Full	-	9	50	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC} (Figure 5, Note 9)	Full	-	9	50	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND (Figure 5, Note 9)	Full	-	9	50	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC} (Figure 5, Note 9)	Full	-	9	50	ns
Maximum Data Rate	f_{MAX}		Full	10	-	-	Mbps
ESD PERFORMANCE							
RS-485 Pins (A, B, Y, Z)		Human Body Model	25	-	±15	-	kV
All Other Pins			25	-	>±7	-	kV

NOTES:

5. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
6. Supply current specification is valid for loaded drivers when DE = 0V.
7. Applies to peak current. See “Typical Performance Curves” on page 9 for more information.
8. Devices meeting these limits are denoted as “single unit load (1 UL)” transceivers. The RS-485 standard allows up to 32 Unit Loads on the bus.
9. Not applicable to the ISL8488E, ISL8490E.
10. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms

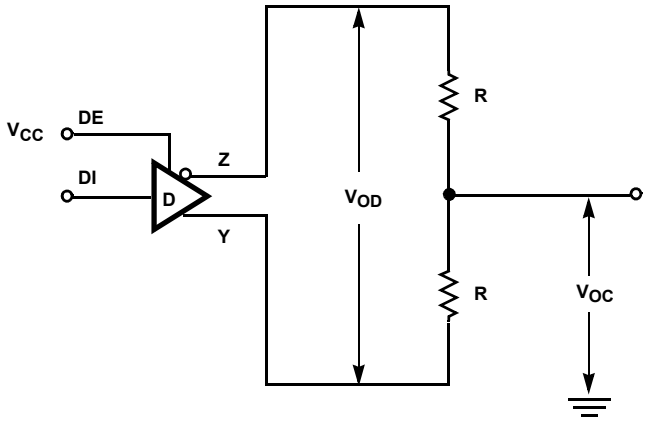


FIGURE 1. DRIVER V_{OD} AND V_{OC}

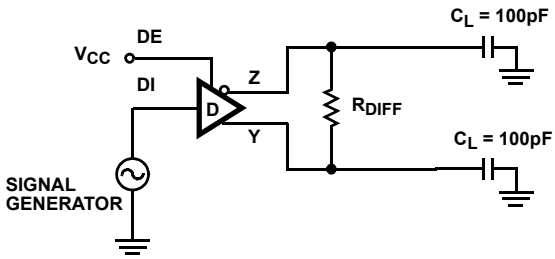
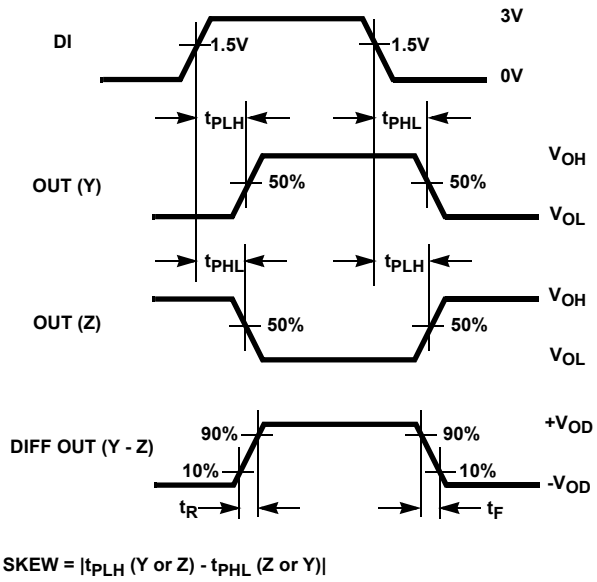


FIGURE 2A. TEST CIRCUIT

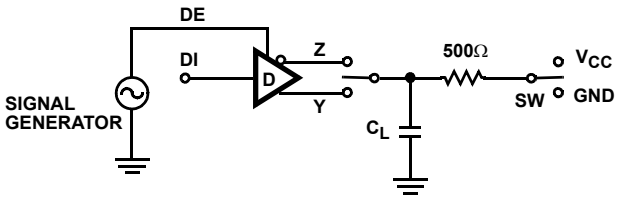


SKEW = $|t_{PLH}$ (Y or Z) - t_{PHL} (Z or Y)$|$

FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES

Test Circuits and Waveforms (Continued)



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	C_L (pF)
t_{HZ}	Y/Z	X	1/0	GND	15
t_{LZ}	Y/Z	X	0/1	V_{CC}	15
t_{ZH}	Y/Z	X	1/0	GND	100
t_{ZL}	Y/Z	X	0/1	V_{CC}	100

FIGURE 3A. TEST CIRCUIT

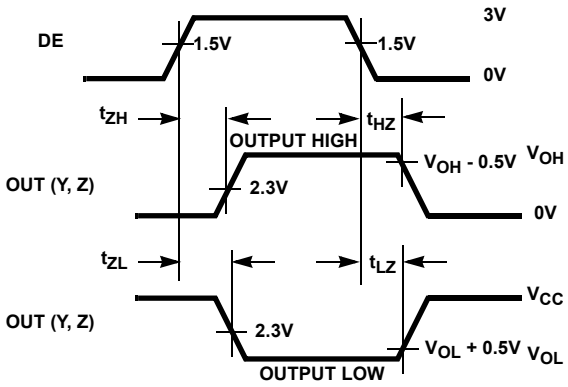


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES (EXCLUDING ISL8488E, ISL8490E)

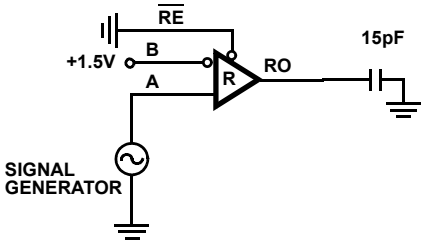


FIGURE 4A. TEST CIRCUIT

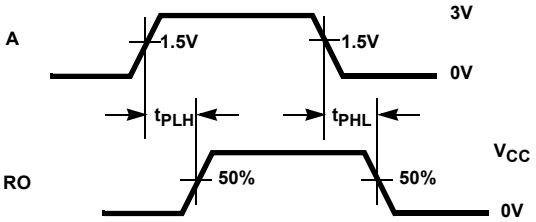
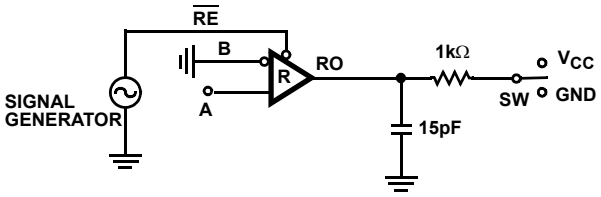


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. RECEIVER PROPAGATION DELAY



PARAMETER	DE	A	SW
t_{HZ}	X	+1.5V	GND
t_{LZ}	X	-1.5V	V_{CC}
t_{ZH}	X	+1.5V	GND
t_{ZL}	X	-1.5V	V_{CC}

FIGURE 5A. TEST CIRCUIT

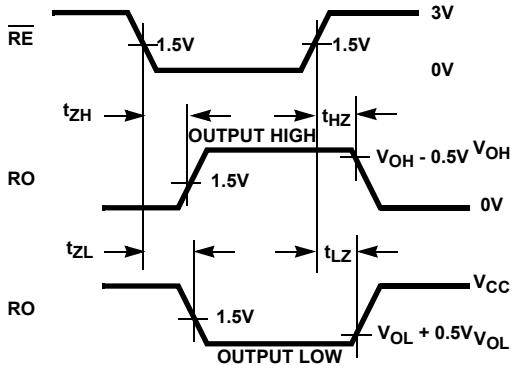


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER ENABLE AND DISABLE TIMES (EXCLUDING ISL8488E, ISL8490E)

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input resistance surpasses the RS-422 specification of 4kΩ, and meets the RS-485 "Unit Load" requirement of 12kΩ minimum.

Receiver inputs function with common mode voltages as great as ±7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages are a realistic concern.

All the receivers include a "fail-safe if open" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating).

Receivers easily meet the data rate supported by the corresponding driver. ISL8489E/ISL8491E receiver outputs are three-statable via the active low $\overline{RE}$ input.

Driver Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485), and at least 2V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI. ISL8489E/ISL8491E driver outputs are three-statable via the active high DE input.

The ISL8488E/ISL8489E driver outputs are slew rate limited to further reduce EMI, and to minimize reflections in unterminated or improperly terminated networks. Data rates on these slew rate limited versions are a maximum of 250kbps. Outputs of ISL8490E/ISL8491E drivers are not limited, so faster output transition times allow data rates of at least 10Mbps.

Data Rate, Cables, and Terminations

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

RS-485/RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 10Mbps are limited to lengths of a few hundred feet, while the 250kbps versions can operate at full data rates with lengths in excess of 1000'.

Proper termination is imperative, when using the 10Mbps devices, to minimize reflections. Short networks using the 250kbps versions need not be terminated, but, terminations are recommended unless power dissipation is an overriding concern. In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. The ISL84xxE devices meet this requirement via driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 specification, even at the common mode voltage range extremes. Additionally, these devices utilize a foldback circuit which reduces the short circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short circuit condition, ISL84xxE devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically reenable after the die temperature drops about 15°. If the contention persists, the thermal shutdown/reenable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

ESD Protection

All pins on these devices include class 3 Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of

±15kV HBM. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latch-up mechanism to activate, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified.

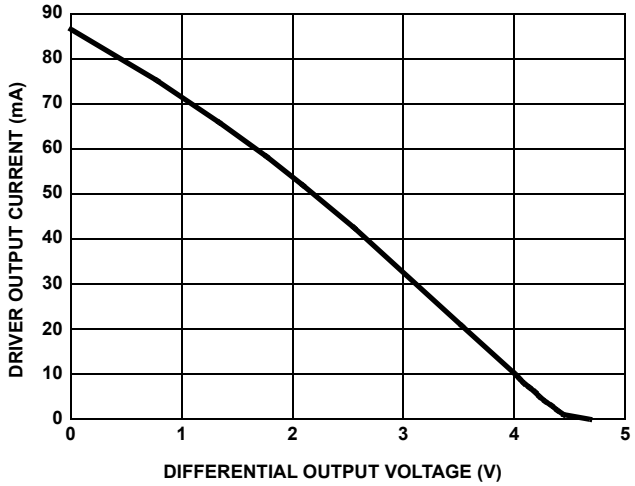


FIGURE 6. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

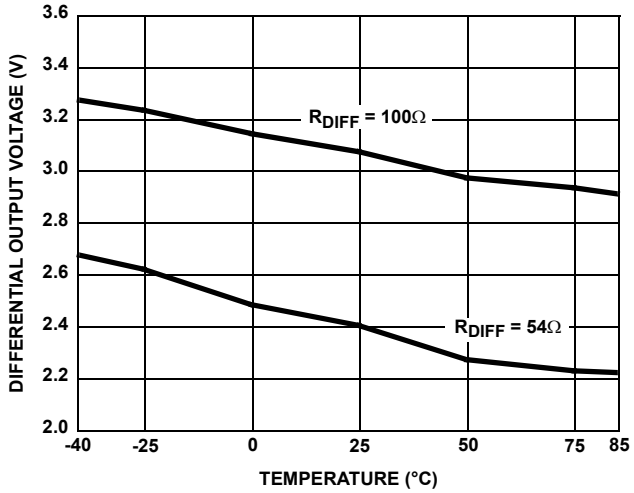


FIGURE 7. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

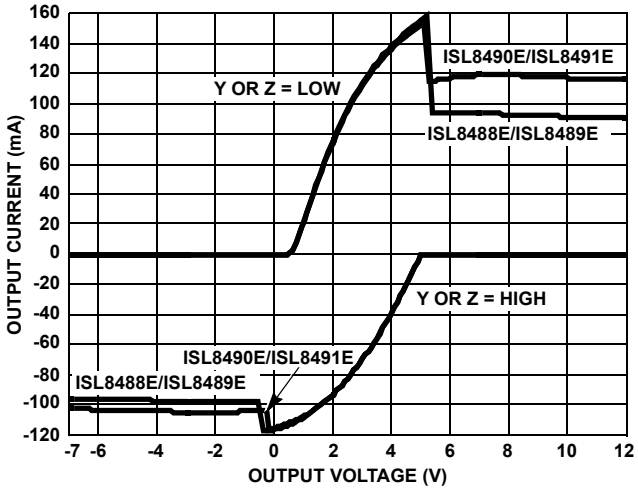


FIGURE 8. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

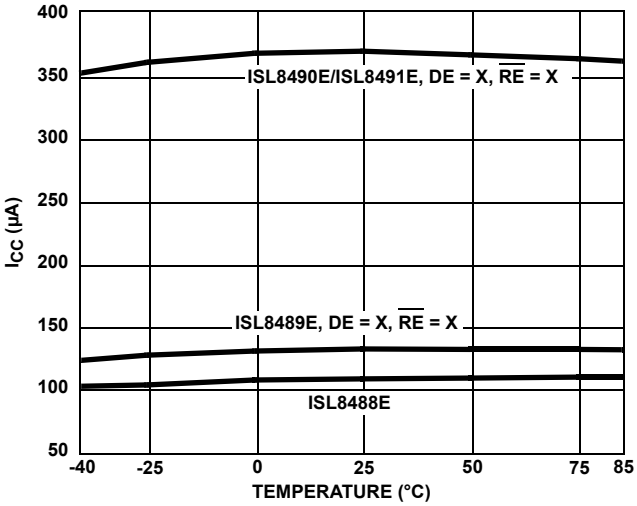


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified.

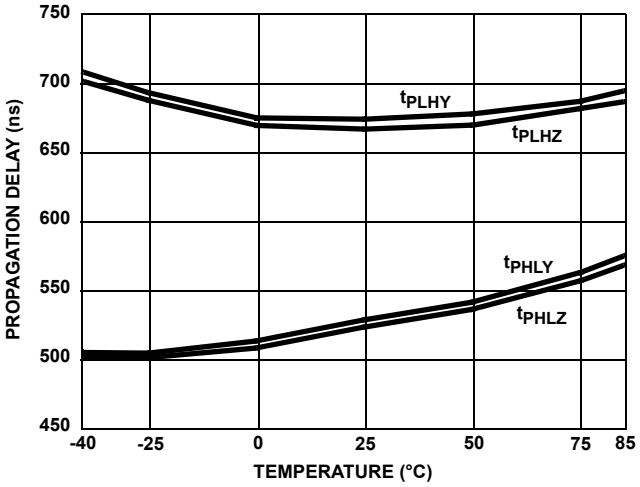


FIGURE 10. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL8488E/ISL8489E)

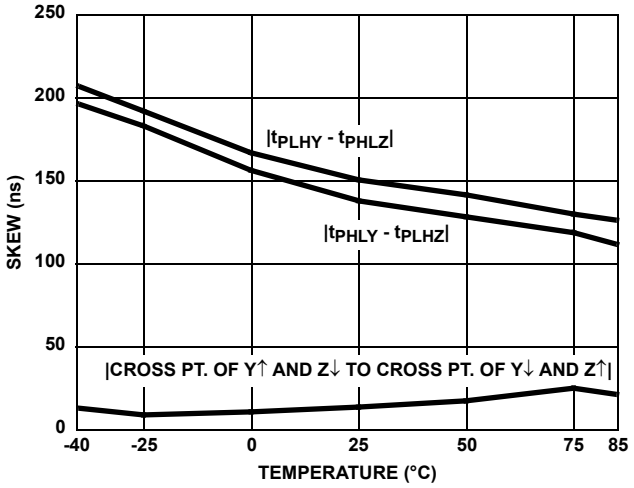


FIGURE 11. DRIVER SKEW vs TEMPERATURE (ISL8488E/ISL8489E)

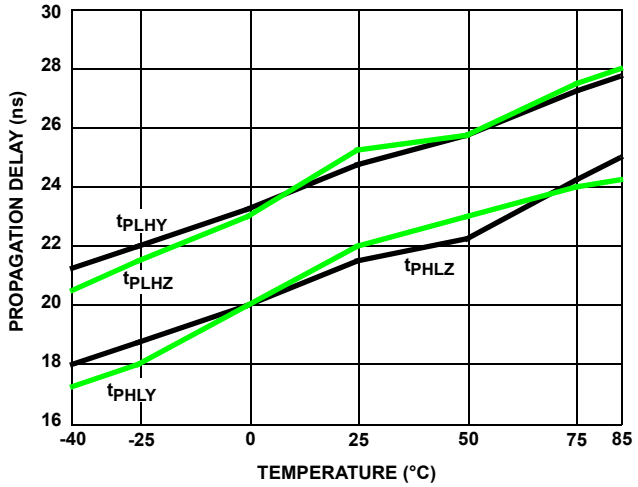


FIGURE 12. DRIVER PROPAGATION DELAY vs TEMPERATURE (ISL8490E/ISL8491E)

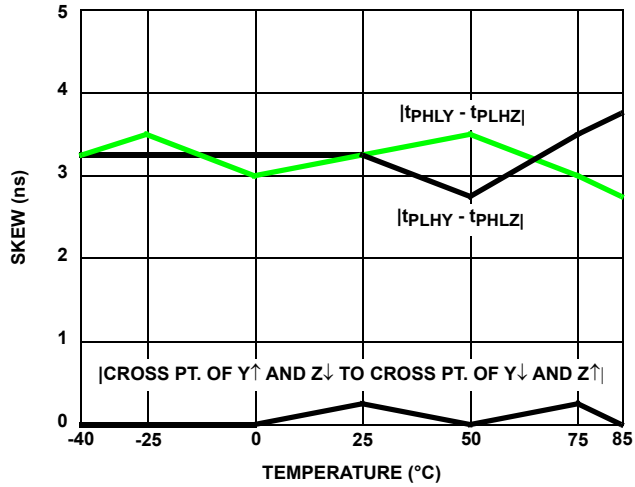


FIGURE 13. DRIVER SKEW vs TEMPERATURE (ISL8490E/ISL8491E)

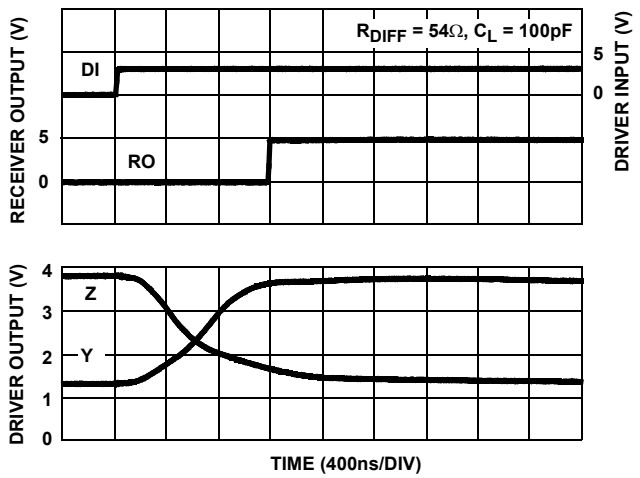


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL8488E/ISL8489E)

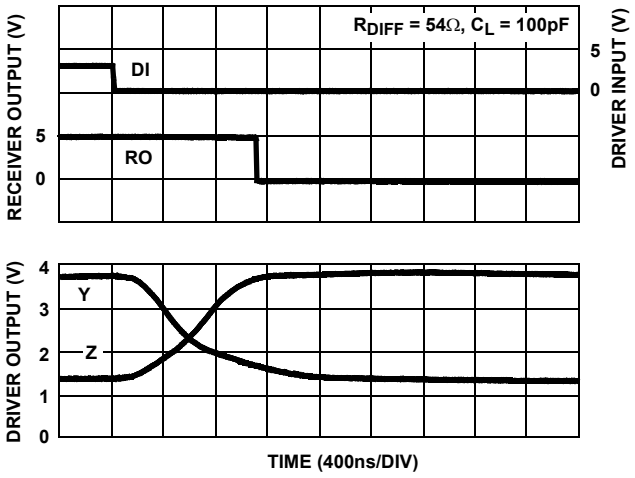


FIGURE 15. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL8488E/ISL8489E)

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified.

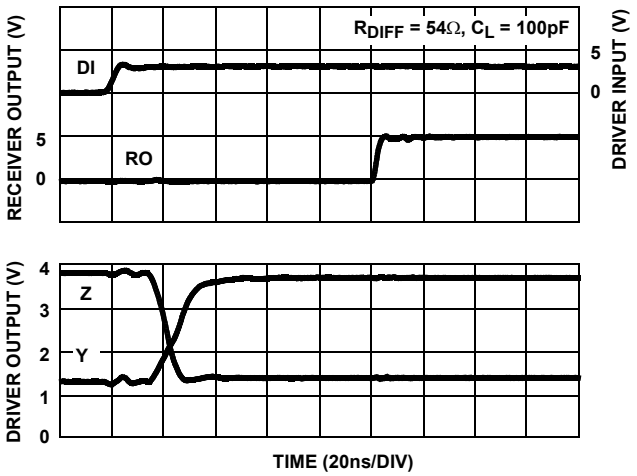


FIGURE 16. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL8490E/ISL8491E)

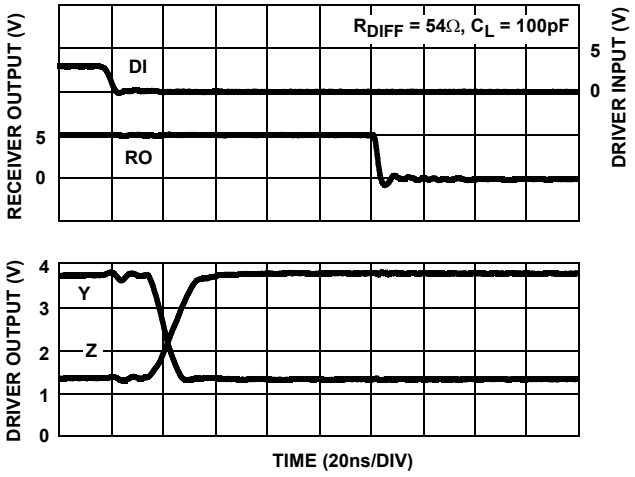


FIGURE 17. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL8490E/ISL8491E)

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

518

PROCESS:

Si Gate BiCMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

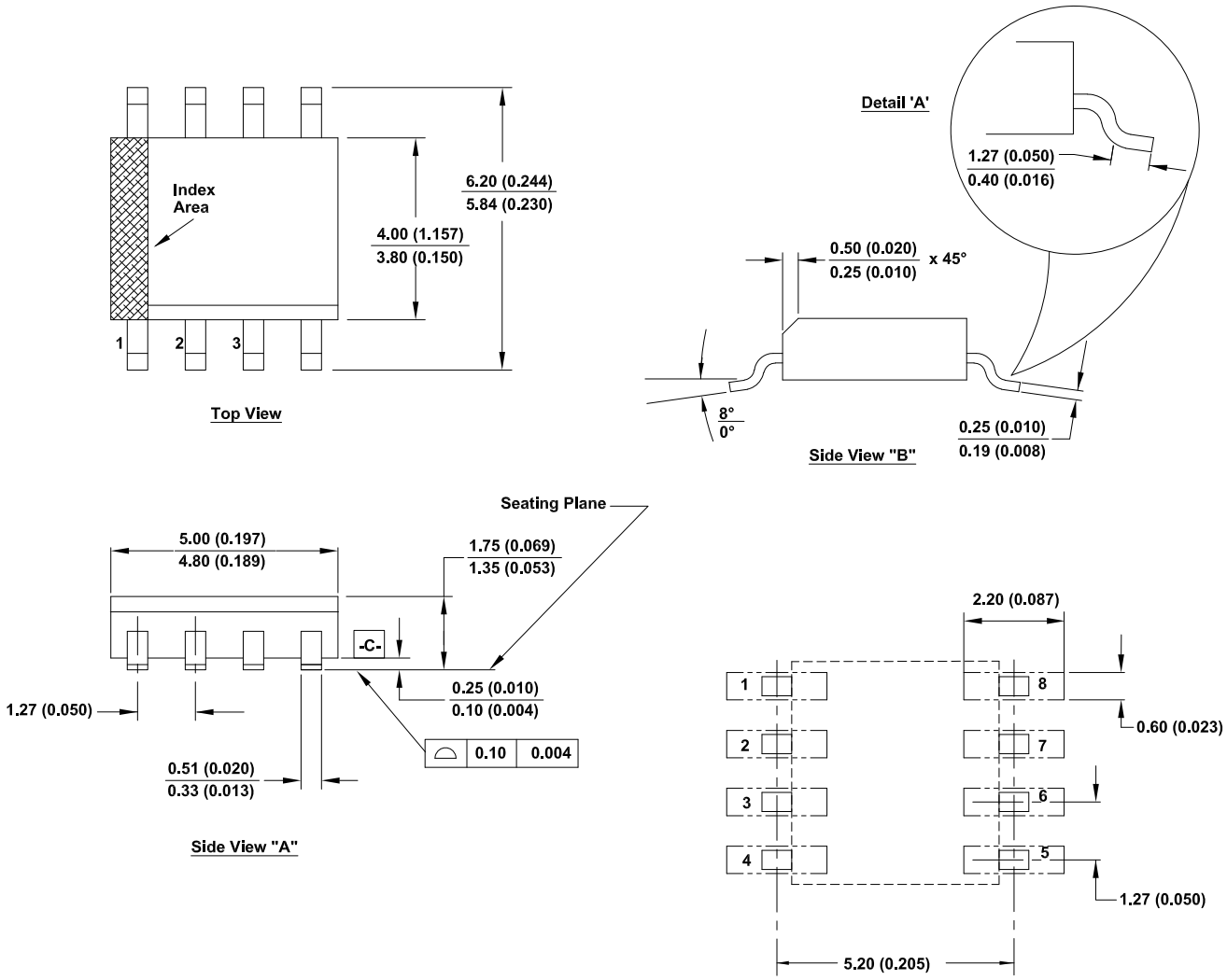
DATE	REVISION	CHANGE
Feb 3, 2022	4.01	Added links on page 1. Updated ordering information table formatting. Corrected typo for Logic Input Low Voltage spec by moving 0.8 value from minimum to maximum column. Added revision history section. Updated POD M8.15 to the latest revision, changes are as follows: - Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. - Changed 1982 to 1994 in Note 1. - Added the coplanarity spec into the drawing. Updated POD M14.15 to the latest revision, changes are as follows: - Add land pattern and moved dimensions from table onto drawing. - In Side View B and Detail A: Added lead length dimension (1.27 – 0.40) and Changed angle of the lead to 0-8 degrees.

Package Outline Drawings

For the most recent package outline drawing, see M8.15.

M8.15

8 Lead Narrow Body Small Outline Plastic Package
Rev 5, 4/2021

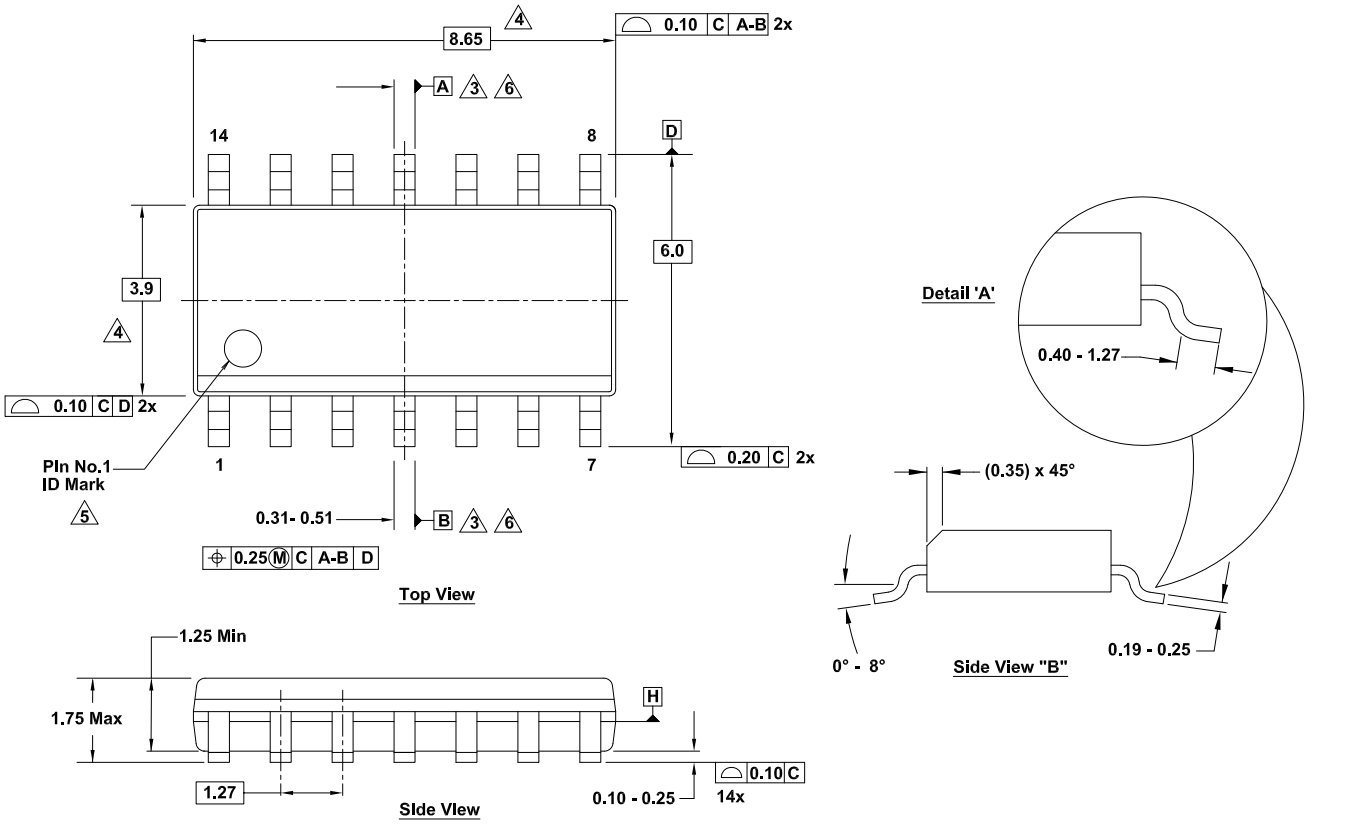


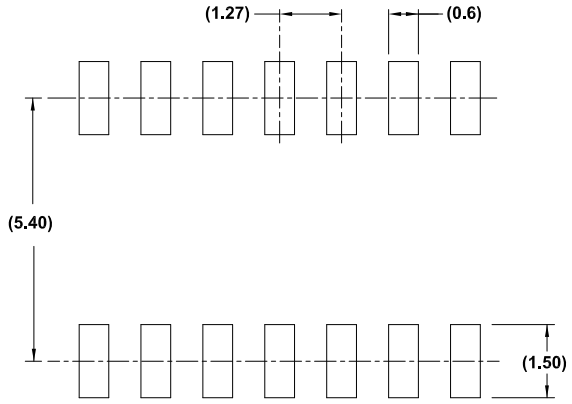
NOTES:

1. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
2. Package length does not Include mold flash, protrustion or gate burrs. Mold flash, protrustion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrustions. Interlead flash and protrustions shallnot exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. if it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 Inch).
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

For the most recent package outline drawing, see M14.15.

M14.15
14 Lead Narrow Body Small Outline Plastic Package
Rev 2, 6/20





Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Datums A and B are determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier can be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

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(Rev.1.0 Mar 2020)

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