

# IRF3808PbF

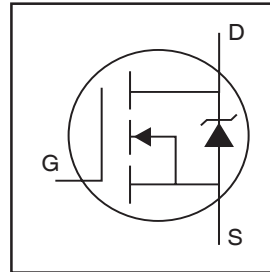
HEXFET® Power MOSFET

## Typical Applications

- Industrial Motor Drive

## Benefits

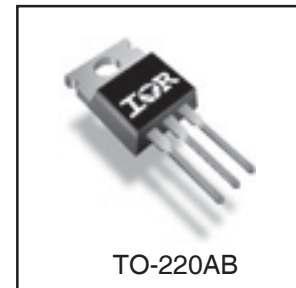
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free



$V_{DSS} = 75V$
$R_{DS(on)} = 0.007\Omega$
$I_D = 140A\text{⑥}$

## Description

This Advanced Planar Stripe HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, low  $R\theta JC$ , fast switching speed and improved repetitive avalanche rating. This combination makes the design an extremely efficient and reliable choice for use in a wide variety of applications.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	140⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	97⑥	
$I_{DM}$	Pulsed Drain Current ①	550	
$P_D @ T_C = 25^\circ C$	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②	430	mJ
$I_{AR}$	Avalanche Current①	82	A
$E_{AR}$	Repetitive Avalanche Energy⑦	See Fig.12a, 12b, 15, 16	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

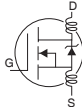
## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.086	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.9	7.0	$m\Omega$	$V_{GS} = 10V, I_D = 82A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	100	—	—	S	$V_{DS} = 25V, I_D = 82A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 75V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 60V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	150	220	nC	$I_D = 82A$
$Q_{gs}$	Gate-to-Source Charge	—	31	47		$V_{DS} = 60V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	50	76		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 38V$
$t_r$	Rise Time	—	140	—		$I_D = 82A$
$t_{d(off)}$	Turn-Off Delay Time	—	68	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	120	—		$V_{GS} = 10V$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	5310	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	890	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	130	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	6010	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	570	—		$V_{GS} = 0V, V_{DS} = 60V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	1140	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 60V$

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	140	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	550		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 82A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	93	140	ns	$T_J = 25^\circ\text{C}, I_F = 82A$
$Q_{rr}$	Reverse Recovery Charge	—	340	510	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.130\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 82A$ . (See Figure 12).
- ③  $I_{SD} \leq 82A$ ,  $di/dt \leq 310A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

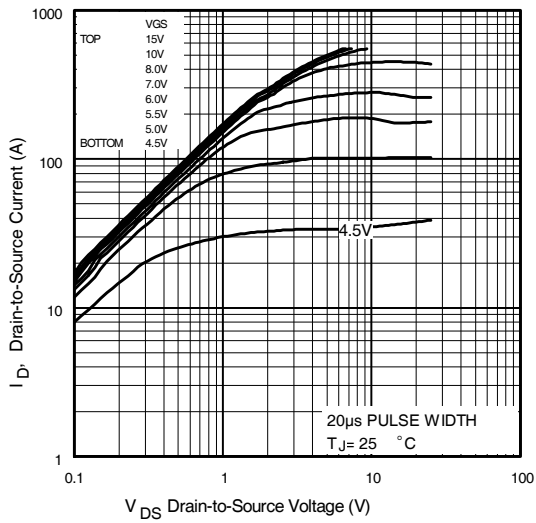


Fig 1. Typical Output Characteristics

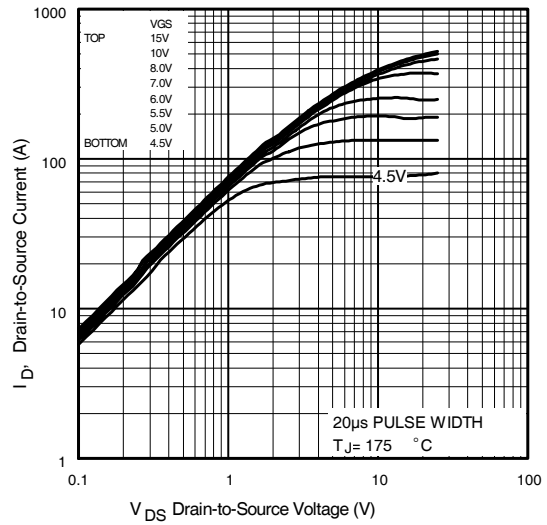


Fig 2. Typical Output Characteristics

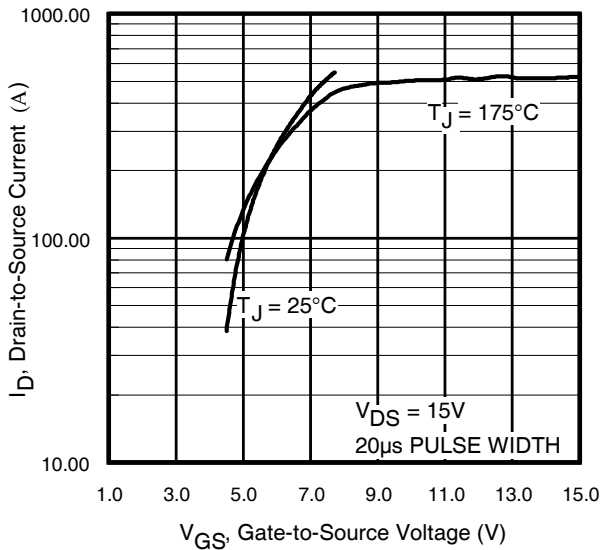


Fig 3. Typical Transfer Characteristics

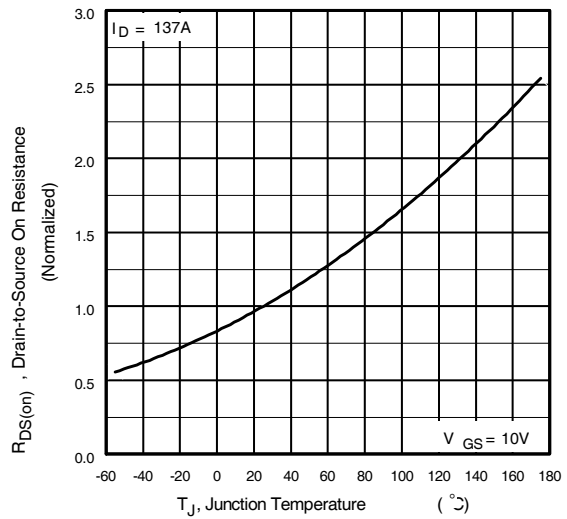
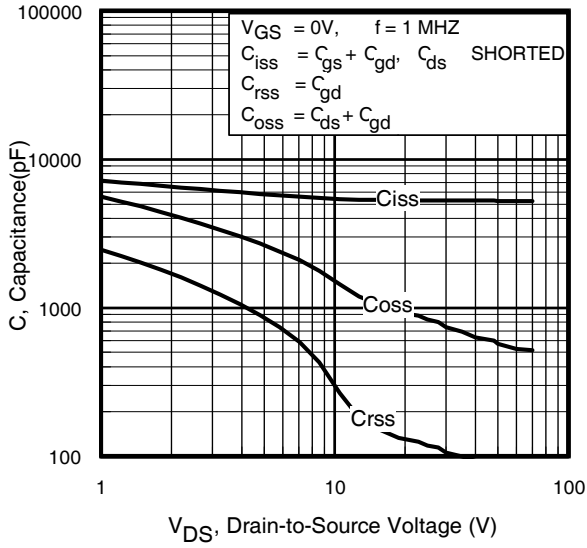
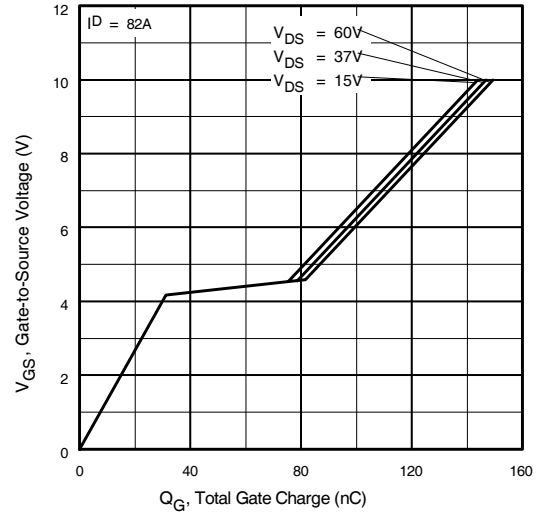


Fig 4. Normalized On-Resistance Vs. Temperature

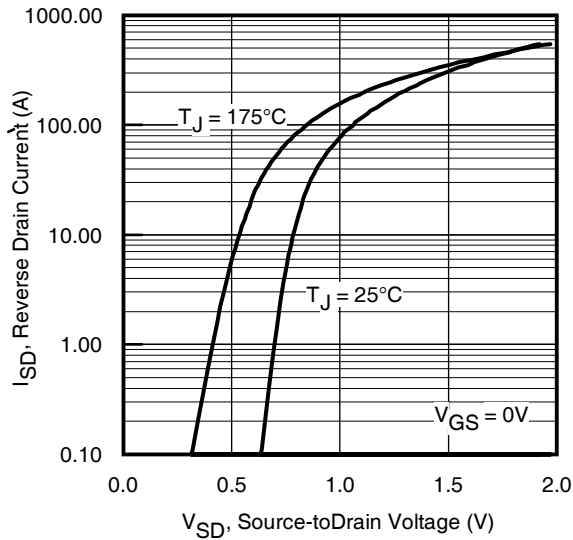
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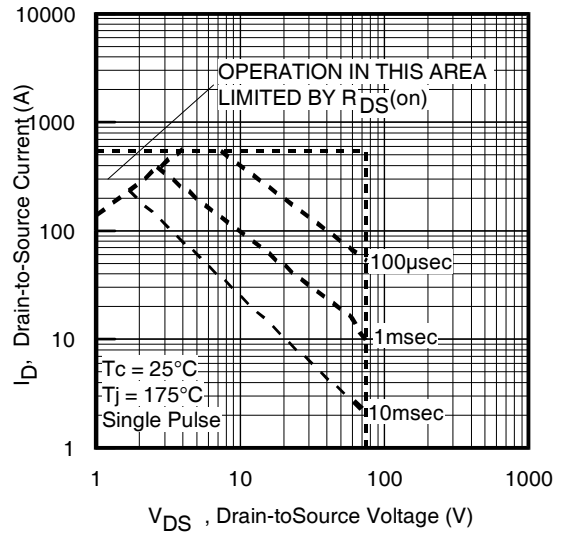
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



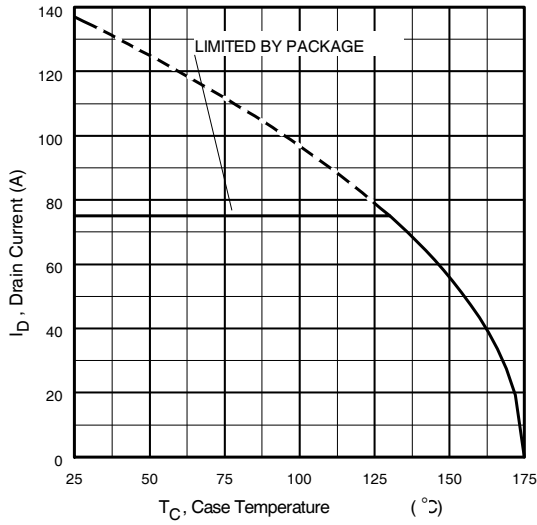
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



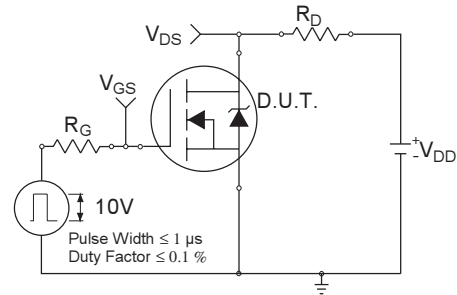
**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



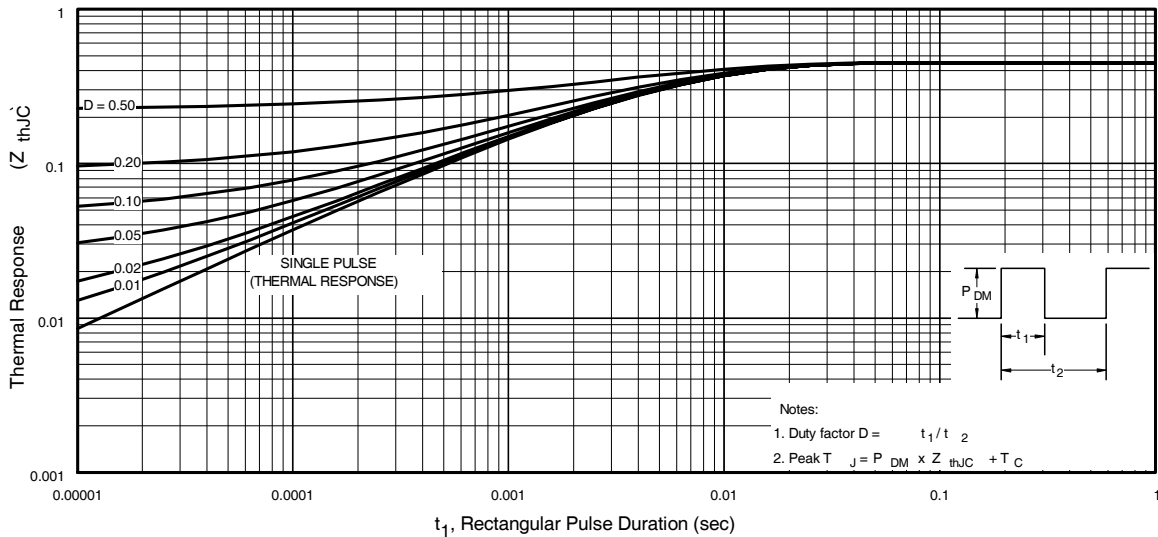
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

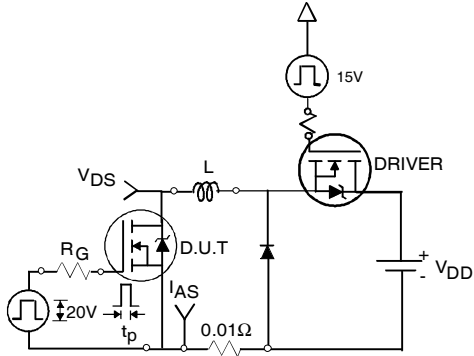


**Fig 10b.** Switching Time Waveforms

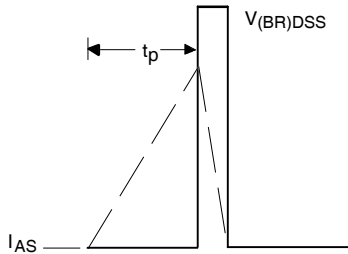


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

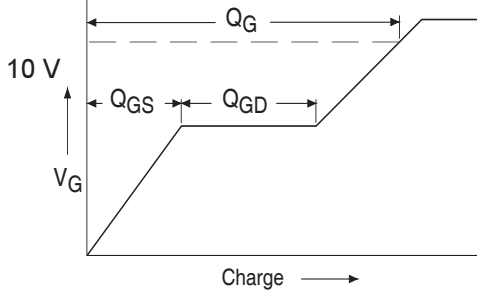
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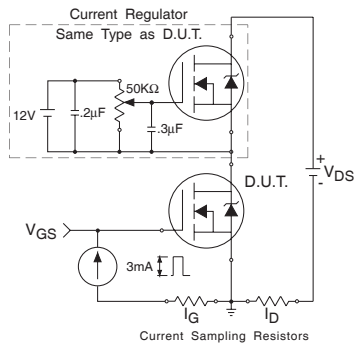
**Fig 12a.** Unclamped Inductive Test Circuit



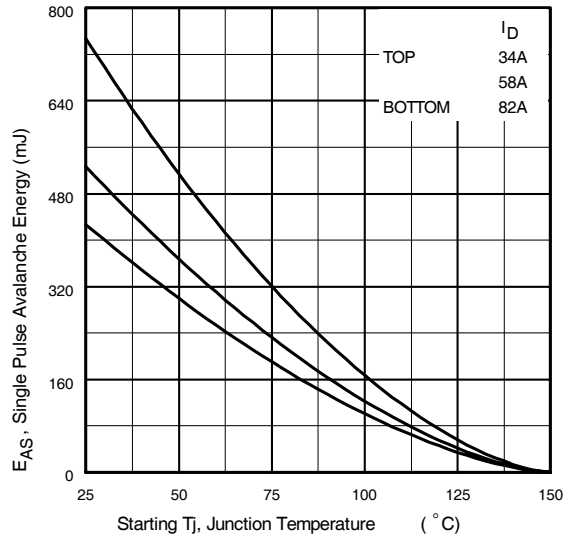
**Fig 12b.** Unclamped Inductive Waveforms



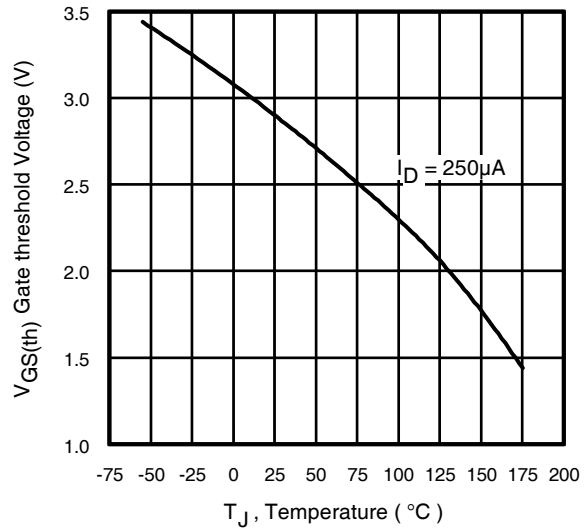
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Threshold Voltage Vs. Temperature

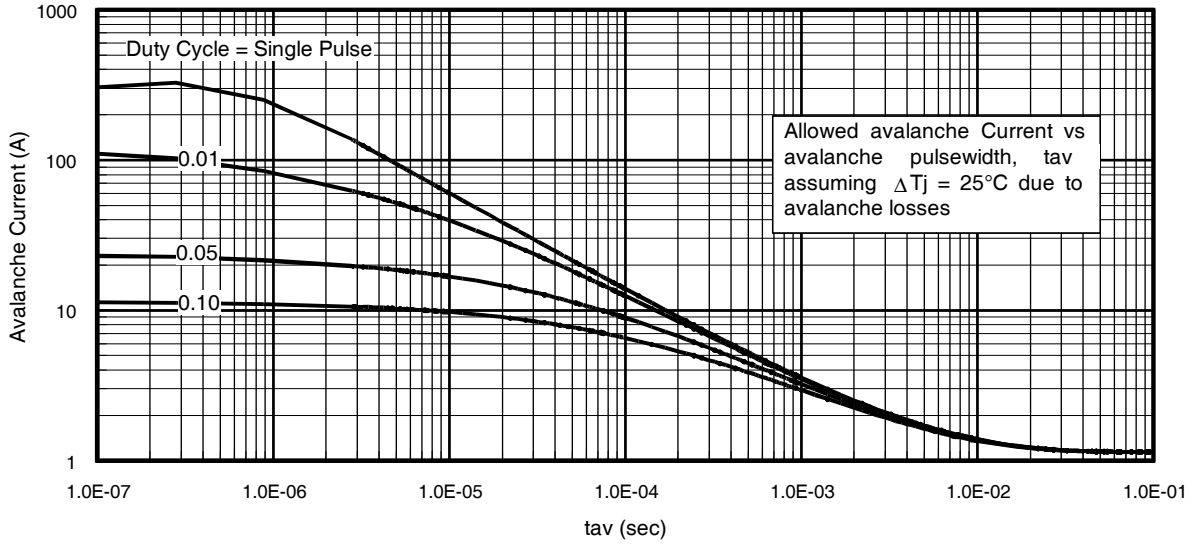


Fig 15. Typical Avalanche Current Vs.Pulsewidth

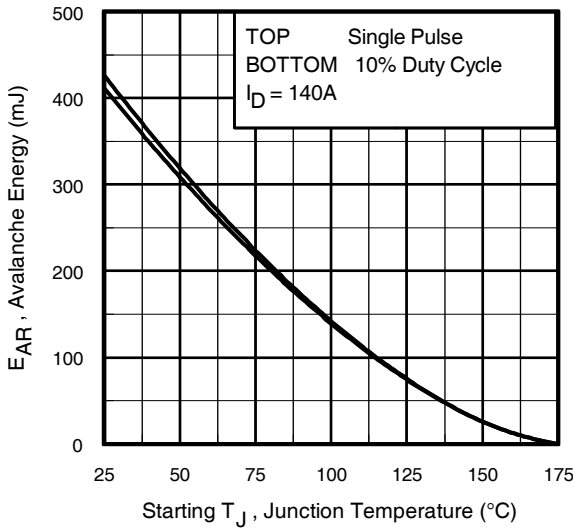


Fig 16. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

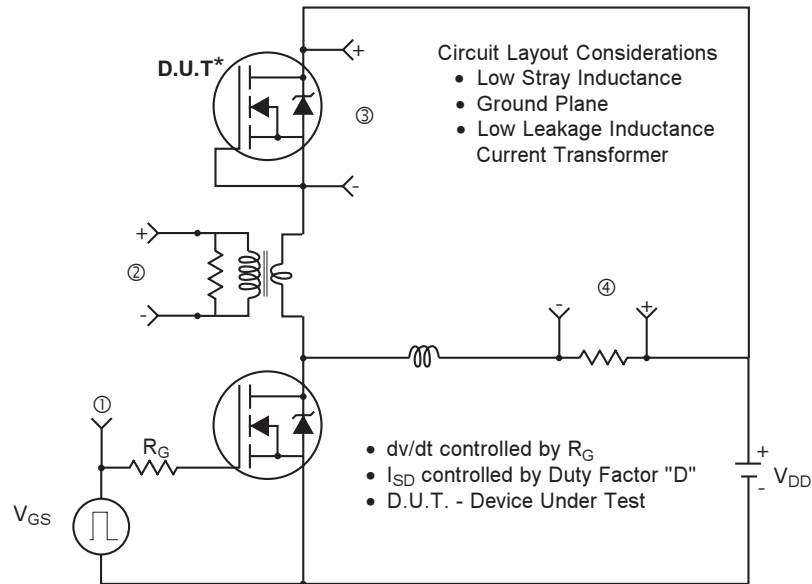
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

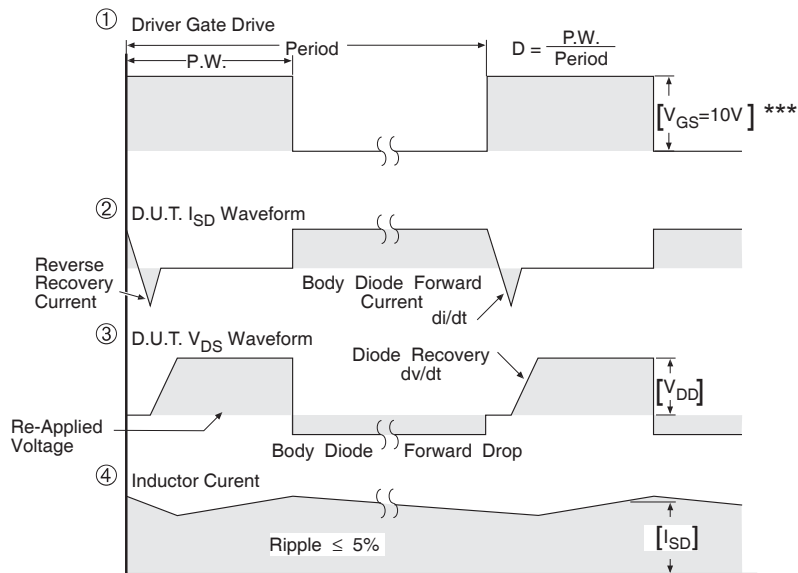
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



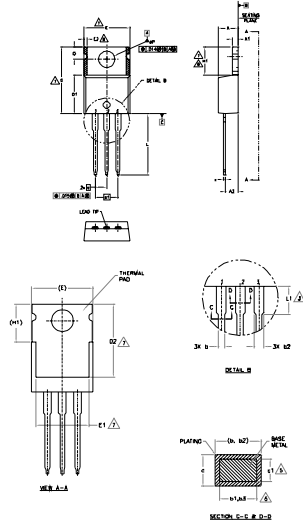
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 17.** For N-channel HEXFET® power MOSFETs



## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1- DIMENSIONS AND TOLERANCING AS PER ASME Y14.5 M-1994
  - 2- DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS)
  - 3- LEAD DIMENSIONS AND FINISH UNLESS OTHERWISE NOTED
  - 4- DIMENSIONS D, E, H & I DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .002" (0.051) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMITY OF THE PLASTIC BODY
  - 5- DIMENSIONS M, N & O APPLY TO BARE METAL ONLY
  - 6- CONTROLLING DIMENSION - INCHES
  - 7- THERMAL AND CONDUCTIVE COEFFICIENT DIMENSIONS (M102 & T1)
  - 8- DIMENSION T2 IS NOT DEFINED A 25MA. WHITE STAMPING AND SKEW/ROTATION INDICATORS ARE ALLOWED
  - 9 - OUTLINE DIMENSIONS TO ASSEMBLY TO 25% EXCEPT A2 (max) AND D2 (min). THESE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SHAPE	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
B	0.38	1.01	.015	.040	
B1	0.38	0.91	.015	.036	5
B2	1.14	1.78	.045	.070	
B3	1.14	1.71	.045	.068	5
C	0.36	0.41	.014	.016	
D1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.52	.330	.375	
D2	11.40	12.80	.450	.507	7
E	9.82	10.87	.390	.425	4,7
E1	8.86	8.89	.350	.350	7
E2	-	0.76	-	.030	8
F	2.54	2.54	.100	.100	
H1	0.84	6.86	.330	270	7,8
L	12.70	14.73	.500	.580	
L1	5.56	4.06	.140	.160	3
M	5.24	4.08	.138	.161	
Q	2.54	3.42	.100	.135	

USE DIMENSIONS

1- CASE

2- DIM.

3- DIM.

4- DIM.

5- DIM.

6- DIM.

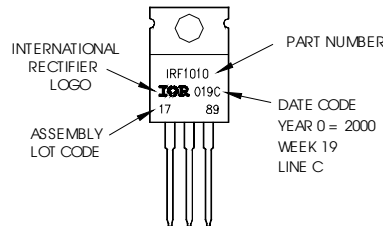
7- DIM.

8- DIM.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 2000  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-220AB package is not recommended for Surface Mount Application

### Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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