IR MOSFET-DirectFET™

IRF7749L1TRPbF

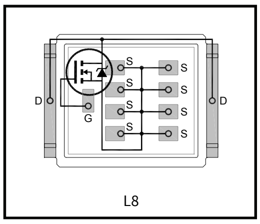
Quality Requirement Category: Industrial

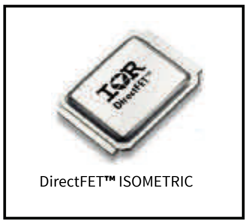
DirectFET™ N-Channel Power MOSFET

V_{DSS}	60V
$R_{DS(on)}$ typ. @ V_{GS} = 10V	1.1mΩ
$R_{DS(on)}$ max @ V_{GS} = 10V	1.5mΩ
I_D (Silicon Limited)	345A ⑦
I_D (Package Limited)	375A ①

Applications

- RoHS Compliant, Halogen Free
- Lead-Free (Qualified up to 260°C Reflow)
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible
- Compatible with existing Surface Mount Techniques





RoHS

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF7749L1TRPbF	DirectFET™ Large Can (LA)	Tape and Reel	4000	IRF7749L1TRPbF

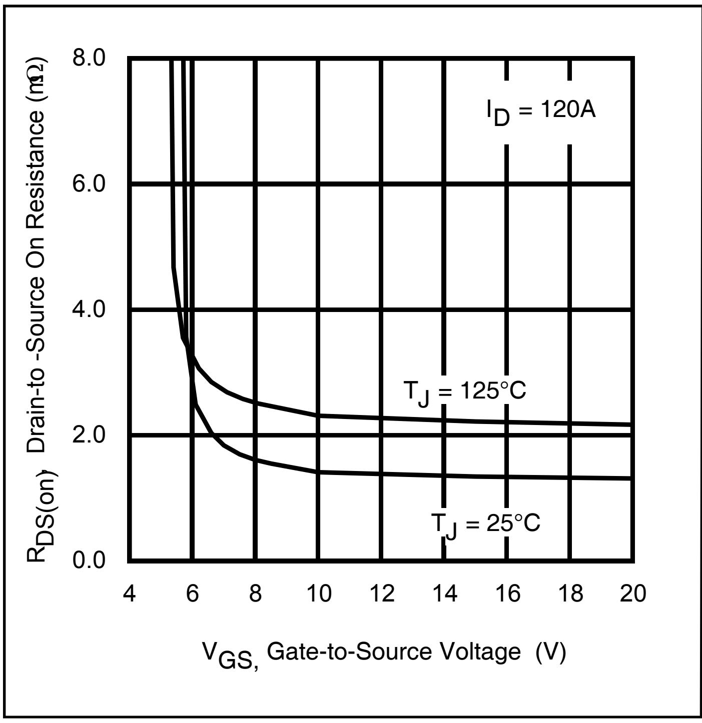


Figure 1 Typical On-Resistance vs. Gate Voltage

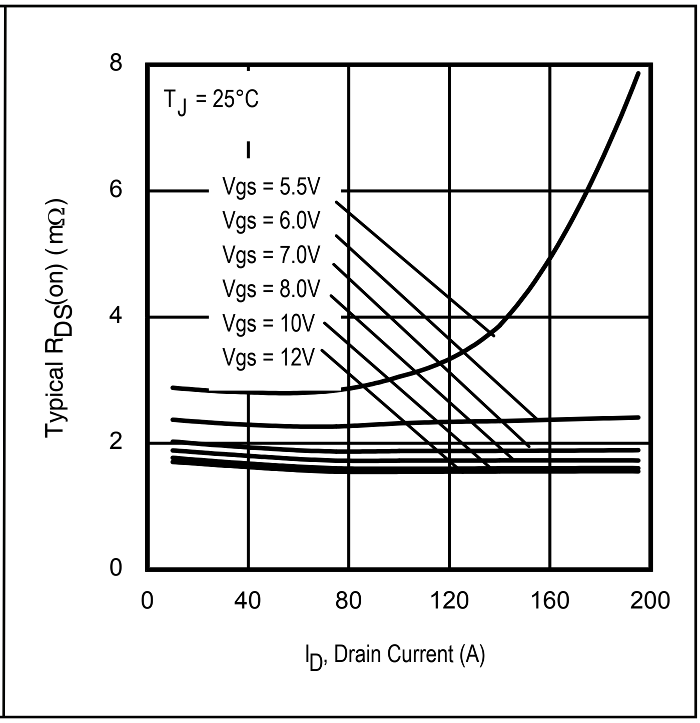


Figure 2 Typical On-Resistance vs. Drain Current

Table of Contents

1 Parameters

Table1 Key performance parameters

Parameter	Values	Units
V_{DS}	60	V
$R_{DS(on)\ max}$	1.5	mΩ
I_D @ T_C	345 ⑦	A
I_D @ T_A	36	A

2 Maximum ratings and thermal characteristics

Table 2 Maximum ratings (at T_J=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current (Silicon Limited) ❹	I_D	T_C = 25°C, V_{GS} @ 10V	345 ⑦	A
Continuous Drain Current (Silicon Limited) ❹	I_D	T_C = 100°C, V_{GS} @ 10V	243	
Continuous Drain Current (Silicon Limited) ❶	I_D	T_A= 25°C, V_{GS} @ 10V	36	
Continuous Drain Current (Package Limited) ❹	I_D	T_C = 25°C, V_{GS} @ 10V	375 ①	
Pulsed Drain Current ②	I_{DM}	T_C = 25°C	1380	
Maximum Power Dissipation	P_D	T_C = 25°C	341	W
Maximum Power Dissipation	P_D	T_A = 25°C	3.8	
Linear Derating Factor	-	-	0.025	W/°C
Gate-to-Source Voltage	V_{GS}	-	± 20	V
Operating Junction	T_J	-	-55 to + 175	°C
Storage Temperature Range	T_{STG}	-		

Table 3 Thermal characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Ambient ❶	$R_{\theta JA}$	-	-	-	40	°C/W
Junction-to-Ambient ❸	$R_{\theta JA}$	-	-	12.5	-	
Junction-to-Ambient ❷	$R_{\theta JA}$	-	-	20	-	
Junction-to-Case ❹ ⑥	$R_{\theta JC}$	-	-	-	0.44	
Junction-to-PCB Mounted	$R_{\theta JA\text{-}PCB}$	-	-	-	0.5	

Table 4 Avalanche characteristics

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy (Thermally Limited ③	E_{AS}	315	mJ
Single Pulse Avalanche Energy (Tested) ③	E_{AS}	714	
Avalanche Current ②	I_{AR}	See Fig.15,16, 19a, 19b	A
Repetitive Avalanche Energy ②	E_{AR}		mJ

Notes:

① *Package limit current based on source connection technology*
② *Repetitive rating; pulse width limited by max. junction temperature.*
③ *Limited by $T_J$max, starting T_J = 25°C, L = 0.044mH, R_G = 50Ω, I_{AS} = 120A, V_{GS} =10V.*
④ *Pulse width ≤ 400µs; duty cycle ≤ 2%.*
⑤ *C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
⑥ *R_θ is measured at T_J approximately 90°C.*
⑦ *Silicon limit current based on maximum allowable junction temperature $T_{Jmax.}$*

3 Electrical characteristics

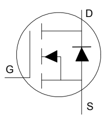
Table 5 Static characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, I_D = 3.0mA	-	56	-	mV/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 120A	-	1.1	1.5	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	-	4.0	V
Gate Threshold Voltage Coefficient	$\Delta V_{GS(th)}/\Delta T_J$		-	8.8	-	mV/°C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	-	-	20	μA
		V_{DS} = 60V, V_{GS} = 0V, T_J = 125°C	-	-	250	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 20V	-	-	100	nA
	I_{GSS}	V_{GS} = -20V	-	-	100	
Gate Resistance	R_G	-	-	1.5	-	Ω

Table 6 Dynamic characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Forward Trans conductance	gfs	V_{DS} = 10V, I_D = 120A	185	-	-	S
Total Gate Charge	Q_g	I_D = 120A V_{DS} = 30V V_{GS} = 10V ④	-	183	275	nC
Gate-to-Source Charge	Q_{gs1}		-	39	-	
Gate-to-Source Charge	Q_{gs2}			19		
Gate-to-Drain ("Miller) Charge	Q_{gd}		-	46	-	
Gate Charge Overdrive	Q_{godr}		-	79	-	
Switch Charge (Qgs2 + Qgd)	Q_{sw}		-	65	-	
Output Charge	Q_{oss}	V_{DS} = 48V, V_{GS} = 0V	-	119	-	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30V	-	29	-	ns
Rise Time	t_r	I_D = 120A	-	149	-	
Turn-Off Delay Time	$t_{d(off)}$	R_G = 1.8Ω	-	72	-	
Fall Time	t_f	V_{GS} = 10V ④	-	88	-	
Input Capacitance	C_{iss}	V_{GS} = 0V	-	10655	-	pF
Output Capacitance	C_{oss}	V_{DS} = 25V	-	1627	-	
Reverse Transfer Capacitance	C_{rss}	f = 1.0MHz	-	680	-	
Effective Output Capacitance	C_{oss} eff.	V_{GS} = 0V, V_{DS} = 0V to 48V ⑤	-	1959	-	

Table 7 Reverse Diode

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	345⑦	A
Pulsed Source Current (Body Diode) ②	I_{SM}		-	-	1380	
Diode Forward Voltage	V_{SD}	T_J = 25°C, I_S = 120A, V_{GS} = 0V ④	-	-	1.3	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = 120A,	-	42	-	ns
Reverse Recovery Charge	Q_{rr}	V_{DD} = 30V, di/dt = 100A/μs ④	-	54	-	nC

4 Electrical characteristic diagrams

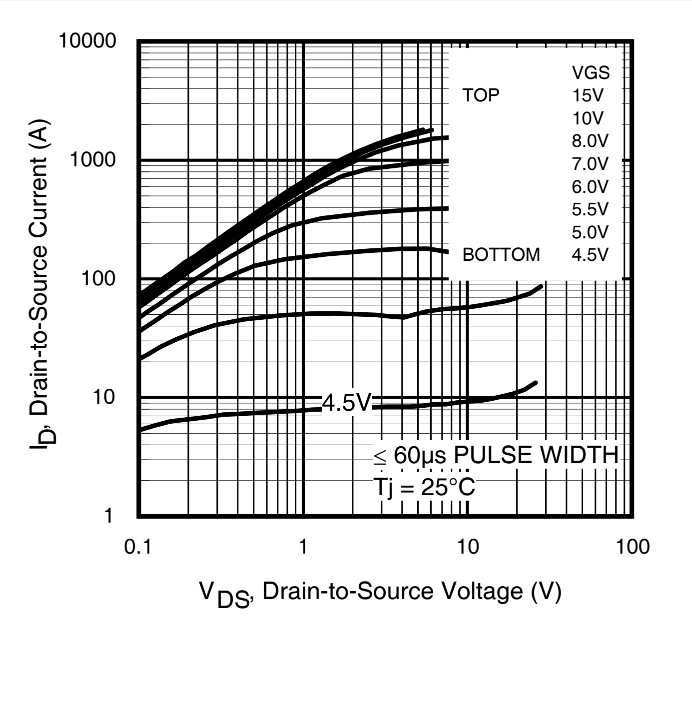


Figure 3 **Typical Output Characteristics**

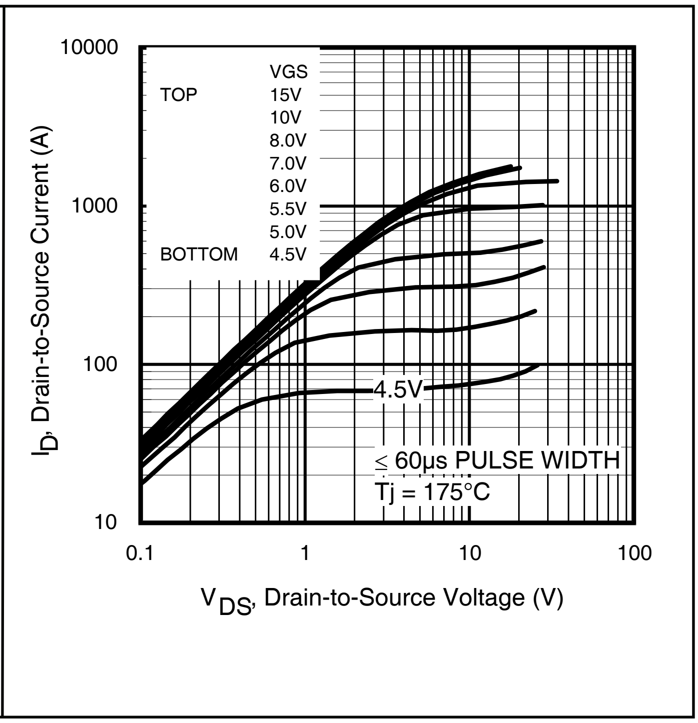


Figure 4 **Typical Output Characteristics**

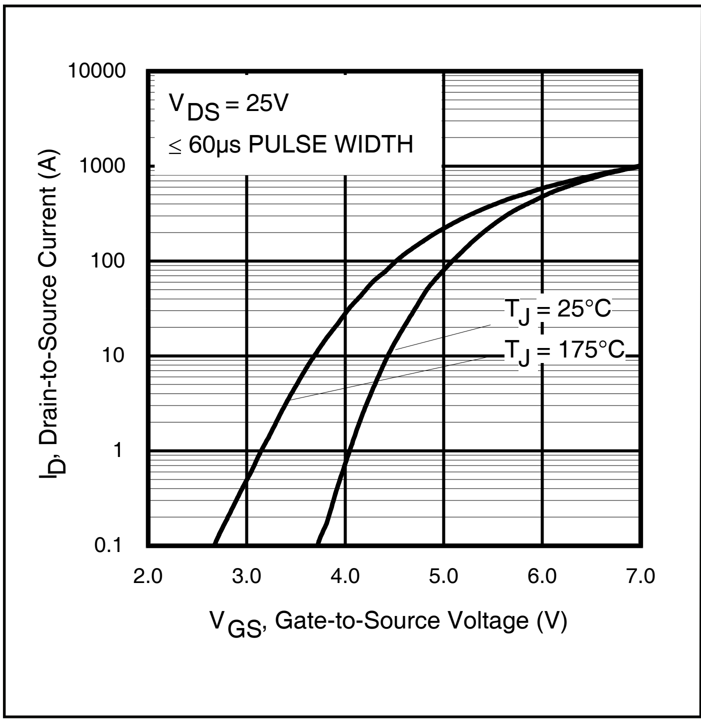


Figure 5 **Typical Transfer Characteristics**

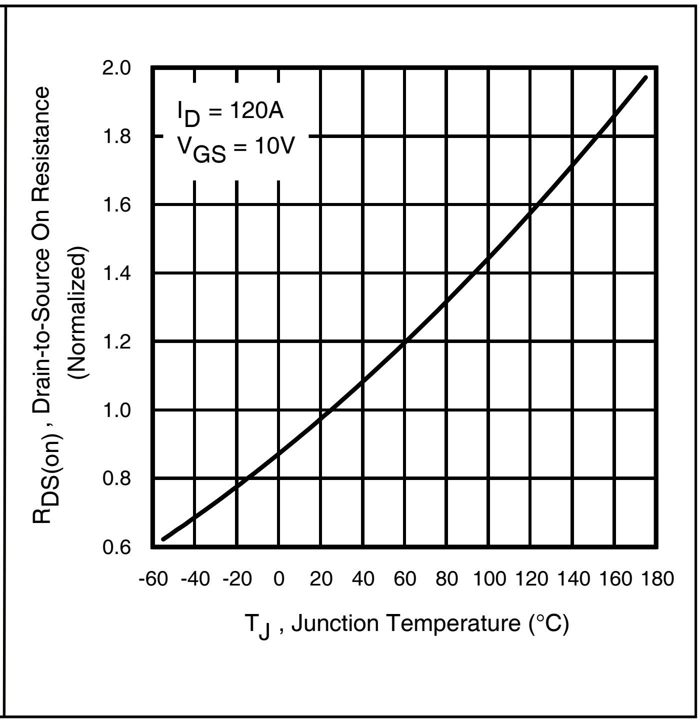
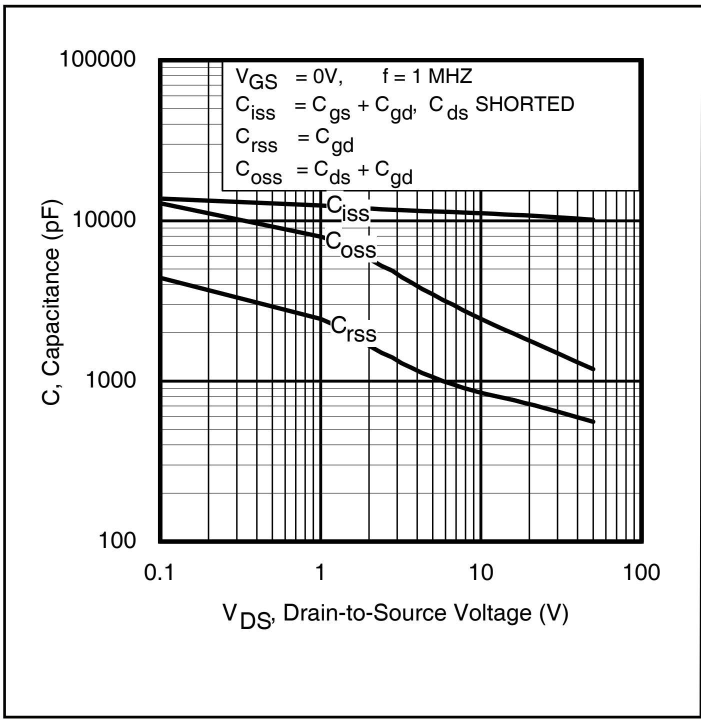


Figure 6 **Normalized On-Resistance vs. Temperature**



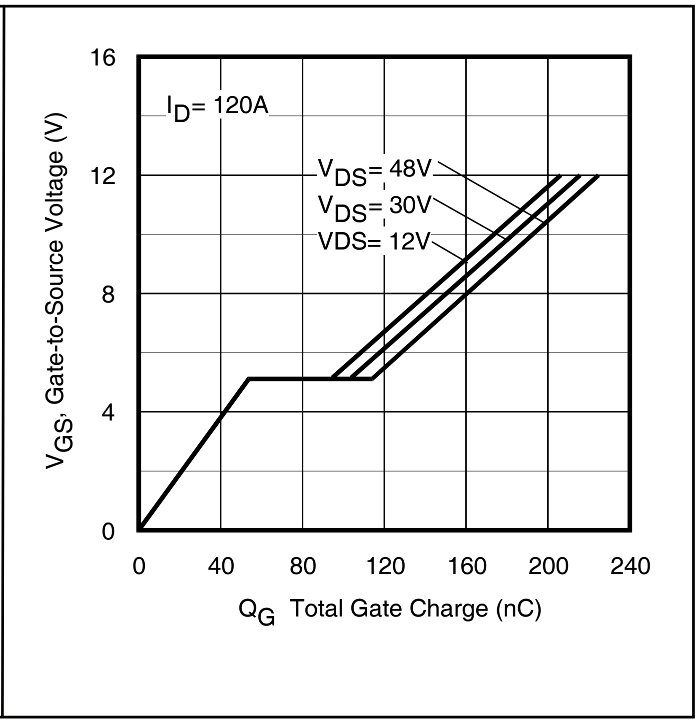
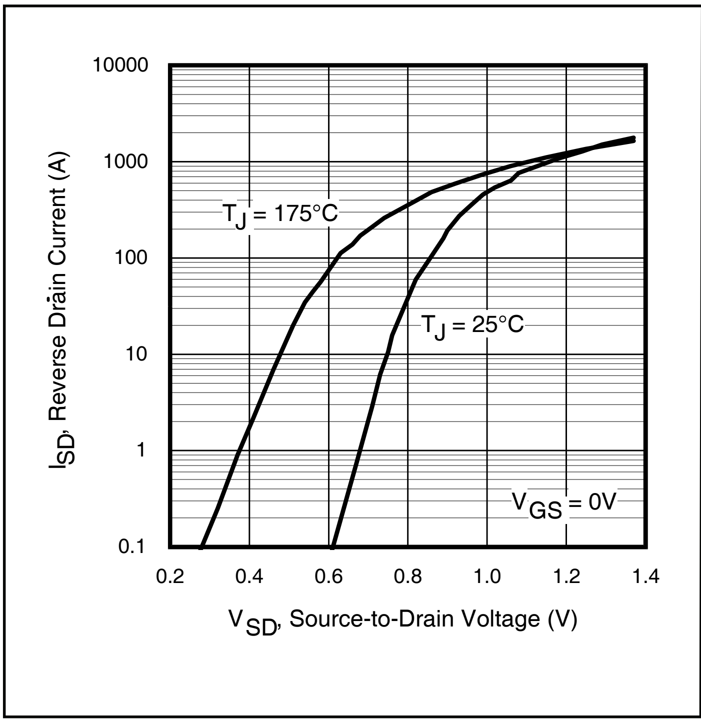


Figure 7 **Typical Capacitance vs. Drain-to-Source Voltage**

Figure 8 **Typical Gate Charge vs. Gate-to-Source Voltage**



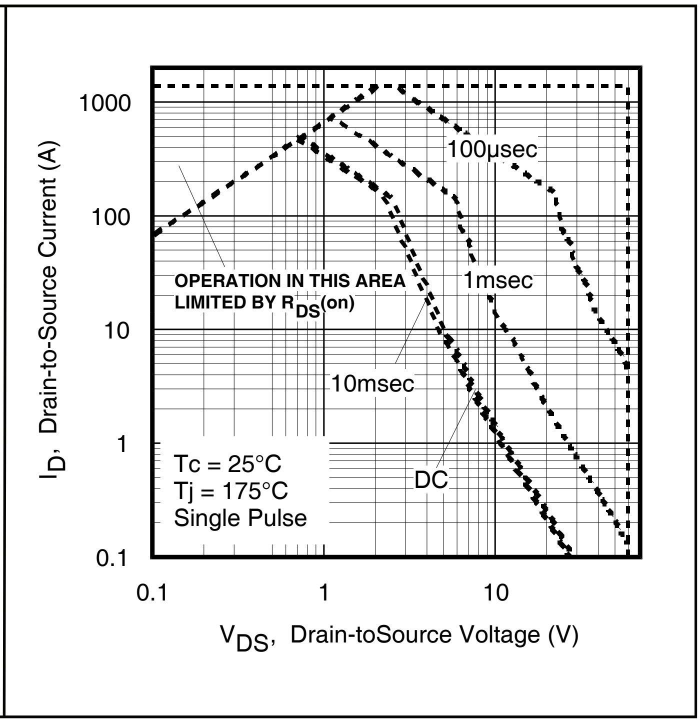


Figure 9 **Typical Source-Drain Diode Forward Voltage**

Figure 10 **Maximum Safe Operating Area**

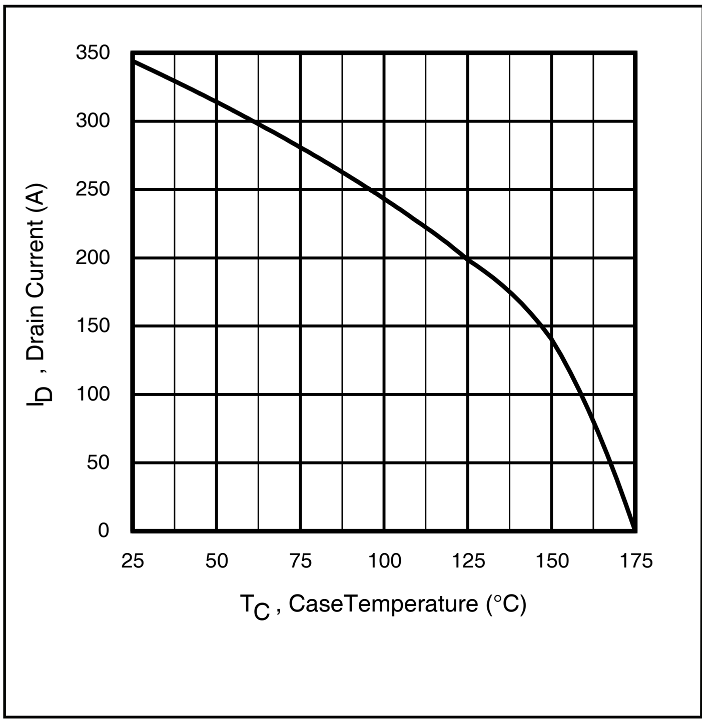


Figure 11 Maximum Drain Current vs. Case Temperature

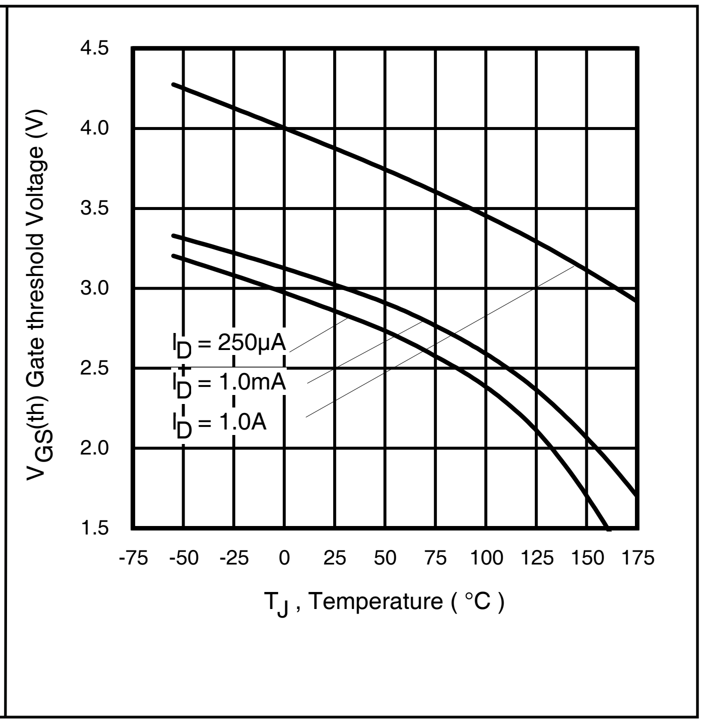


Figure 12 Typical Threshold Voltage vs. Junction Temperature

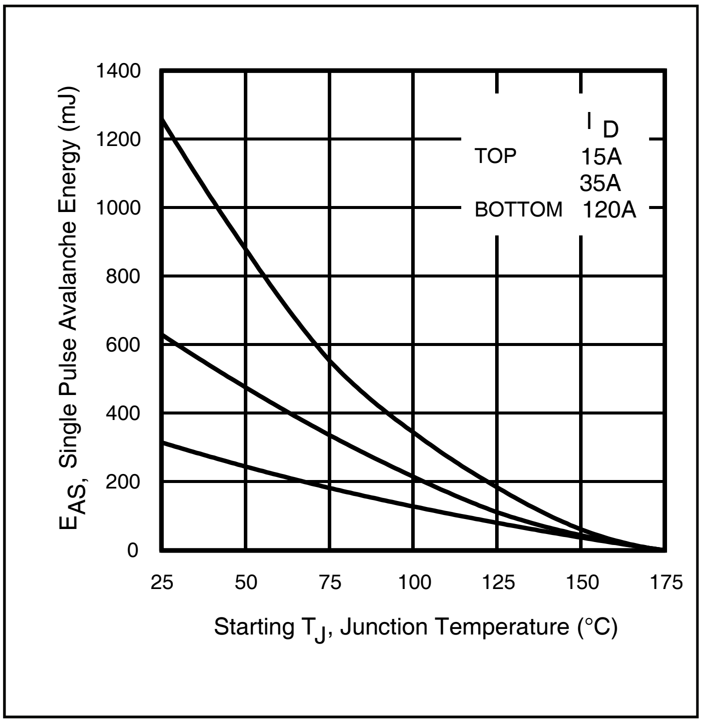


Figure 13 Maximum Avalanche Energy vs. Temperature

Electrical characteristic diagrams

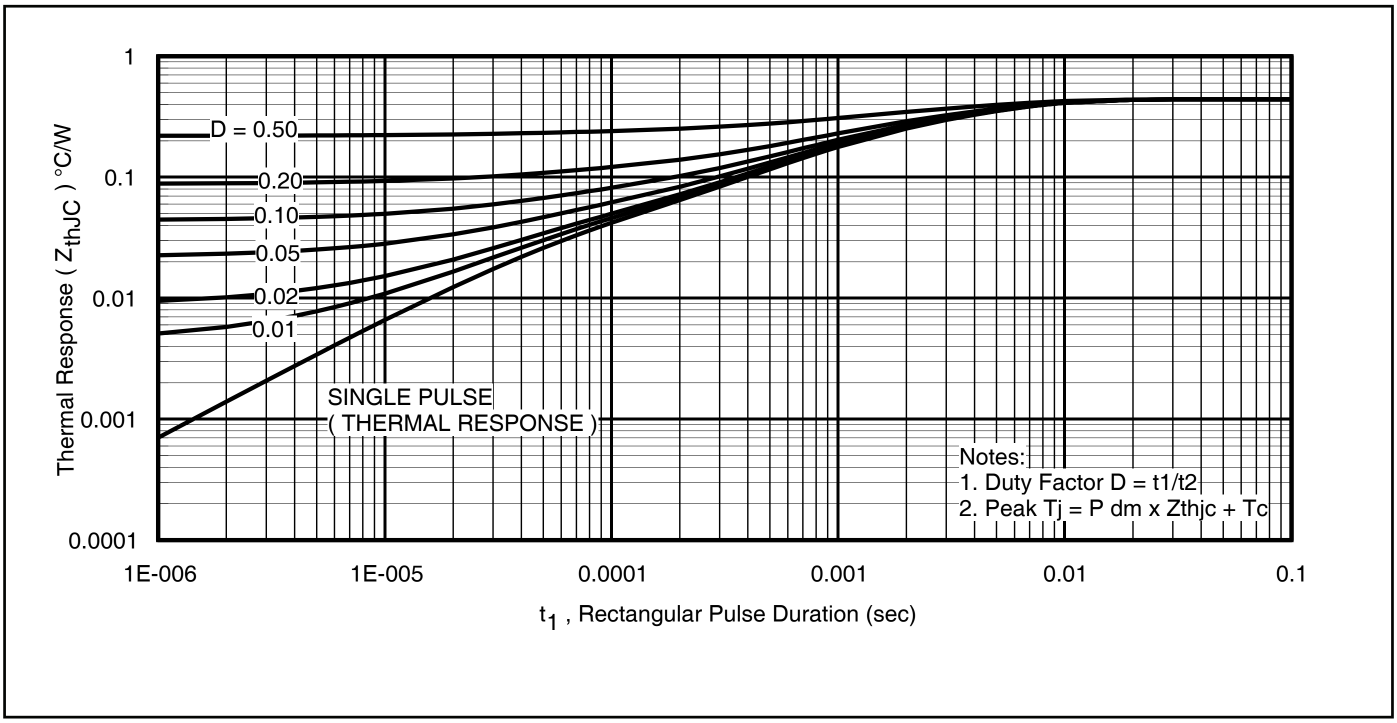


Figure 14 Maximum Effective Transient Thermal Impedance, Junction-to-Case

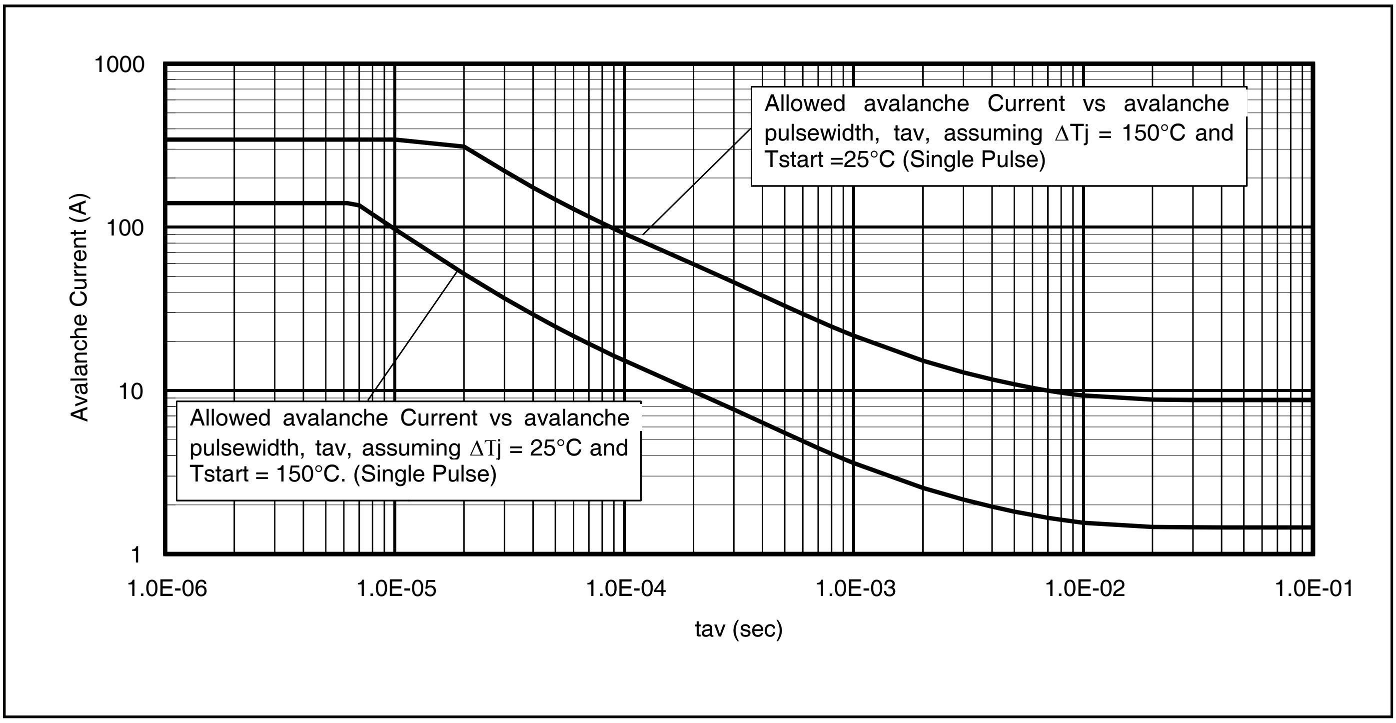


Figure 15 Typical Avalanche Current vs. Pulse Width

Electrical characteristic diagrams

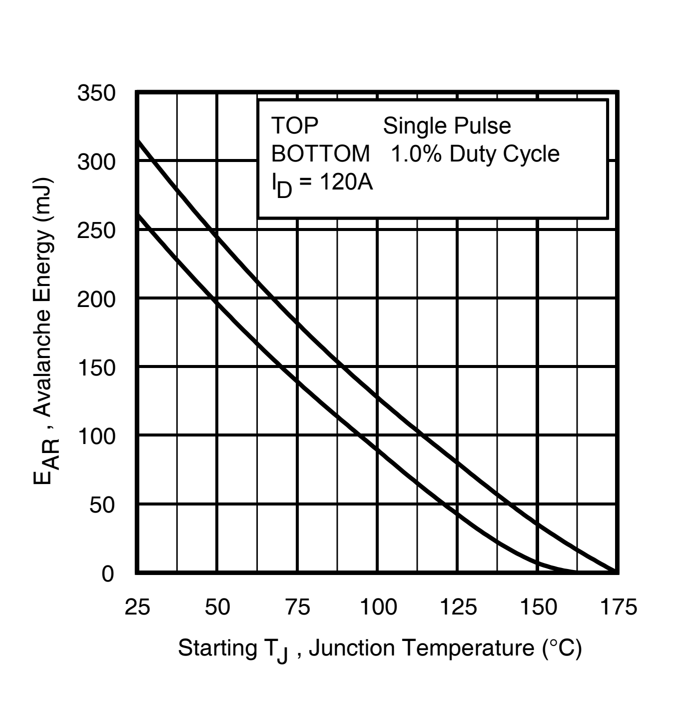


Figure 16 Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.infineon.com)

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 19a, 19b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. DT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.
D = Duty cycle in avalanche = tav ·f
$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

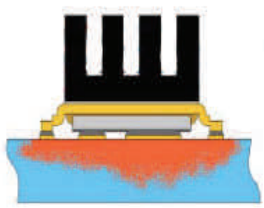
$$PD\ (ave) = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Notes:

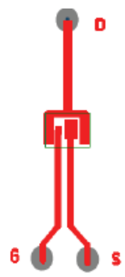
❷ Used double sided cooling , mounting pad with large heatsink
❸ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

❹ TC measured with thermocouple mounted to top (Drain) of part.

❶ Surface mounted on 1 in. square Cu board (still air).



❷ Mounted to a PCB with small clip heatsink (still air).



❸ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

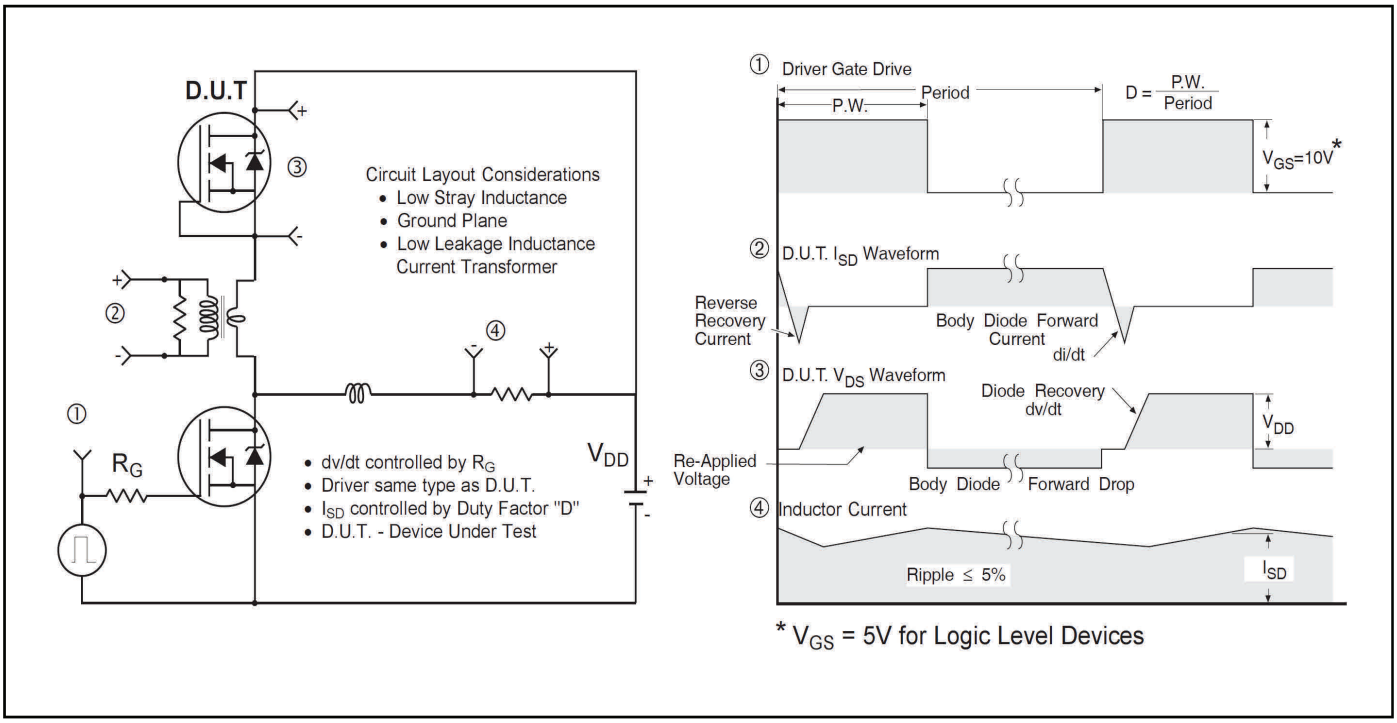


Figure 17 Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET™ Power MOSFETs

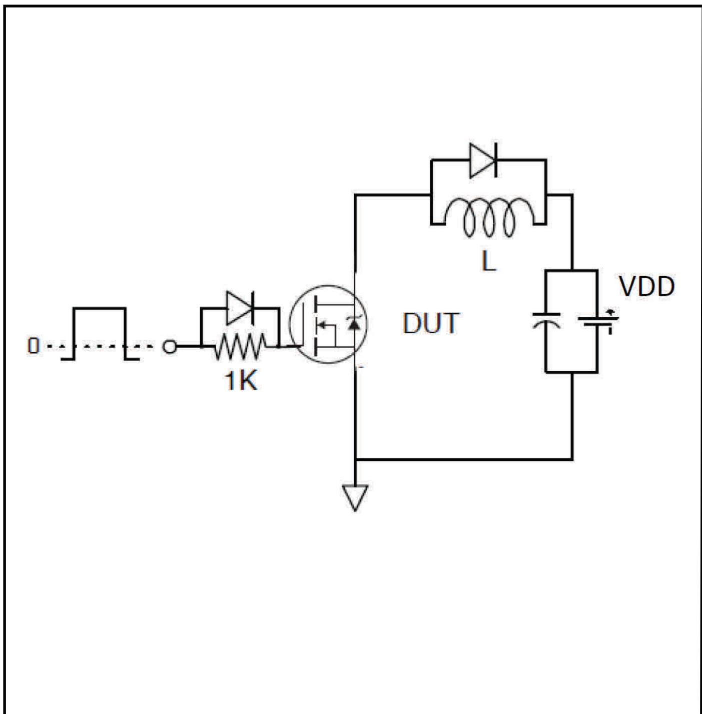


Figure 18a Gate Charge Test Circuit

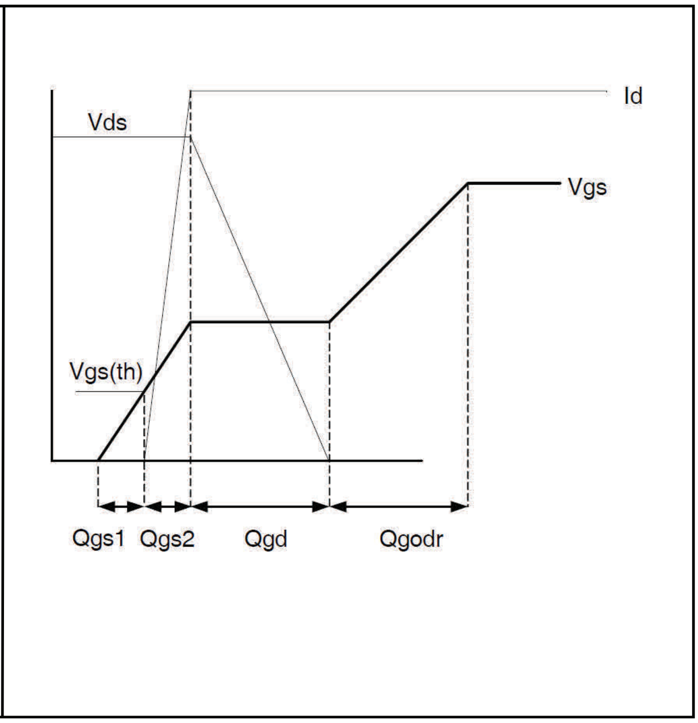
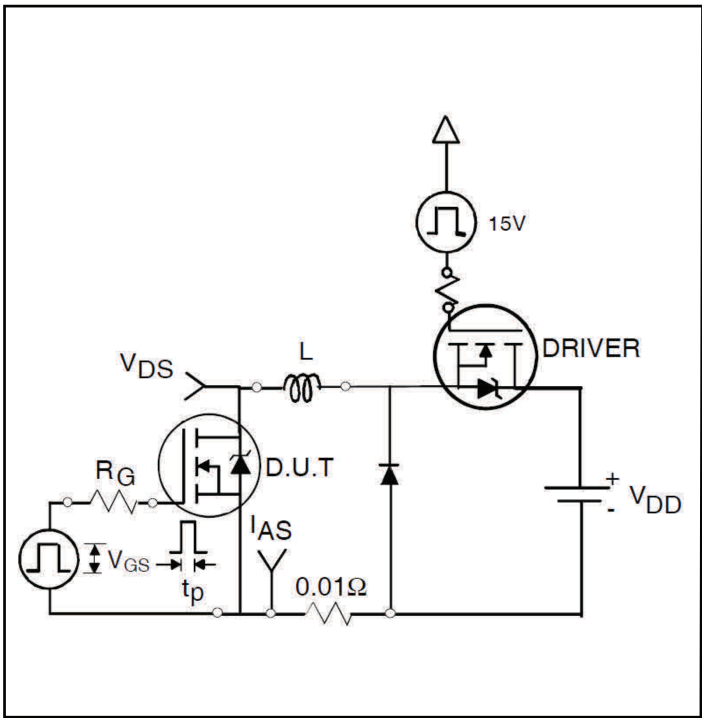


Figure 18b Gate Charge Waveform



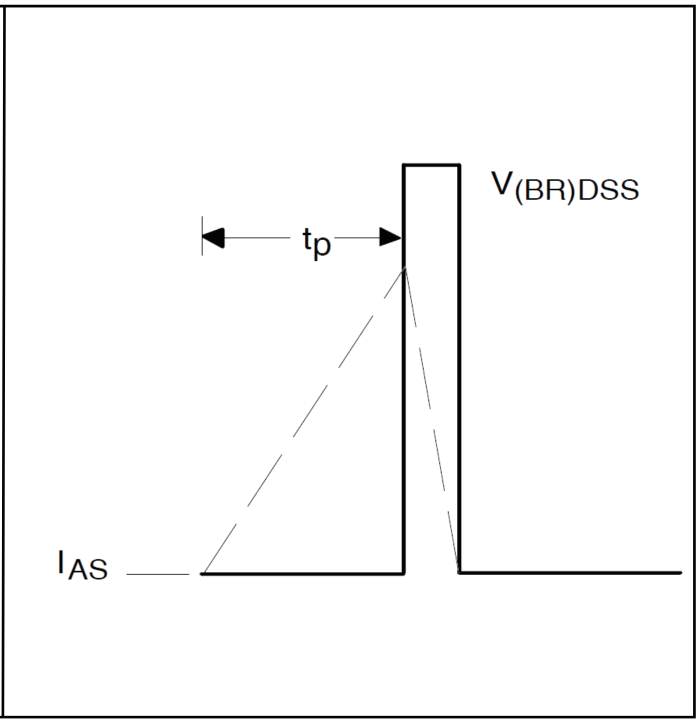
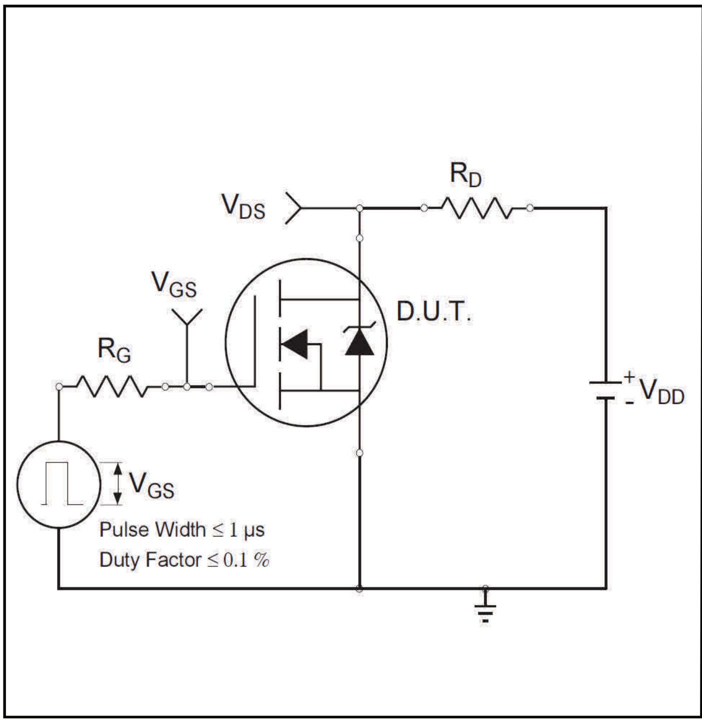


Figure 19a **Unclamped Inductive Test Circuit**

Figure 19b **Unclamped Inductive Waveforms**



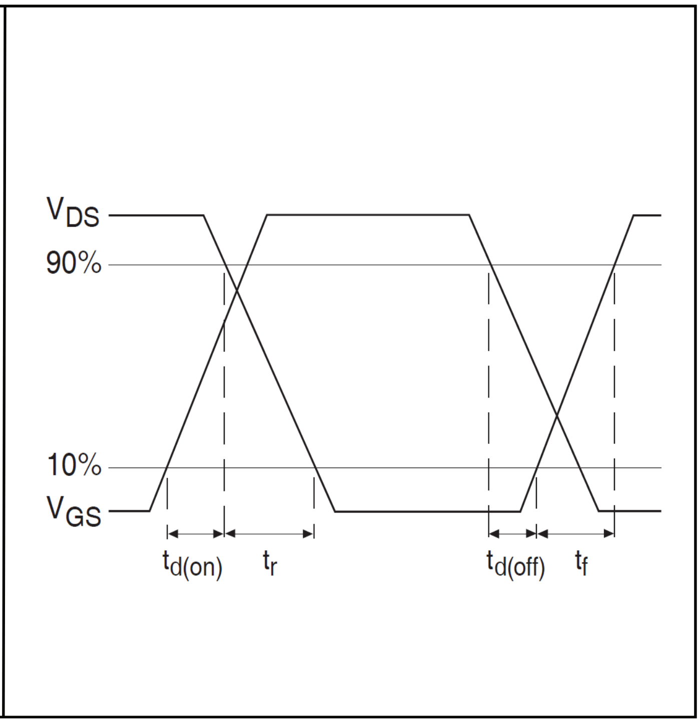
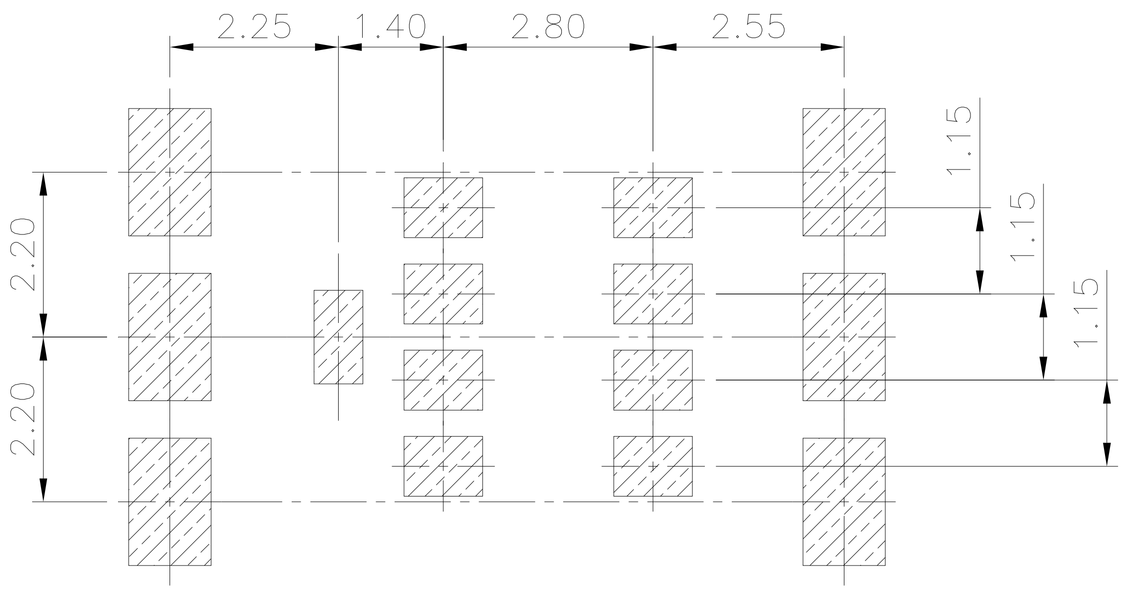


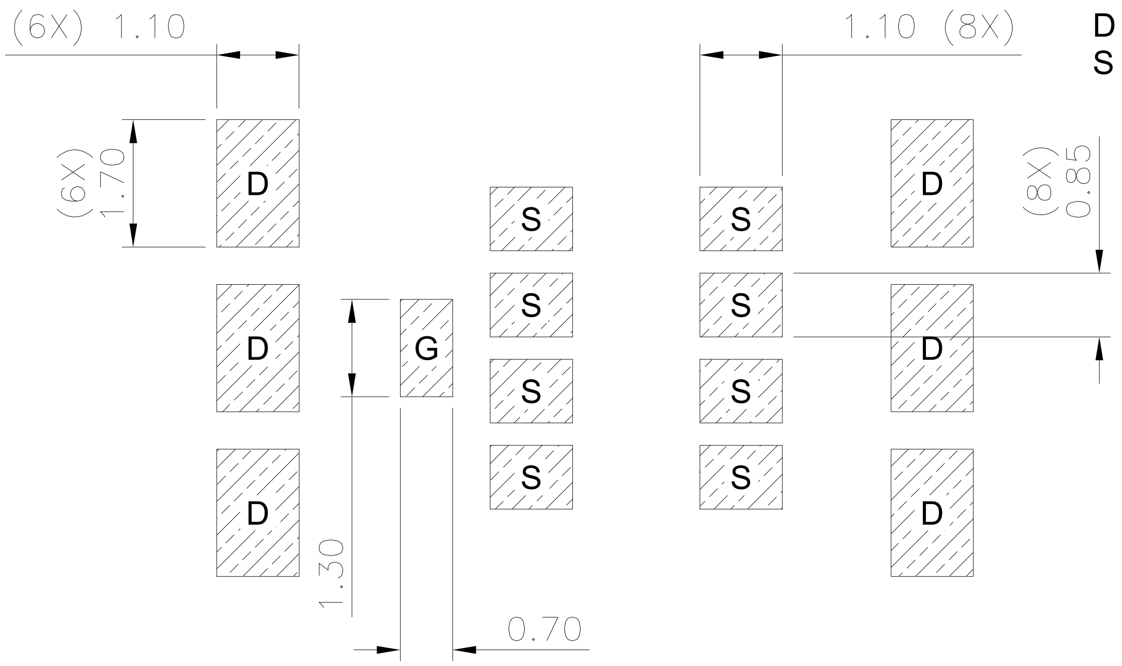
Figure 20a **Switching Time Test Circuit**

Figure 20b **Switching Time Waveforms**

5 Package Information

DirectFET™ Board Footprint, L8 Outline
(Large Size Can, 8-Source Pads)
Please see DirectFET™ application note AN-1035 for all details regarding the assembly of DirectFET™.
This includes all recommendations for stencil and substrate designs.

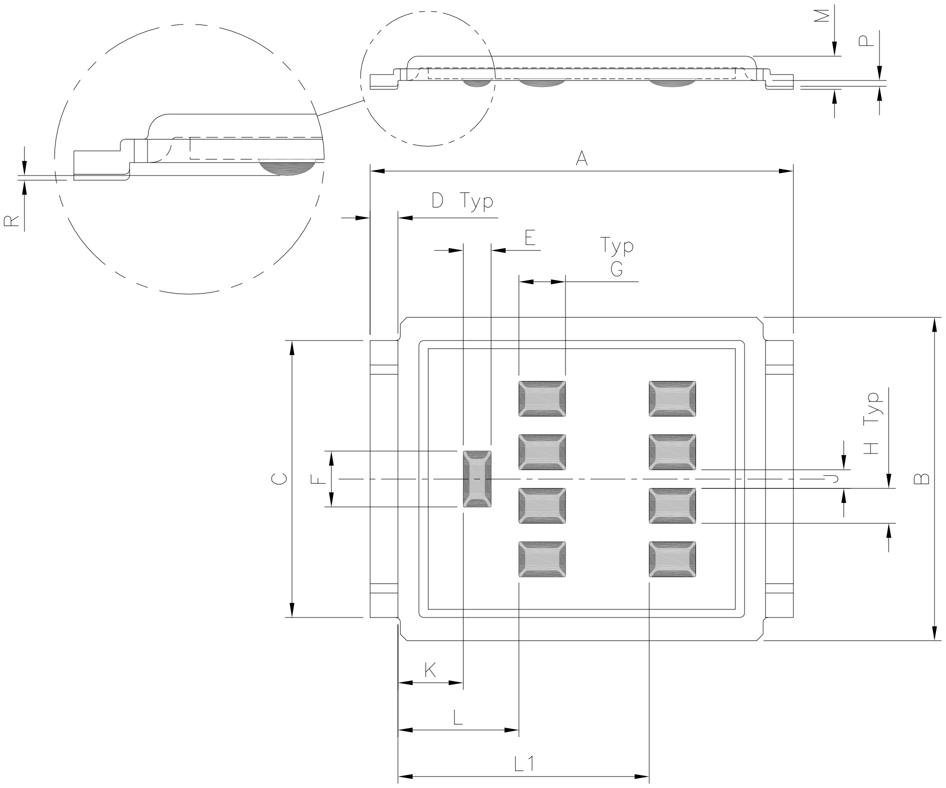




Package Information

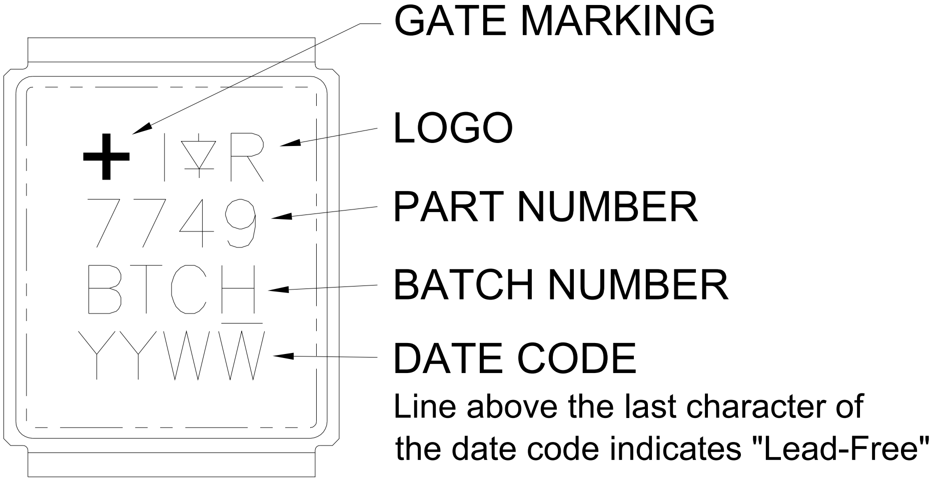
DirectFET™ Outline Dimension, L8 Outline (Large Size Can, 8-Source Pads)

Please see DirectFET™ application note AN-1035 for all details regarding the assembly of DirectFET™. This includes all recommendations for stencil and substrate designs.



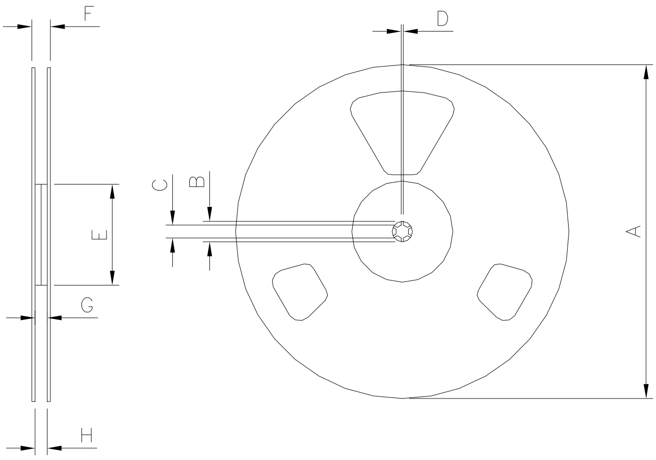
DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	9.05	9.15	0.356	0.360
B	6.85	7.10	0.270	0.280
C	5.90	6.00	0.232	0.236
D	0.55	0.65	0.022	0.026
E	0.58	0.62	0.023	0.024
F	1.18	1.22	0.046	0.048
G	0.98	1.02	0.039	0.040
H	0.73	0.77	0.029	0.030
J	0.38	0.42	0.015	0.017
K	1.35	1.45	0.053	0.057
L	2.55	2.65	0.100	0.104
L1	5.35	5.45	0.211	0.215
M	0.68	0.74	0.027	0.029
P	0.09	0.17	0.003	0.007
R	0.02	0.08	0.001	0.003

DirectFET™ Part Marking



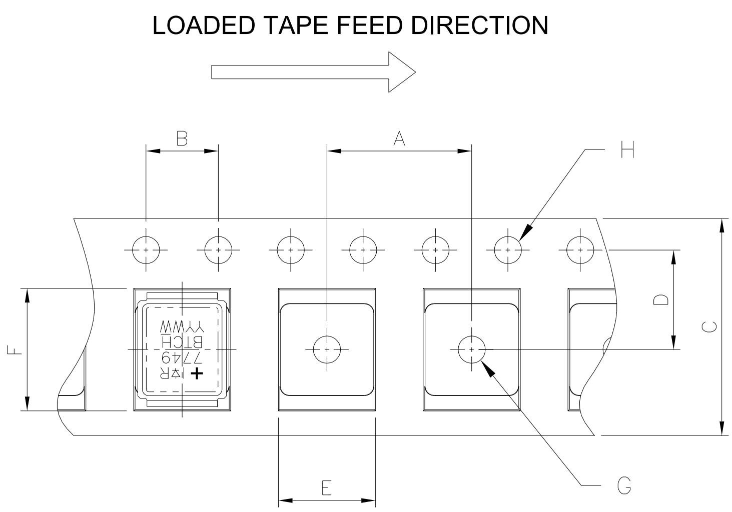
Tape & Reel Information

DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4000 parts. (ordered as IRF7749L1TRPBF).

REEL DIMENSIONS				
STANDARD OPTION **(QTY 4000)**				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	330.00	N.C	12.992	N.C
B	20.20	N.C	0.795	N.C
C	12.80	13.20	0.504	0.520
D	1.50	N.C	0.059	N.C
E	99.00	100.00	3.900	3.940
F	N.C	22.40	N.C	0.880
G	16.40	18.40	0.650	0.720
H	15.90	19.40	0.630	0.760



NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	11.90	12.10	4.69	0.476
B	3.90	4.10	0.154	0.161
C	15.90	16.30	0.623	0.642
D	7.40	7.60	0.291	0.299
E	7.20	7.40	0.283	0.291
F	9.90	10.10	0.390	0.398
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

6 Qualification Information

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	DirectFET™ Large Can	MSL1 (per JEDEC J-STD-020D)†
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Major changes since the last revision

Page or Reference	Revision	Date	Description of changes
All pages	2.0	2013-01-07	• First release Final data sheet.
All pages	2.1	2013-02-13	• TR1 option removed and Tape & Reel Info updated accordingly. Hyperlinks added throw-out the document
All pages	2.2	2019-02-20	• Update to R-Theta.

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