

# IRLS3034-7PPbF

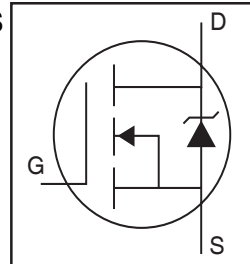
HEXFET® Power MOSFET

## Applications

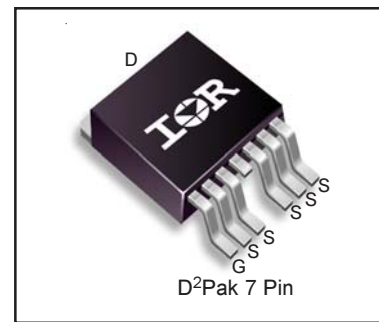
- DC Motor Drive
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

## Benefits

- Optimized for Logic Level Drive
- Very Low  $R_{DS(ON)}$  at 4.5V  $V_{GS}$
- Superior  $R \cdot Q$  at 4.5V  $V_{GS}$
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode  $dV/dt$  and  $dI/dt$  Capability
- Lead-Free



$V_{DSS}$		<b>40V</b>
$R_{DS(on)}$	typ.	<b>1.0mΩ</b>
	max.	<b>1.4mΩ</b>
$I_D$ (Silicon Limited)		<b>380A</b> ①
$I_D$ (Package Limited)		<b>240A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	380①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	270①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	240	
$I_{DM}$	Pulsed Drain Current ②	1540	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	380	W
	Linear Derating Factor	2.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$dv/dt$	Peak Diode Recovery ④	1.3	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

## Avalanche Characteristics

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	250	mJ
$I_{AR}$	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy ②		mJ

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤⑥	—	0.40	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	40	

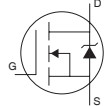
Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.035	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 5mA$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.0	1.4	m $\Omega$	$V_{GS} = 10V, I_D = 200A$ ⑤
		—	1.2	1.7		$V_{GS} = 4.5V, I_D = 180A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$R_G$	Internal Gate Resistance	—	1.9	—	$\Omega$	

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

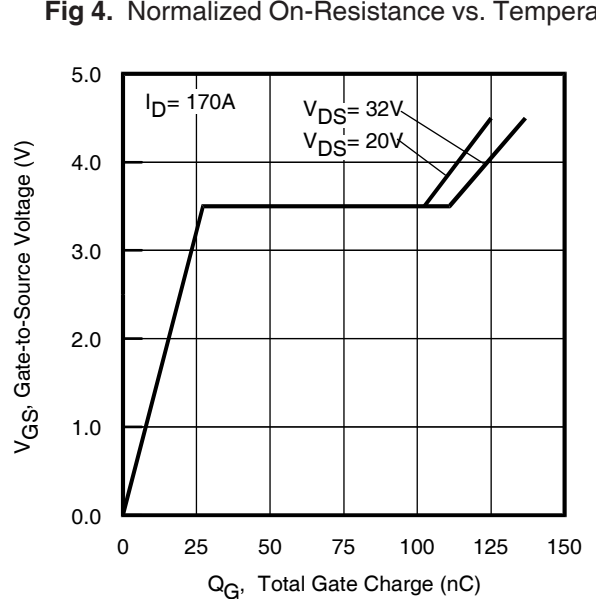
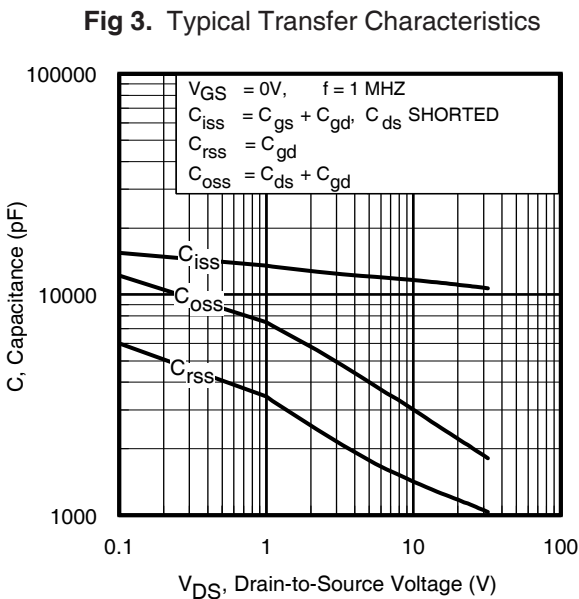
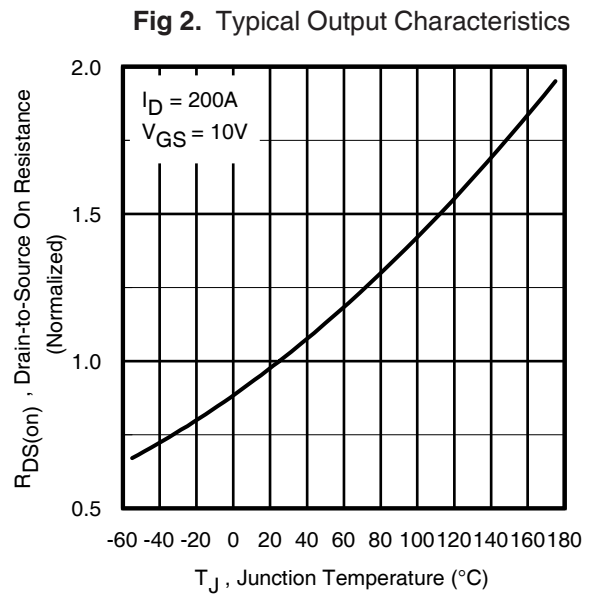
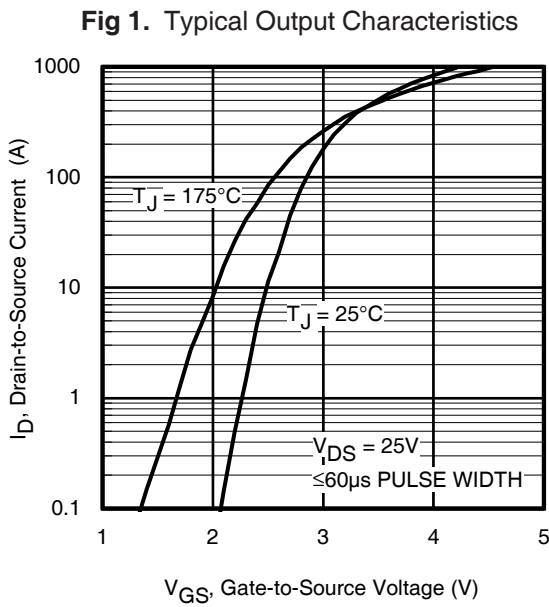
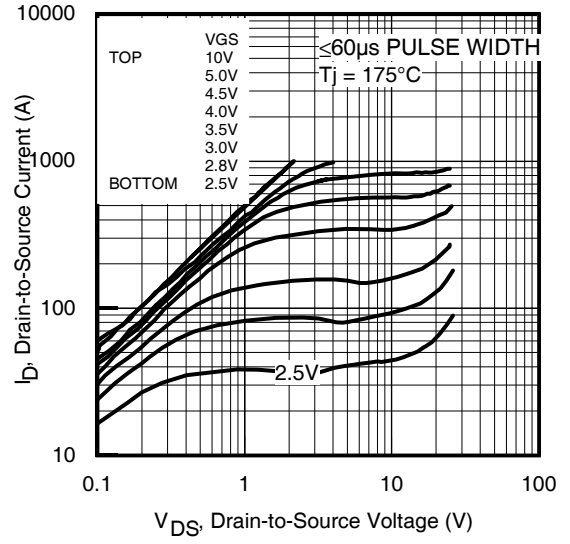
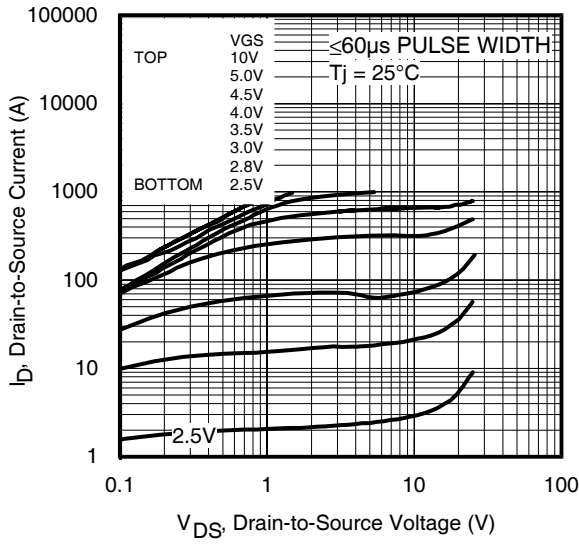
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	370	—	—	S	$V_{DS} = 10V, I_D = 220A$
$Q_g$	Total Gate Charge	—	120	180	nC	$I_D = 170A$
$Q_{gs}$	Gate-to-Source Charge	—	32	—		$V_{DS} = 20V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	71	—		$V_{GS} = 4.5V$ ⑤
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	49	—		$I_D = 170A, V_{DS} = 0V, V_{GS} = 4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	71	—	ns	$V_{DD} = 26V$
$t_r$	Rise Time	—	590	—		$I_D = 220A$
$t_{d(off)}$	Turn-Off Delay Time	—	94	—		$R_G = 2.7\Omega$
$t_f$	Fall Time	—	200	—		$V_{GS} = 4.5V$ ⑤
$C_{iss}$	Input Capacitance	—	10990	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	2030	—		$V_{DS} = 40V$
$C_{riss}$	Reverse Transfer Capacitance	—	1100	—		$f = 1.0MHz$ , See Fig. 5
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	2520	—		$V_{GS} = 0V, V_{DS} = 0V$ to $32V$ ⑦, See Fig. 11
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑧	—	3060	—		$V_{GS} = 0V, V_{DS} = 0V$ to $32V$ ⑧

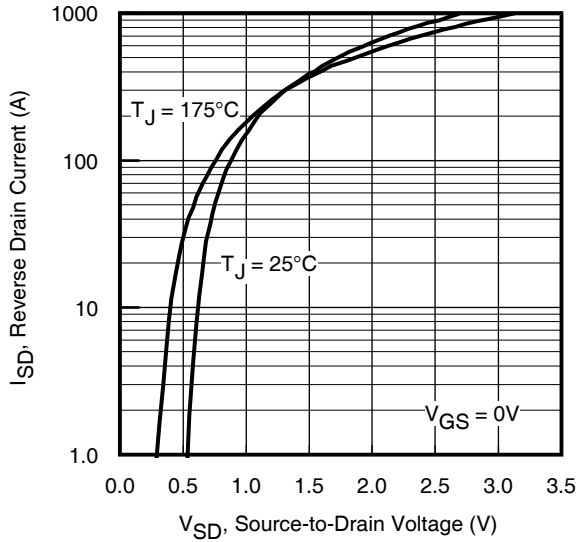
## Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	380①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ②	—	—	1540	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 200A, V_{GS} = 0V$ ⑤
$t_{rr}$	Reverse Recovery Time	—	46	—	ns	$T_J = 25^\circ\text{C}$
		—	49	—		$T_J = 125^\circ\text{C}$
$Q_{rr}$	Reverse Recovery Charge	—	100	—	nC	$T_J = 25^\circ\text{C}$
		—	110	—		$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	3.7	—	A	$T_J = 25^\circ\text{C}$
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

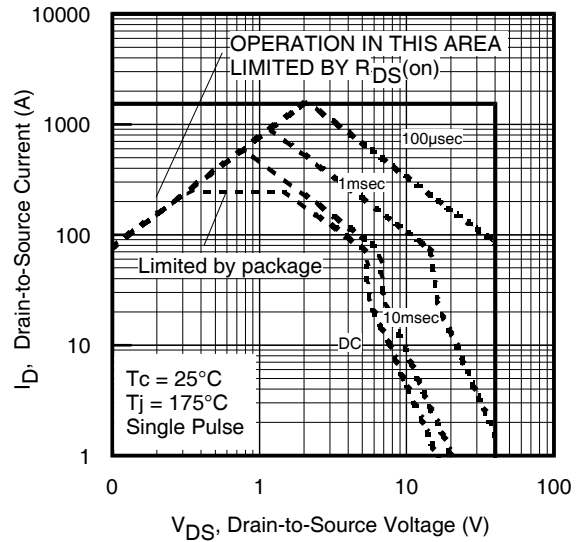
## Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.010mH$   
 $R_G = 25\Omega, I_{AS} = 220A, V_{GS} = 10V$ . Part not recommended for use above this value .
- ④  $I_{SD} \leq 220A, di/dt \leq 1240A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss \text{ eff. (TR)}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss \text{ eff. (ER)}}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑩  $R_{\theta JC}$  value shown is at time zero.

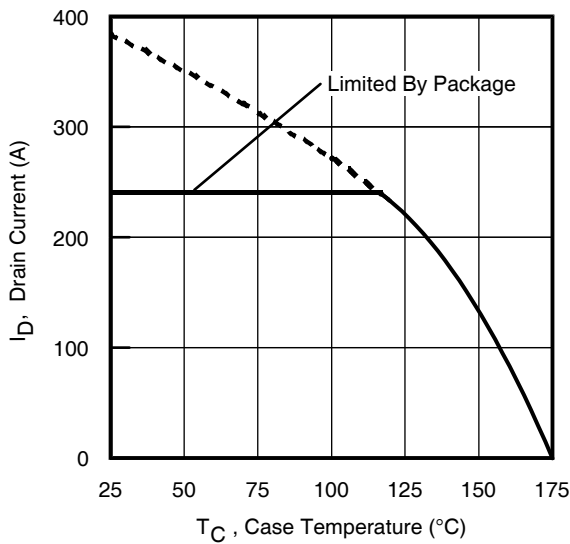




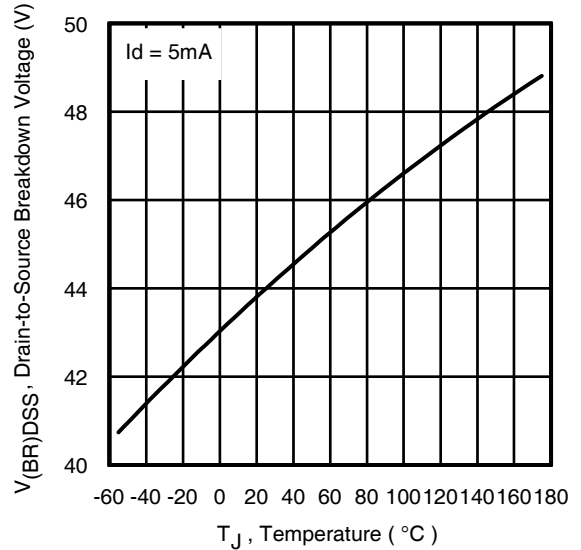
**Fig 7.** Typical Source-Drain Diode Forward Voltage



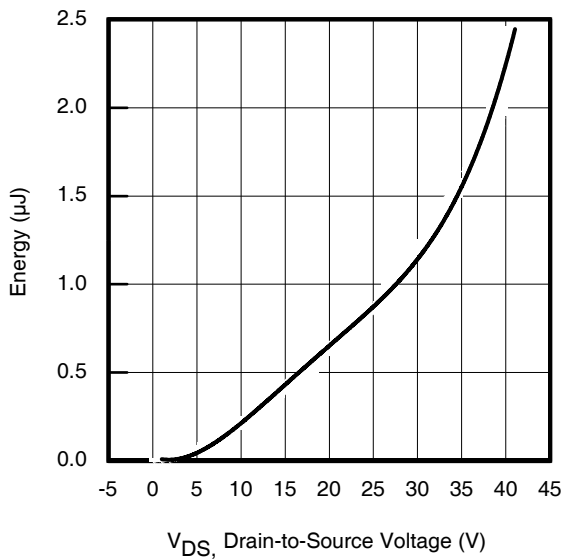
**Fig 8.** Maximum Safe Operating Area



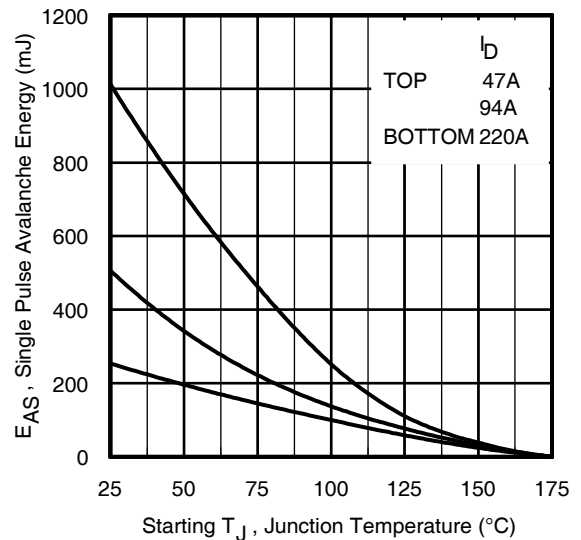
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy Vs. DrainCurrent

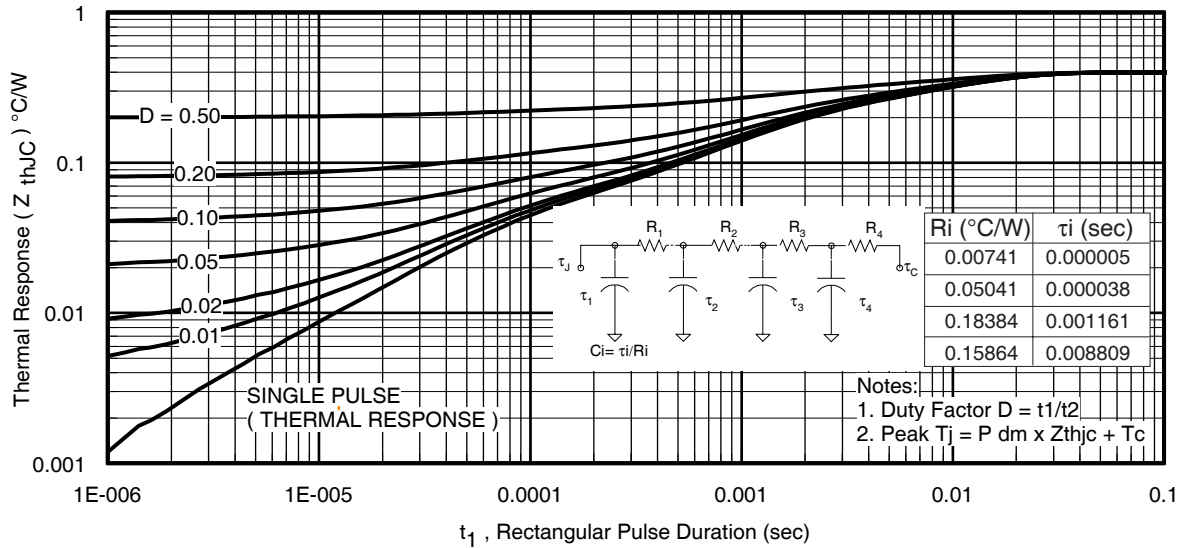


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

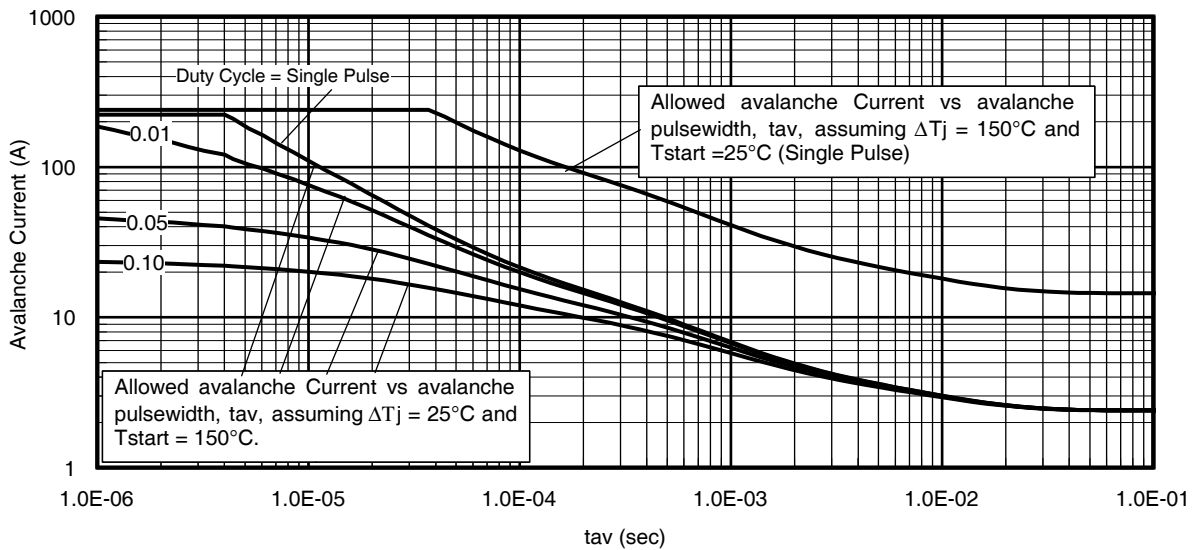
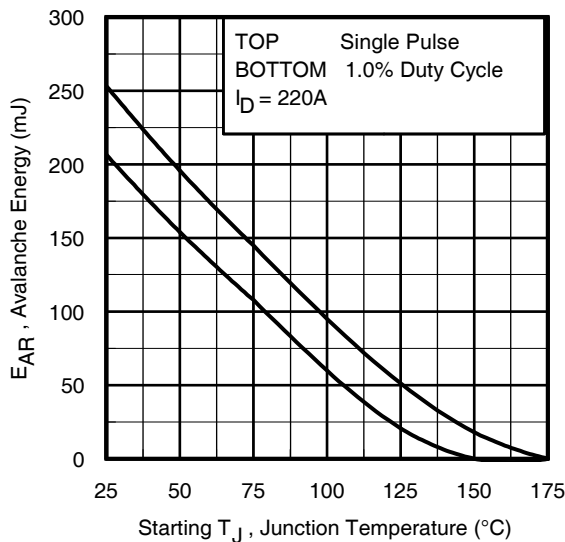


Fig 14. Typical Avalanche Current vs. Pulsewidth



**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

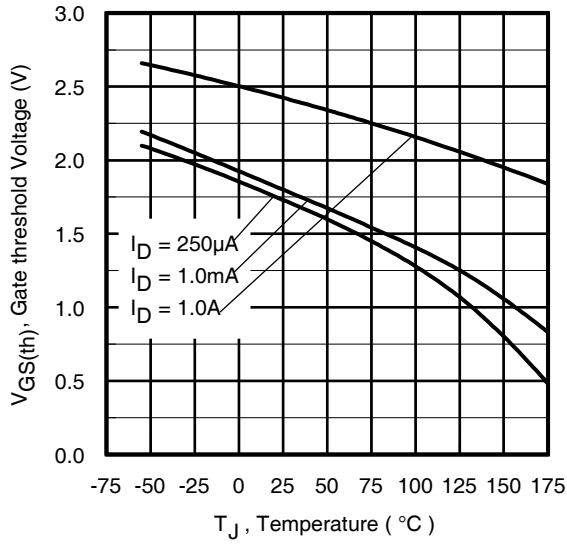


Fig 16. Threshold Voltage vs. Temperature

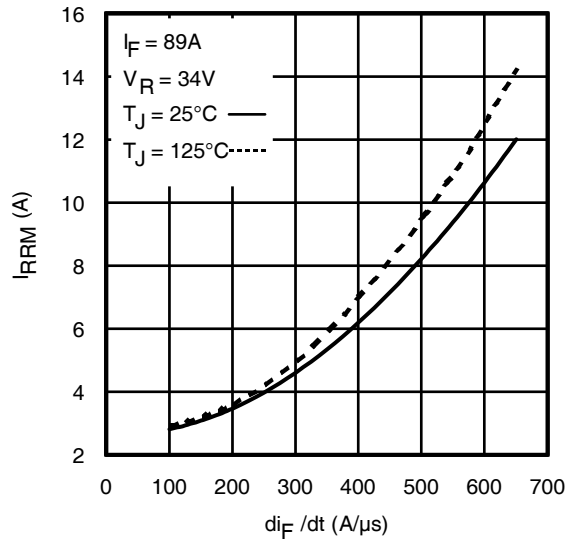


Fig. 17 - Typical Recovery Current vs.  $di/dt$

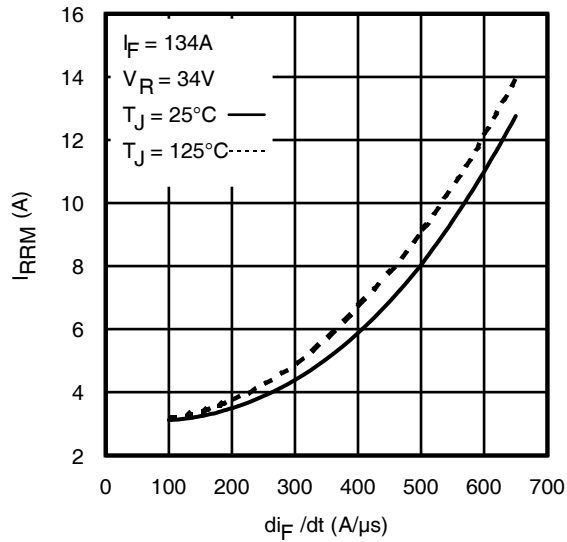


Fig. 18 - Typical Recovery Current vs.  $di/dt$

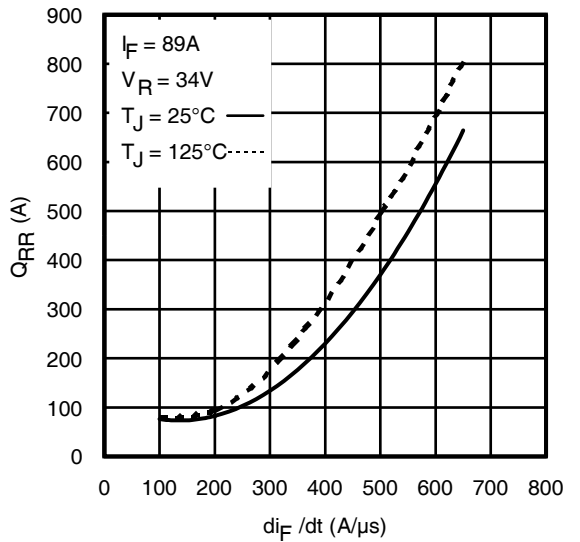


Fig. 19 - Typical Stored Charge vs.  $di/dt$

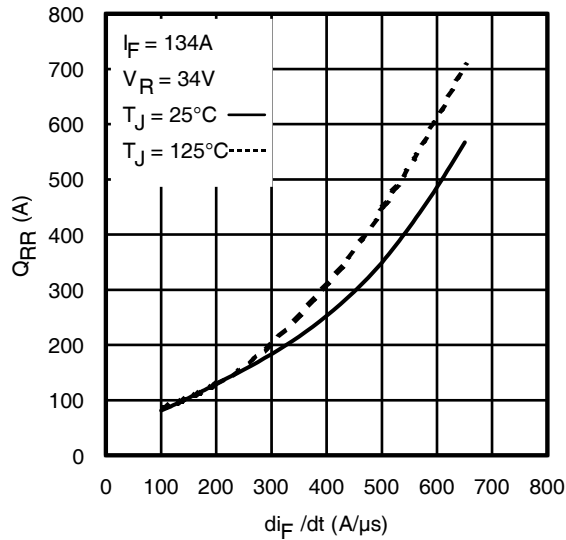
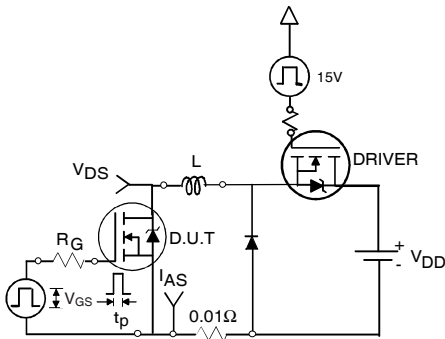


Fig. 20 - Typical Stored Charge vs.  $di/dt$



\*  $V_{GS} = 5V$  for Logic Level Devices

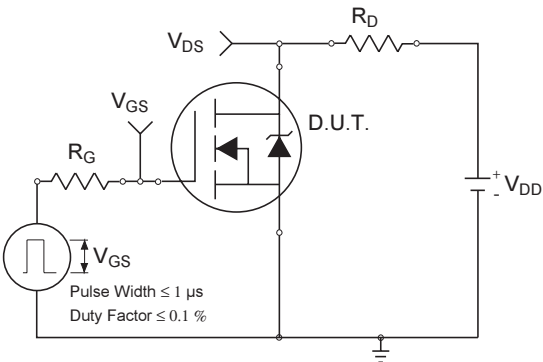
**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**



**Fig 22a. Unclamped Inductive Test Circuit**



**Fig 22b. Unclamped Inductive Waveforms**



**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



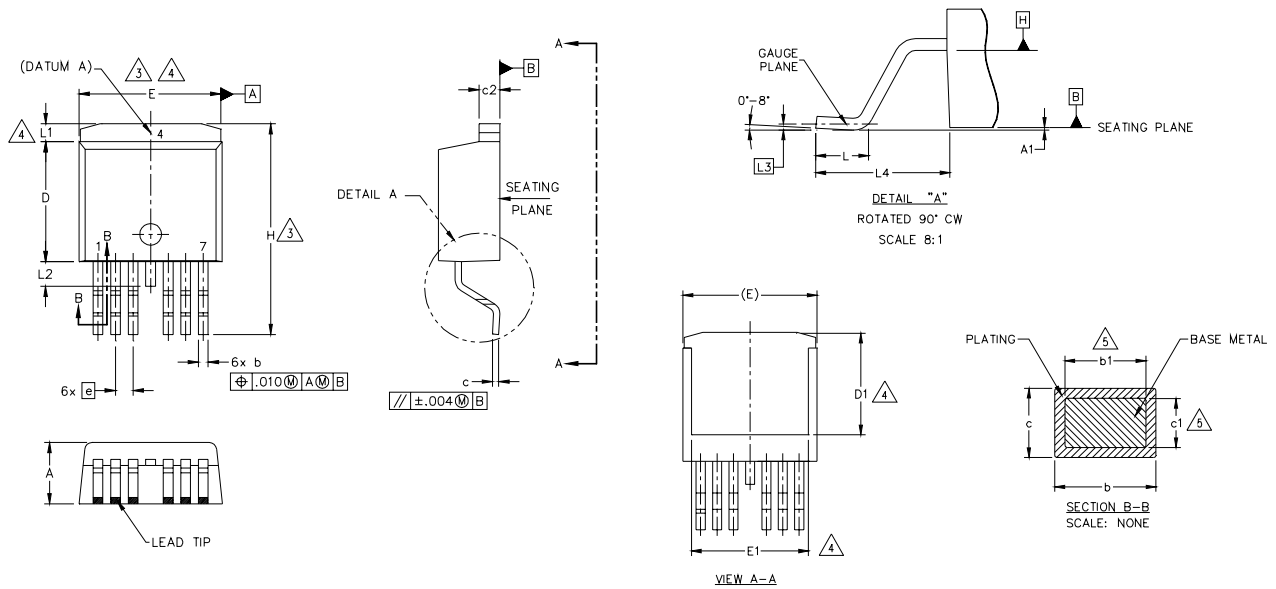
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

D<sup>2</sup>Pak - 7 Pin Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	-	0.254	-	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	
E	9.65	10.67	.380	.420	
E1	6.22	-	.245	-	4
e	1.27 BSC		.050 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.68	-	.066	
L2	-	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.

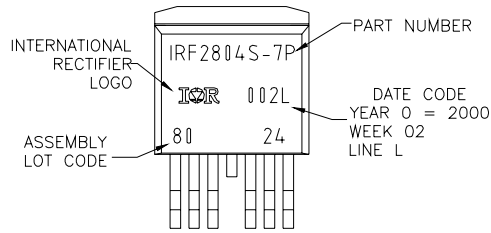
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



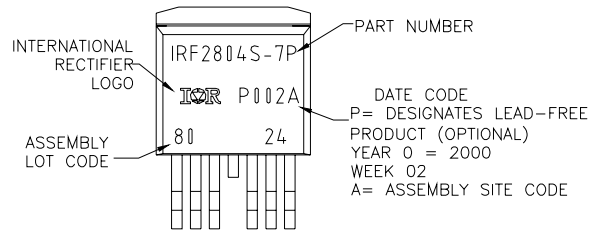
## D<sup>2</sup>Pak - 7 Pin Part Marking Information

EXAMPLE: THIS IS AN IRF2804S-7P WITH  
 LOT CODE 8024  
 ASSEMBLED ON WW02,2000  
 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line  
 position indicates "Lead Free"



OR

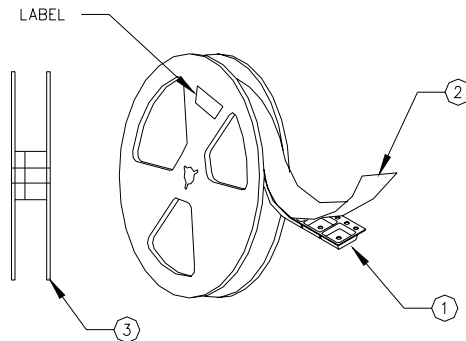
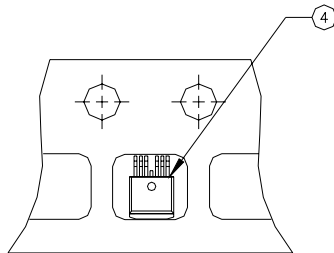


## D<sup>2</sup>Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
  - 1.1 REEL SIZE 13 INCH DIAMETER.
  - 1.2 EACH REEL CONTAINING 800 DEVICES.
  - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
  - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
  - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
  - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).
  - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
  - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
  - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
  - 2.4 QUANTITY:
  - 2.5 VENDOR CODE: IR
  - 2.6 LOT CODE:
  - 2.7 DATE CODE:



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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