

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use salesaddresses@nexperia.com (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via salesaddresses@nexperia.com). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia



PBL6022D

60 V, 1.5 A PNP BISS loadswitch

Rev. 01 — 13 August 2009

Product data sheet

1. Product profile

1.1 General description

PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

1.2 Features

- Low V_{CEsat} (BISS) and resistor-equipped transistor in one package
- Low threshold voltage (<1 V) compared to MOSFET
- Space-saving solution
- Reduction of component count
- AEC-Q101 qualified

1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

1.4 Quick reference data

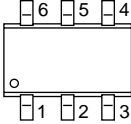
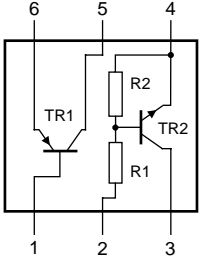
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-60	V
I_C	collector current		-	-	-1.5	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-3	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1.5$ A; $I_B = -100$ mA	[1]	110	175	m Ω
TR2; NPN resistor-equipped transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)		3.3	4.7	6.1	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	base TR1		
2	input (base) TR2		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	collector TR1		
6	emitter TR1		

006aab506

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBLS6022D	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PBLS6022D	KF

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
TR1; PNP low V_{CEsat} transistor						
V_{CBO}	collector-base voltage	open emitter	-	-60	V	
V_{CEO}	collector-emitter voltage	open base	-	-60	V	
V_{EBO}	emitter-base voltage	open collector	-	-5	V	
I_C	collector current		-	-1.5	A	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-3	A	
I_B	base current		-	-300	mA	
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms	-	-1	A	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	370	mW
			[2]	-	480	mW
			[3]	-	630	mW
TR2; NPN resistor-equipped transistor						
V_{CBO}	collector-base voltage	open emitter	-	50	V	
V_{CEO}	collector-emitter voltage	open base	-	50	V	
V_{EBO}	emitter-base voltage	open collector	-	10	V	
V_I	input voltage					
		positive	-	+30	V	
		negative	-	-10	V	
I_O	output current		-	100	mA	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	100	mA	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1][2]	-	200	mW
			[3]			
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	480	mW
			[2]	-	590	mW
			[3]	-	760	mW
T_j	junction temperature		-	150	°C	
T_{amb}	ambient temperature		-55	+150	°C	
T_{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per device						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	260 K/W
			[2]	-	-	211 K/W
			[3]	-	-	165 K/W
R _{th(j-sp)}	thermal resistance from junction to solder point		-	-	100 K/W	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

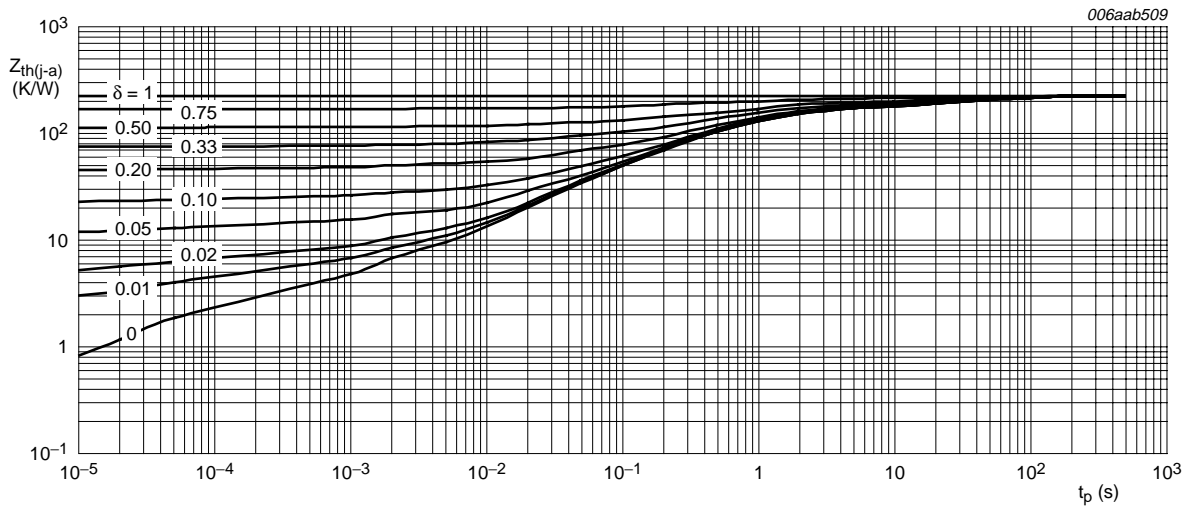
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



FR4 PCB, standard footprint

Fig 2. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm²

Fig 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



7. Characteristics

Table 7. Characteristics

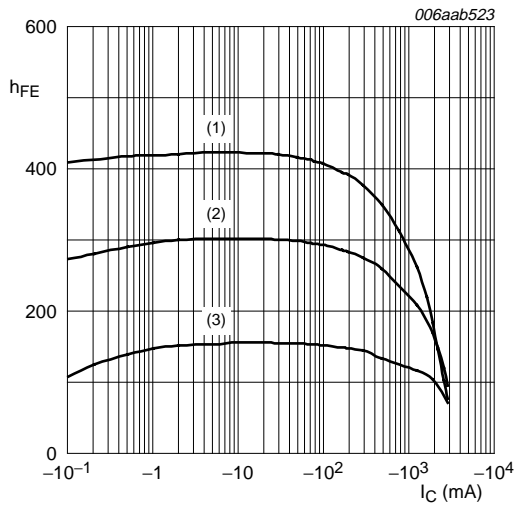
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
I _{CBO}	collector-base cut-off current	V _{CB} = -60 V; I _E = 0 A	-	-	-100	nA
		V _{CB} = -60 V; I _E = 0 A; T _j = 150 °C	-	-	-50	μA
I _{CES}	collector-emitter cut-off current	V _{CE} = -48 V; V _{BE} = 0 A	-	-	-100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A	-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -2 V; I _C = -100 mA	180	285	-	
		V _{CE} = -2 V; I _C = -500 mA	[1] 150	255	-	
		V _{CE} = -2 V; I _C = -1 A	[1] 140	210	-	
		V _{CE} = -2 V; I _C = -1.5 A	[1] 120	185	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -0.5 A; I _B = -50 mA	[1] -	-65	-100	mV
		I _C = -1 A; I _B = -50 mA	[1] -	-130	-200	mV
		I _C = -1 A; I _B = -100 mA	[1] -	-110	-170	mV
		I _C = -1.5 A; I _B = -100 mA	[1] -	-165	-260	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -1 A; I _B = -100 mA	[1] -	110	170	mΩ
		I _C = -1.5 A; I _B = -100 mA	[1] -	110	175	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = -0.5 A; I _B = -50 mA	[1] -	-0.85	-1	V
		I _C = -1.5 A; I _B = -100 mA	[1] -	-0.93	-1.1	V

Table 7. Characteristics ...continued
 $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified.

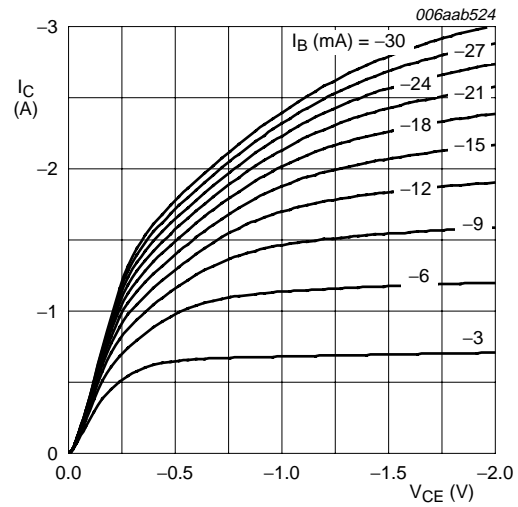
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -10\text{ V}; I_C = -1\text{ A}$	[1] -	-0.75	-1.1	V
t_d	delay time	$V_{CC} = -10\text{ V}; I_C = -1\text{ A};$	-	17	-	ns
t_r	rise time	$I_{Bon} = -50\text{ mA};$	-	38	-	ns
t_{on}	turn-on time	$I_{Boff} = 50\text{ mA}$	-	55	-	ns
t_s	storage time		-	350	-	ns
t_f	fall time		-	65	-	ns
t_{off}	turn-off time		-	415	-	ns
f_T	transition frequency	$I_C = -50\text{ mA}; V_{CE} = -10\text{ V};$ $f = 100\text{ MHz}$	-	150	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = i_e = 0\text{ A};$ $f = 1\text{ MHz}$	-	30	-	pF
TR2; NPN resistor-equipped transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A};$ $T_j = 150^{\circ}\text{C}$	-	-	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	900	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}$	30	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}$	-	1.1	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 20\text{ mA}$	2.5	1.9	-	V
R1	bias resistor 1 (input)		3.3	4.7	6.1	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A};$ $f = 1\text{ MHz}$	-	-	2.5	pF

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.



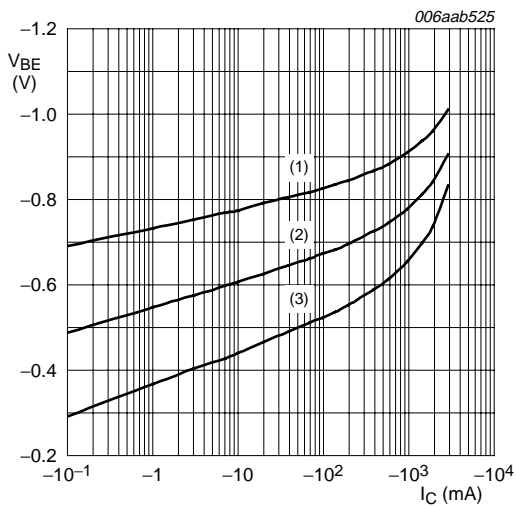
$V_{CE} = -2\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 5. TR1 (PNP): DC current gain as a function of collector current; typical values



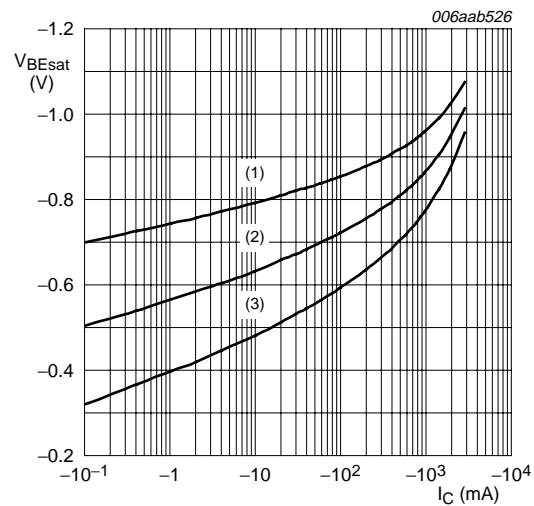
$T_{amb} = 25\text{ °C}$

Fig 6. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values



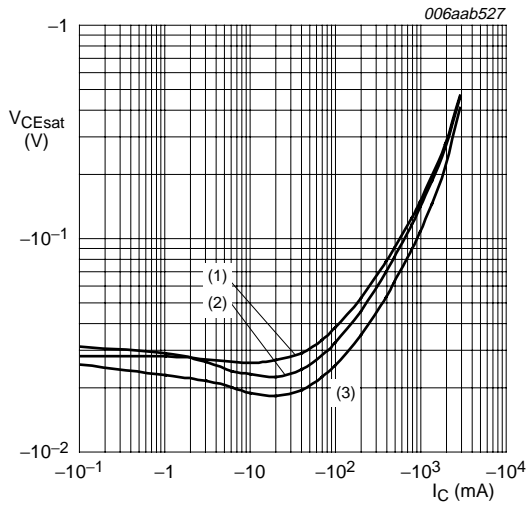
$V_{CE} = -2\text{ V}$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values



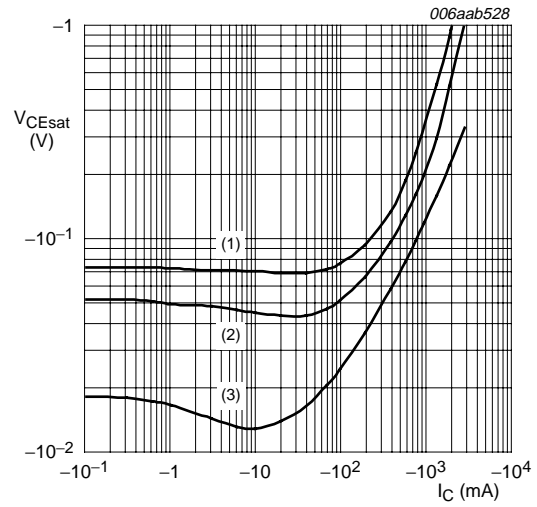
$I_C/I_B = 20$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



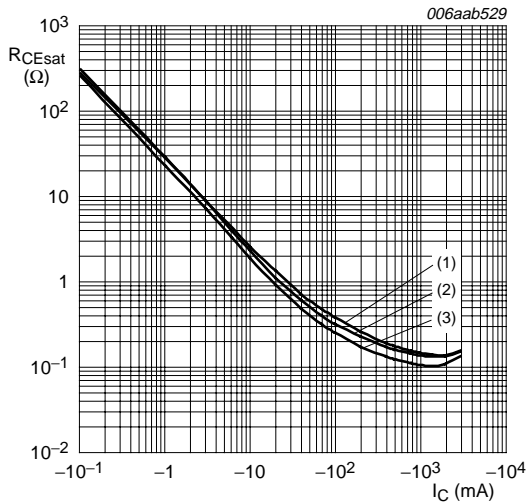
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -55\text{ °C}$

Fig 9. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



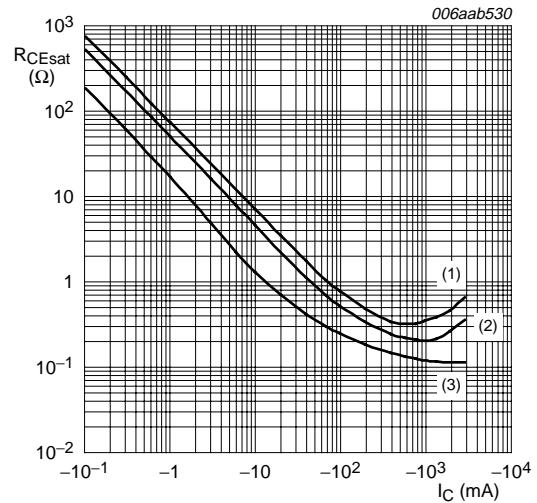
- $T_{amb} = 25\text{ °C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 10. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



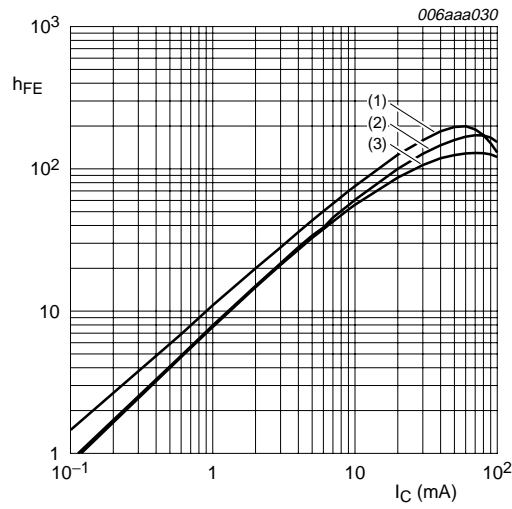
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -55\text{ °C}$

Fig 11. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



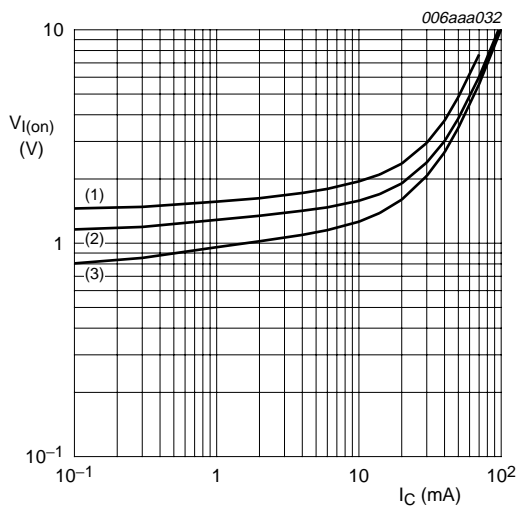
- $T_{amb} = 25\text{ °C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



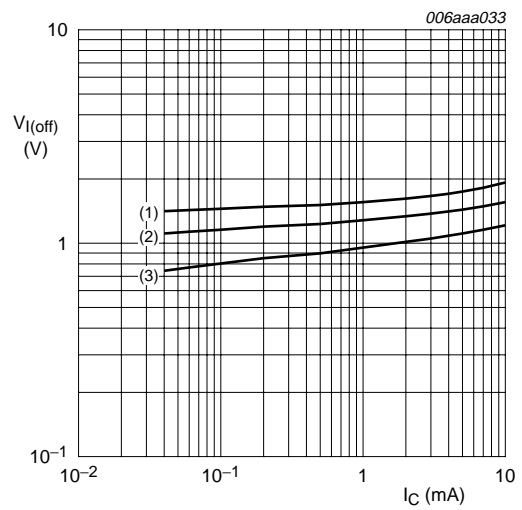
- $V_{CE} = 5\text{ V}$
- (1) $T_{amb} = 150\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -40\text{ °C}$

Fig 13. TR2 (NPN): DC current gain as a function of collector current; typical values



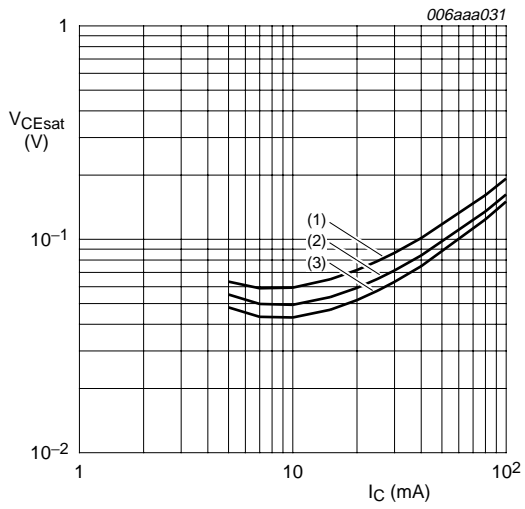
- $V_{CE} = 0.3\text{ V}$
- (1) $T_{amb} = -40\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = 100\text{ °C}$

Fig 14. TR2 (NPN): On-state input voltage as a function of collector current; typical values



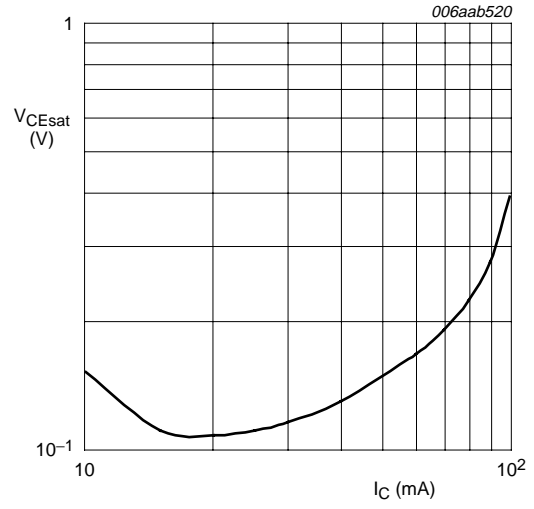
- $V_{CE} = 5\text{ V}$
- (1) $T_{amb} = -40\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = 100\text{ °C}$

Fig 15. TR2 (NPN): Off-state input voltage as a function of collector current; typical values



- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -40\text{ °C}$

Fig 16. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 50; T_{amb} = 25\text{ °C}$

Fig 17. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

8. Test information

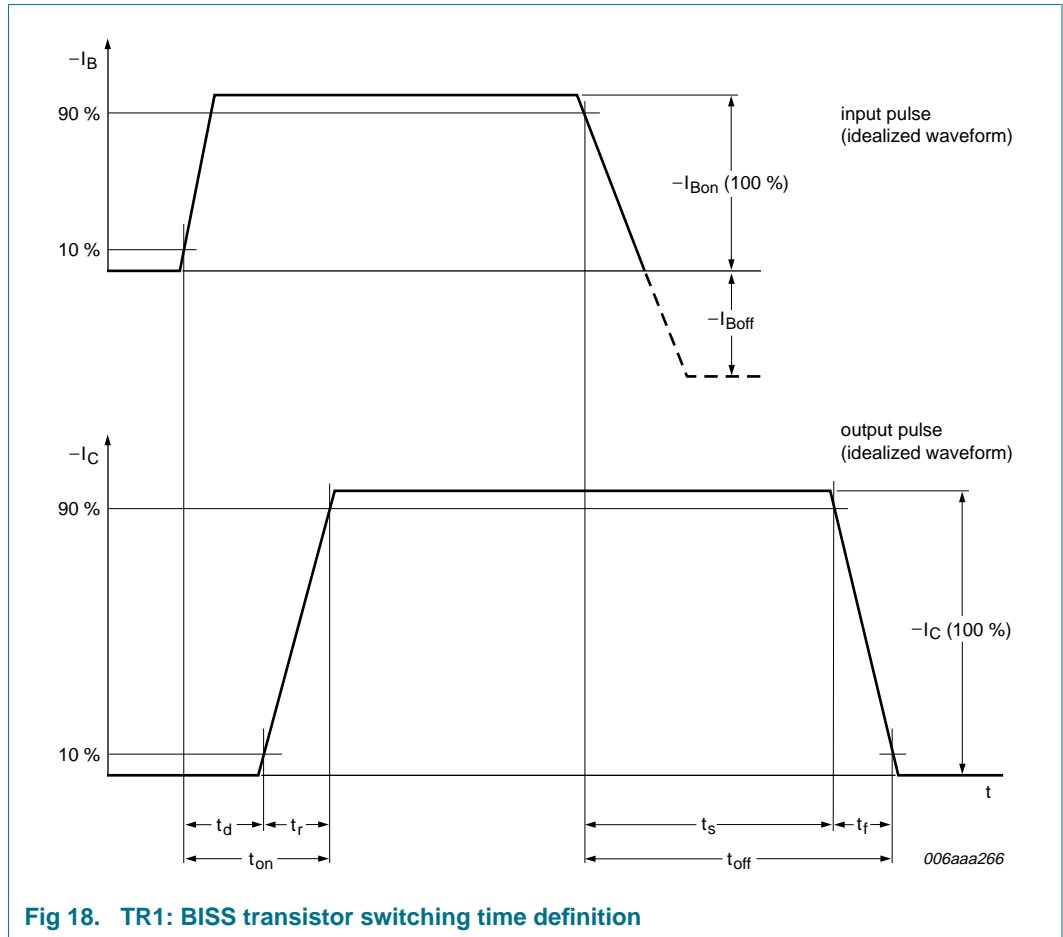


Fig 18. TR1: BISS transistor switching time definition

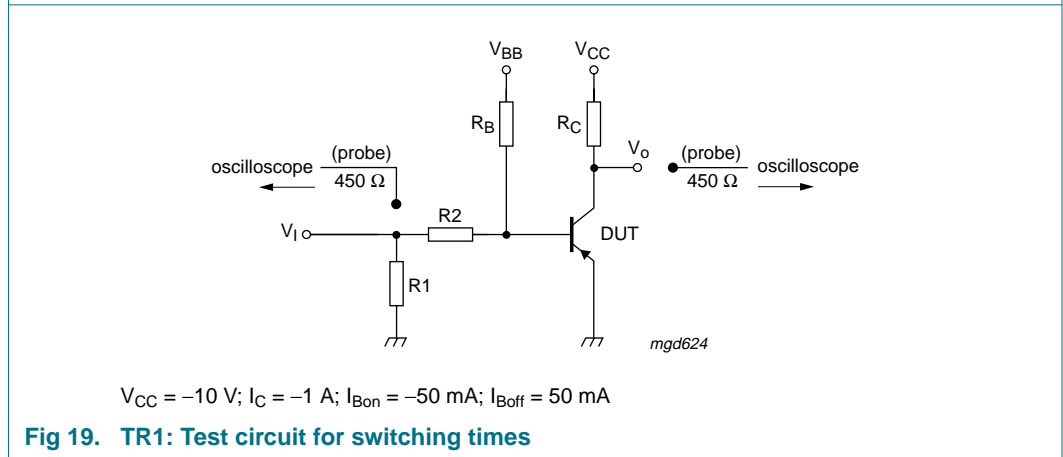
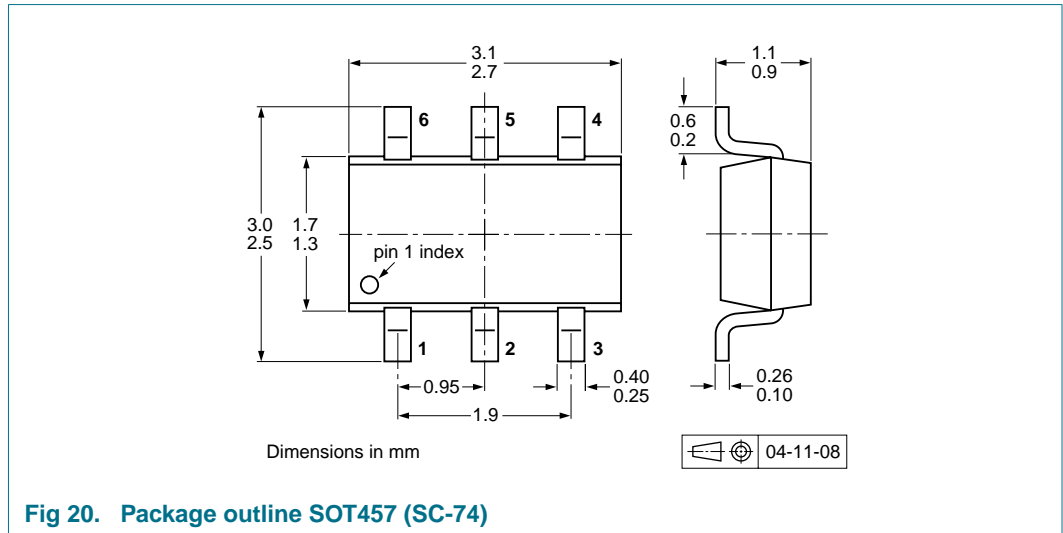


Fig 19. TR1: Test circuit for switching times

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PBLS6022D	SOT457	4 mm pitch, 8 mm tape and reel; T1	^[2] -115	-135
		4 mm pitch, 8 mm tape and reel; T2	^[3] -125	-165

[1] For further information and the availability of packing methods, see [Section 13](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBLS6022D_1	20090813	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

12.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

14. Contents

1 Product profile 1

1.1 General description 1

1.2 Features 1

1.3 Applications 1

1.4 Quick reference data 1

2 Pinning information 2

3 Ordering information 2

4 Marking 2

5 Limiting values 3

6 Thermal characteristics 4

7 Characteristics 6

8 Test information 12

8.1 Quality information 12

9 Package outline 13

10 Packing information 13

11 Revision history 14

12 Legal information 15

12.1 Data sheet status 15

12.2 Definitions 15

12.3 Disclaimers 15

12.4 Trademarks 15

13 Contact information 15

14 Contents 16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

