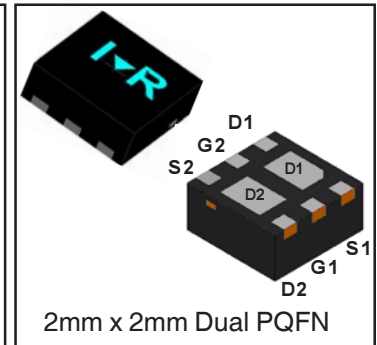
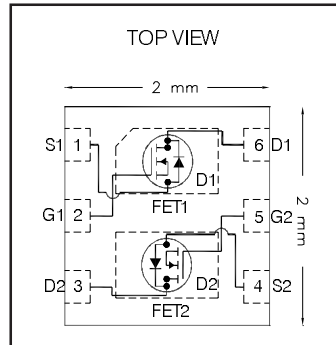


HEXFET® Power MOSFET

V_{DS}	20	V
V_{GS}	±12	V
$R_{DS(on) max}$ (@ $V_{GS} = 4.5V$)	45	mΩ
$R_{DS(on) max}$ (@ $V_{GS} = 2.5V$)	62	mΩ
I_D (@ $T_{c(Bottom)} = 25°C$)	3.4 Ⓣ	A



Applications

- Charge and discharge switch for battery application
- Load/System Switch

Features and Benefits

Features

Low $R_{DS(on)}$ ($\leq 45m\Omega$)	results in ⇒
Low Thermal Resistance to PCB ($\leq 19°C/W$)	
Low Profile ($\leq 1.0mm$)	
Industry-Standard Pinout	
Compatible with Existing Surface Mount Techniques	
RoHS Compliant Containing no Lead, no Bromide and no Halogen	

Resulting Benefits

Lower Conduction Losses
Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLHS6276TRPBF	PQFN Dual 2mm x 2mm	Tape and Reel	4000	
IRLHS6276TR2PBF	PQFN Dual 2mm x 2mm	Tape and Reel	400	EOL notice #259

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	±12	
$I_D @ T_A = 25°C$	Continuous Drain Current, $V_{GS} @ 4.5V$	4.5	A
$I_D @ T_A = 70°C$	Continuous Drain Current, $V_{GS} @ 4.5V$	3.6	
$I_D @ T_{c(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 4.5V$	9.6	
$I_D @ T_{c(Bottom)} = 100°C$	Continuous Drain Current, $V_{GS} @ 4.5V$	6.1	
$I_D @ T_{c(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 4.5V$ (Package Limited)	3.4	
I_{DM}	Pulsed Drain Current ①	40	
$P_D @ T_A = 25°C$	Power Dissipation ④	1.5	W
$P_D @ T_{c(Bottom)} = 25°C$	Power Dissipation ④	6.6	
	Linear Derating Factor ④	0.012	W/°C
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

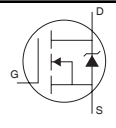
Notes ① through ④ are on page 2

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
B _V DSS	Drain-to-Source Breakdown Voltage	20	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔB _V DSS/ΔT _J	Breakdown Voltage Temp. Coefficient	—	9.3	—	mV/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	33	45	mΩ	V _{GS} = 4.5V, I _D = 3.4A ③②
		—	46	62		V _{GS} = 2.5V, I _D = 3.4A ③②
V _{GS(th)}	Gate Threshold Voltage	0.5	0.8	1.1	V	V _{DS} = V _{GS} , I _D = 10μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-3.8	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 16V, V _{GS} = 0V
		—	—	150		V _{DS} = 16V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 12V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -12V
g _{fs}	Forward Transconductance	8.8	—	—	S	V _{DS} = 10V, I _D = 3.4A②
Q _g	Total Gate Charge ⑥	—	3.1	—	nC	V _{DS} = 10V
Q _{gs}	Gate-to-Source Charge ⑥	—	0.22	—		V _{GS} = 4.5V
Q _{gd}	Gate-to-Drain Charge ⑥	—	1.3	—		I _D = 3.4A② (See Fig.17 & 18)
R _G	Gate Resistance	—	4.0	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	4.4	—	ns	V _{DD} = 10V, V _{GS} = 4.5V
t _r	Rise Time	—	9.3	—		ID = 3.4A②
t _{d(off)}	Turn-Off Delay Time	—	10	—		R _G = 1.8Ω
t _f	Fall Time	—	4.9	—		See Fig.15
C _{iss}	Input Capacitance	—	310	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	79	—		V _{DS} = 10V
C _{rss}	Reverse Transfer Capacitance	—	49	—		f = 1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	9.6②	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	40		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 3.4A②, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	5.2	7.8	ns	T _J = 25°C, I _F = 3.4A②, V _{DD} = 10V
Q _{rr}	Reverse Recovery Charge	—	5.0	7.5	nC	di/dt = 126A/μs ③
t _{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				


Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ⑤	—	19	°C/W
R _{θJC} (Top)	Junction-to-Case ⑤	—	175	
R _{θJA}	Junction-to-Ambient ④	—	86	
R _{θJA} (<10s)	Junction-to-Ambient ④	—	69	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Current limited by package.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ When mounted on 1 inch square copper board.
- ⑤ R_θ is measured at T_J of approximately 90°C.
- ⑥ For DESIGN AID ONLY, not subject to production testing.

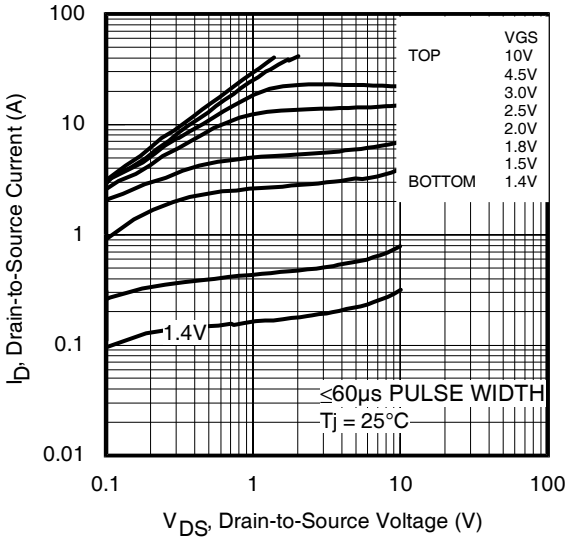


Fig 1. Typical Output Characteristics

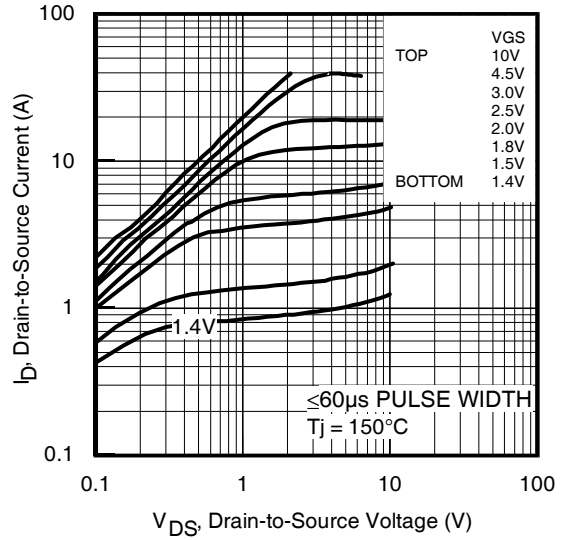


Fig 2. Typical Output Characteristics

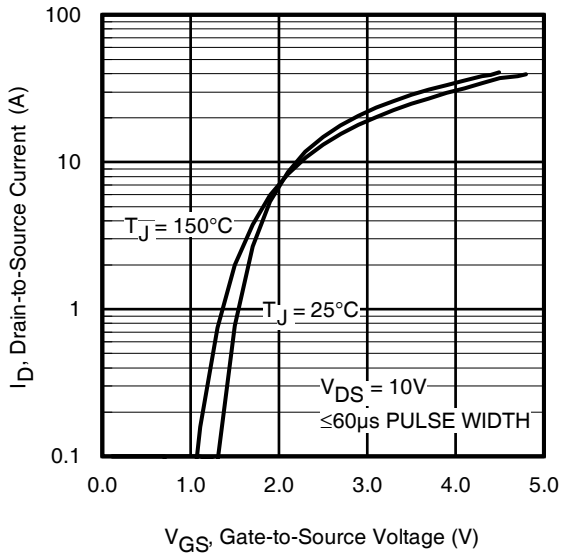


Fig 3. Typical Transfer Characteristics

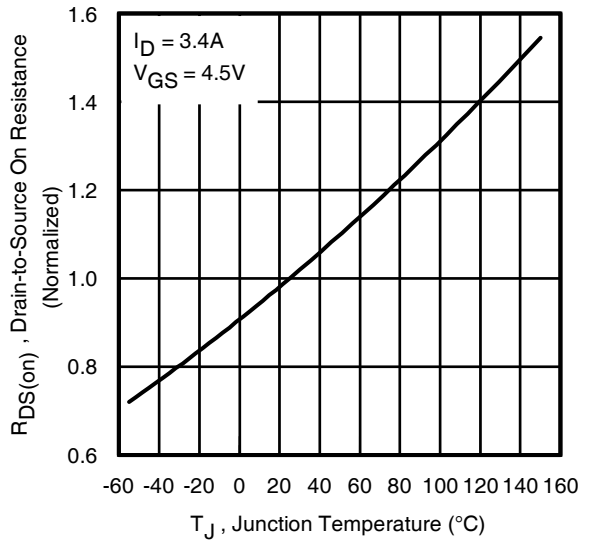


Fig 4. Normalized On-Resistance vs. Temperature

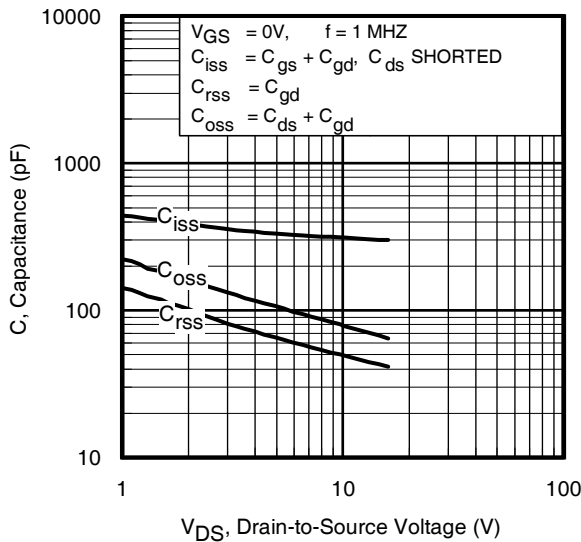


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

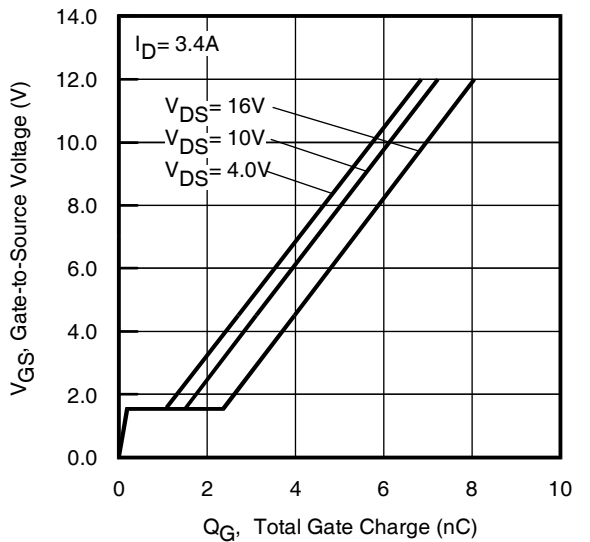


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

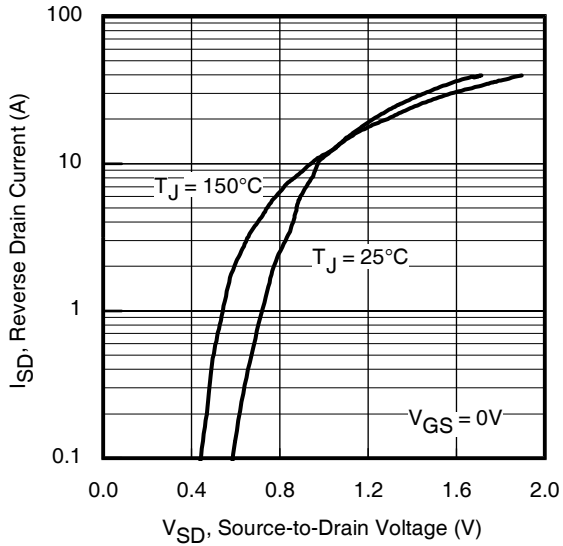


Fig 7. Typical Source-Drain Diode Forward Voltage

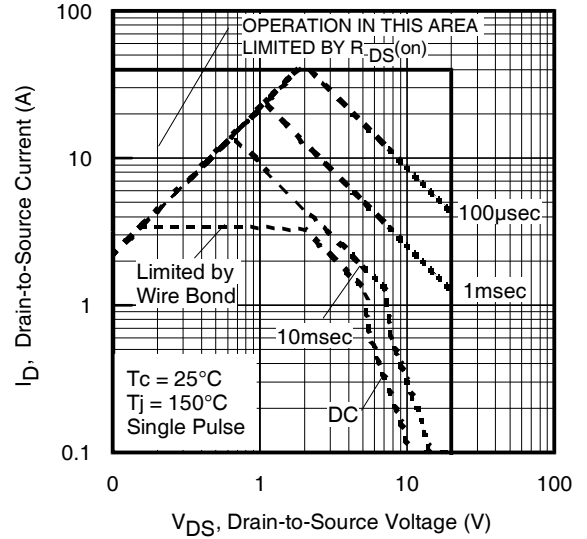


Fig 8. Maximum Safe Operating Area

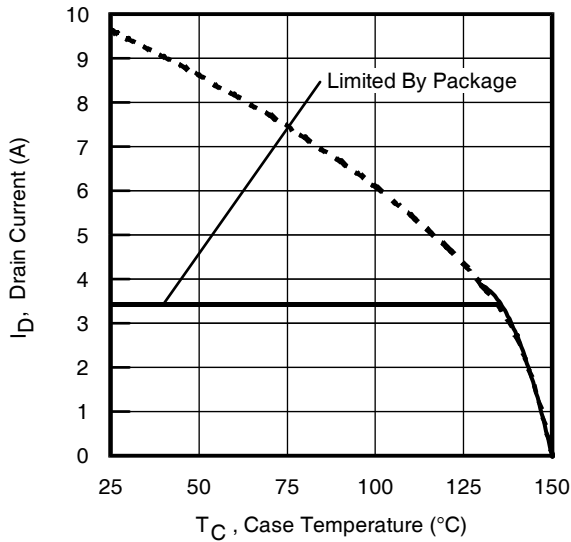


Fig 9. Maximum Drain Current vs. Case (Bottom) Temperature

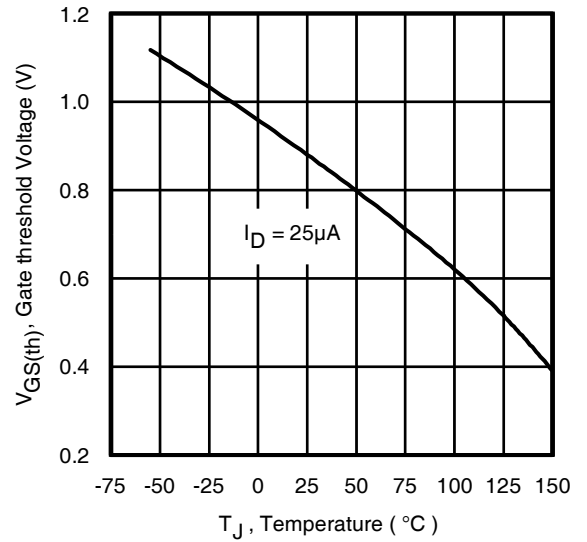


Fig 10. Threshold Voltage vs. Temperature

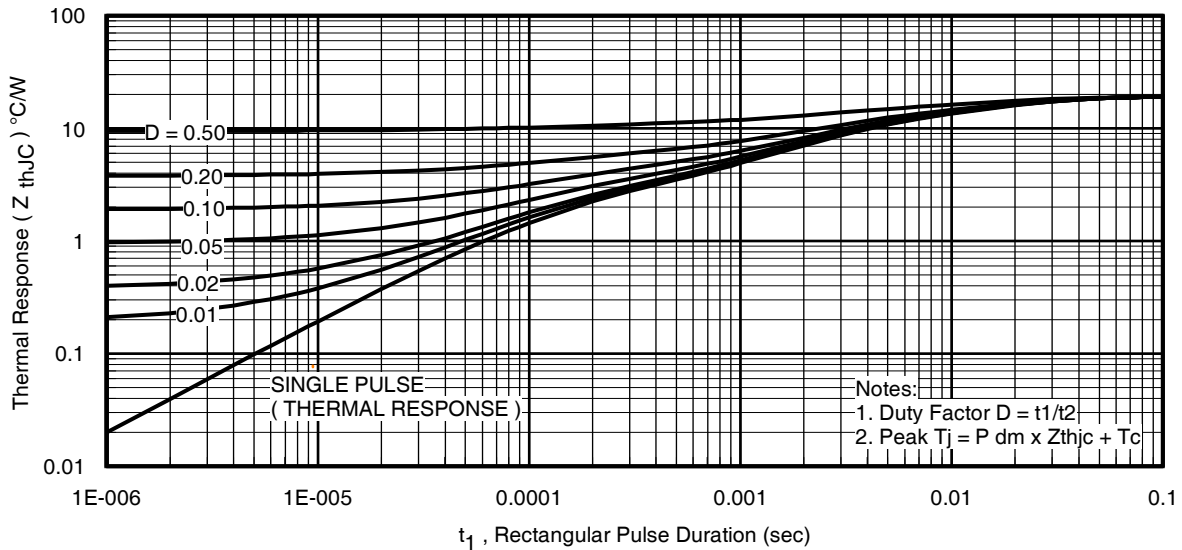


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

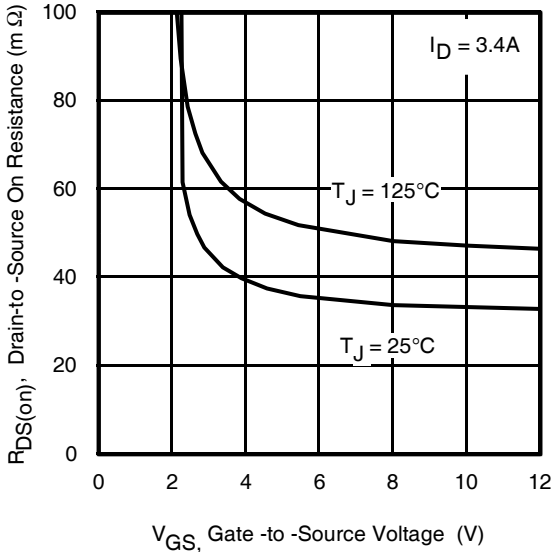


Fig 12. On-Resistance vs. Gate Voltage

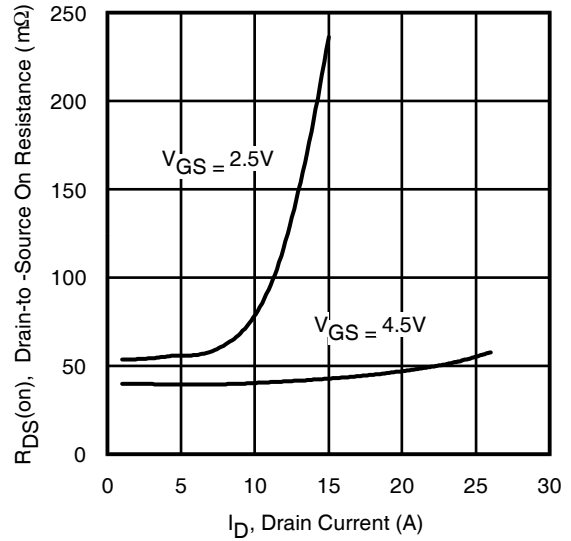


Fig 13. Typical On-Resistance vs. Drain Current

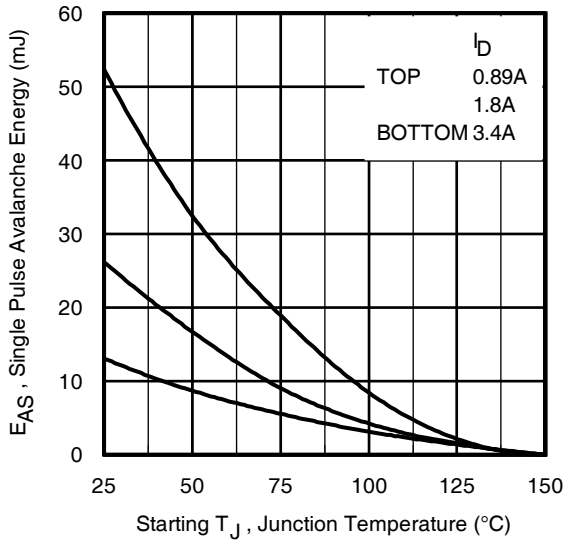


Fig 14. Maximum Avalanche Energy vs. Drain Current

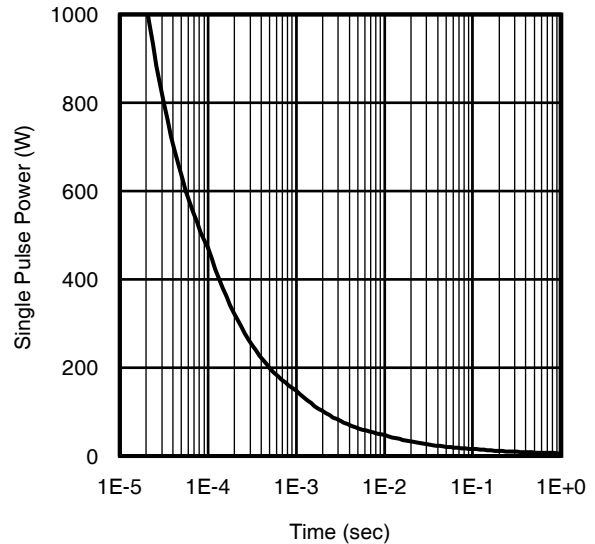
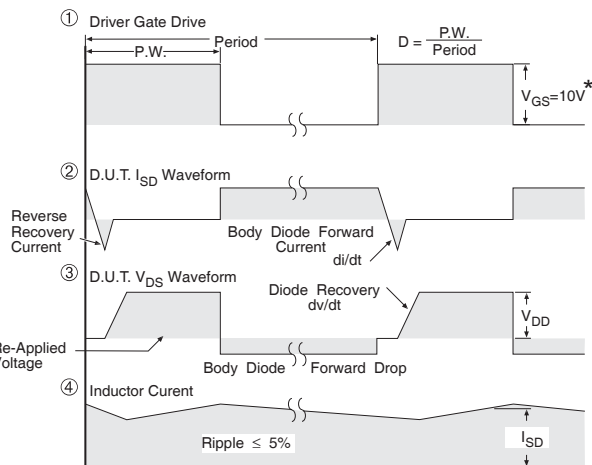
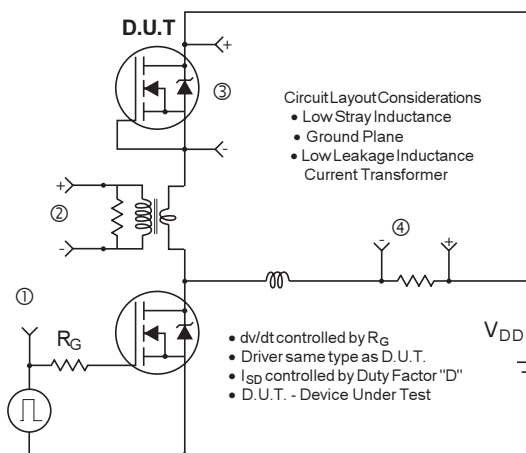


Fig 15. Typical Power vs. Time



* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

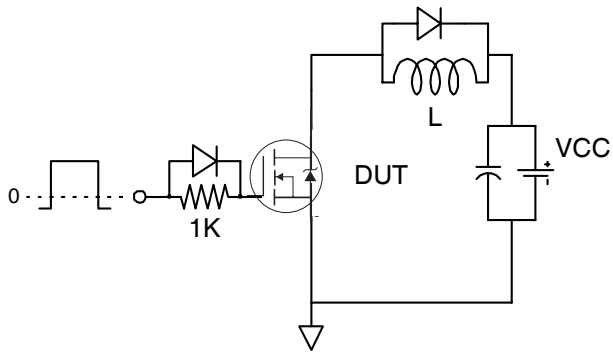


Fig 17a. Gate Charge Test Circuit

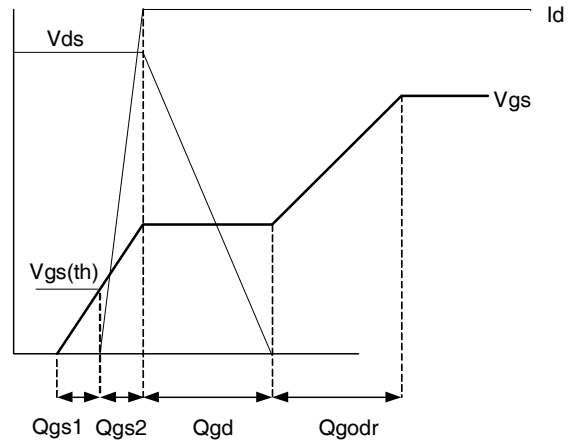


Fig 17b. Gate Charge Waveform

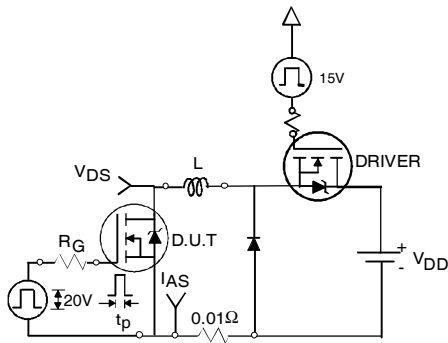


Fig 18a. Unclamped Inductive Test Circuit

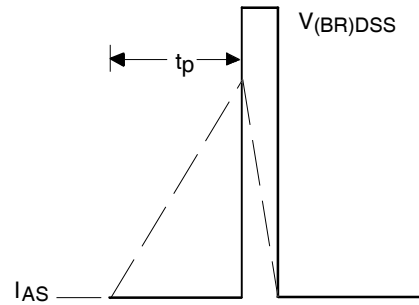


Fig 18b. Unclamped Inductive Waveforms

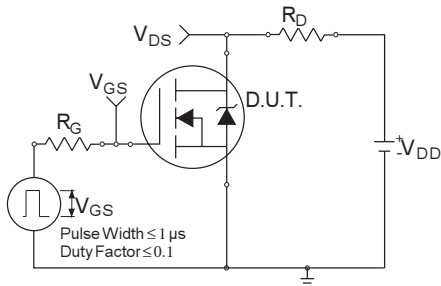


Fig 19a. Switching Time Test Circuit

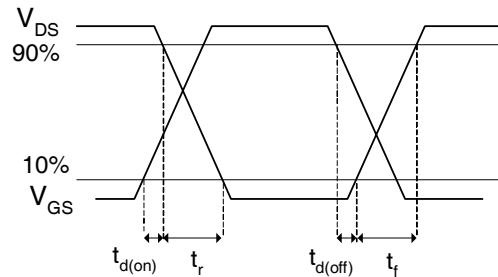
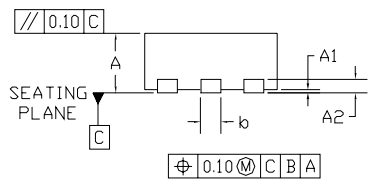
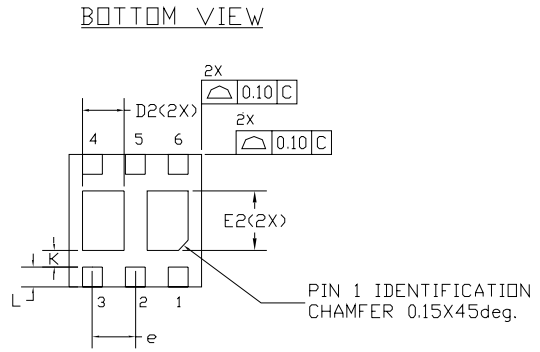
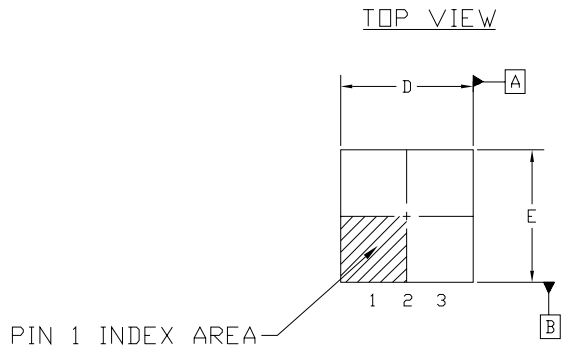


Fig 19b. Switching Time Waveforms

PQFN Dual 2x2 Outline Package Details



SIDE VIEW

NOTES :

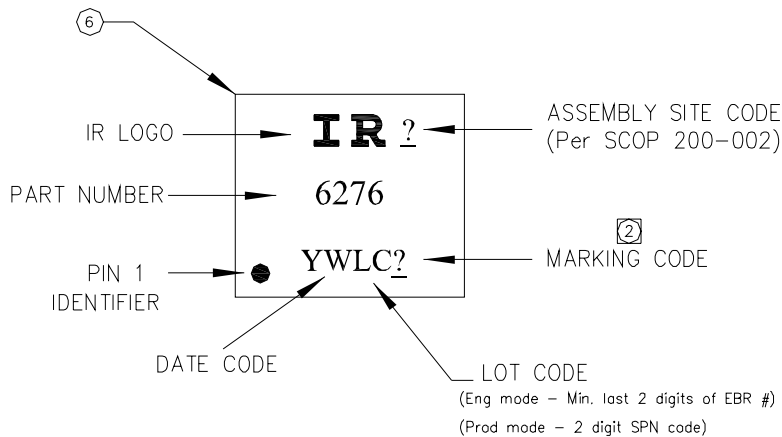
- 1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.

SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.036	0.040
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.203 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	0.575	0.625	0.675	0.023	0.025	0.027
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	0.85	0.90	0.95	0.034	0.036	0.038
e	0.65 BSC			0.026 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
K	0.25	-	-	0.010	-	-

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>
 For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN Dual 2x2 Outline Part Marking

TOP MARKING (LASER)



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

PQFN Dual 2x2 Outline Tape and Reel

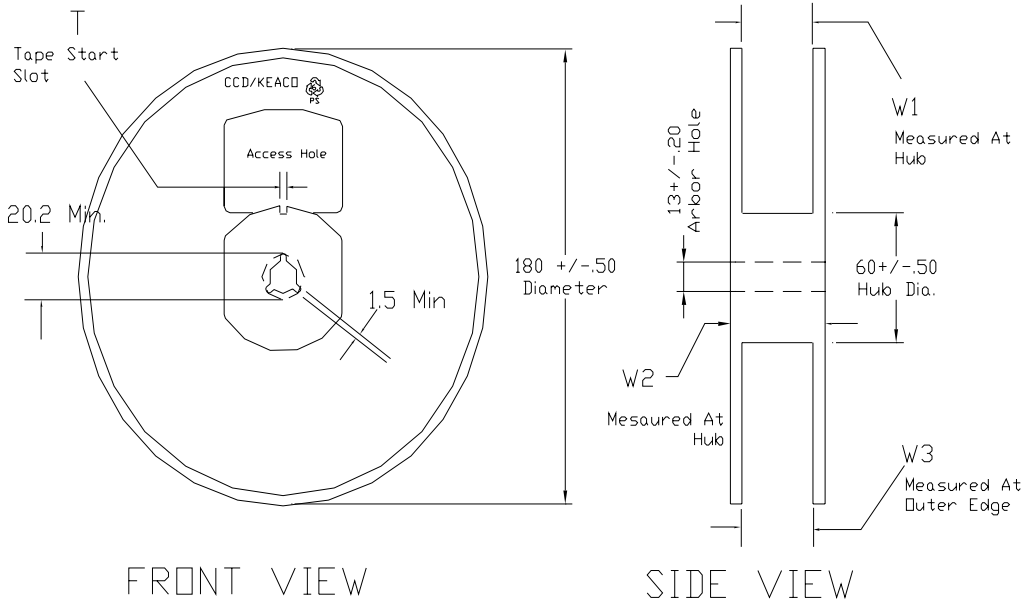
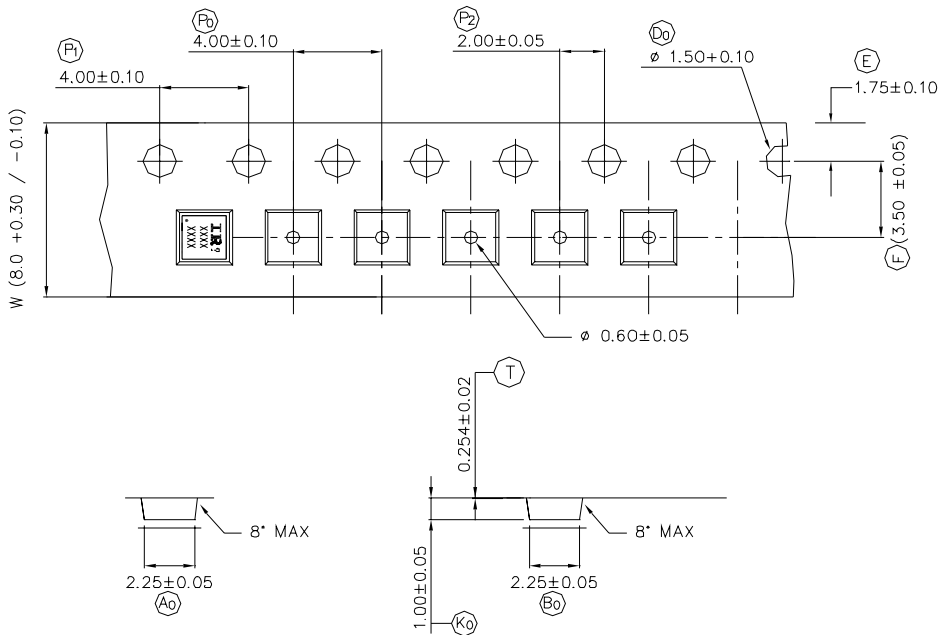


TABLE 1: REEL DETAILS

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 ^{+1.5} _{0.0}	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	12.4 ^{+2.0} _{-0.0}	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is $\geq 1 \times 10^5$ but $< 1 \times 10^{12}$ ohm/sq.



NOTE: The Surface Resistivity is $10^4 - 10^8$ OHM/SQ

Qualification information[†]

Qualification level	Industrial (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	PQFN Dual 2mm x 2mm	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site
<http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
1/9/2014	<ul style="list-style-type: none"> • Updated ordering information to reflect the End-Of-Life (EOL) of the mini-reel option (EOL notice #259). • Updated data sheet with the new IR corporate template. • Updated the qualification level from Consumer to Industrial level.

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