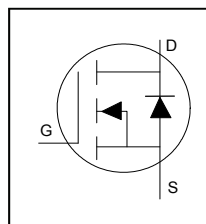


Application

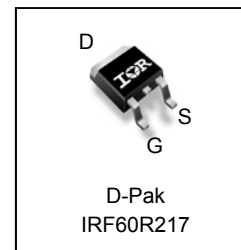
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



V_{DSS}	60V
R_{DS(on)} typ.	8.0mΩ
	max
I_D	58A



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF60R217	D-Pak	Tape and Reel	2000	IRF60R217

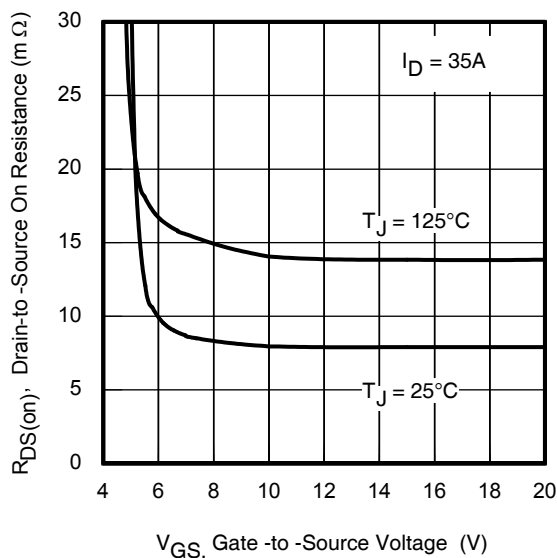


Fig 1. Typical On-Resistance vs. Gate Voltage

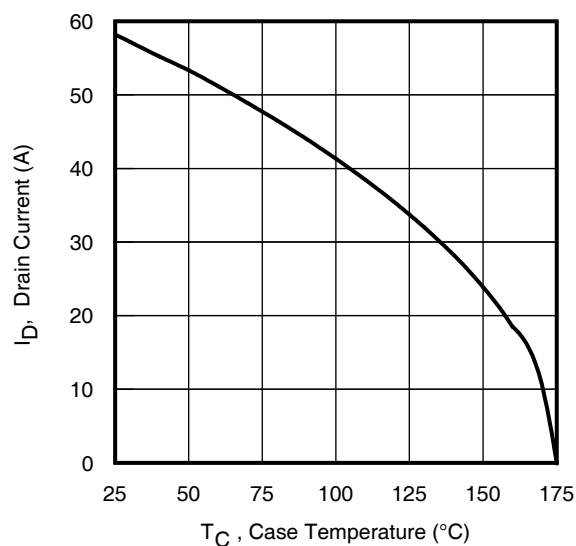


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	58	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	41	
I_{DM}	Pulsed Drain Current ①	217	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	83	W
	Linear Derating Factor	0.56	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	85	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ⑨	124	
I_{AR}	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	1.8	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.047	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	8.0	9.9	mΩ	$V_{GS} = 10\text{V}, I_D = 35\text{A}$
		—	10	—		$V_{GS} = 6.0\text{V}, I_D = 18\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}, I_D = 50\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Gate Resistance	—	2.0	—	Ω	

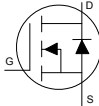
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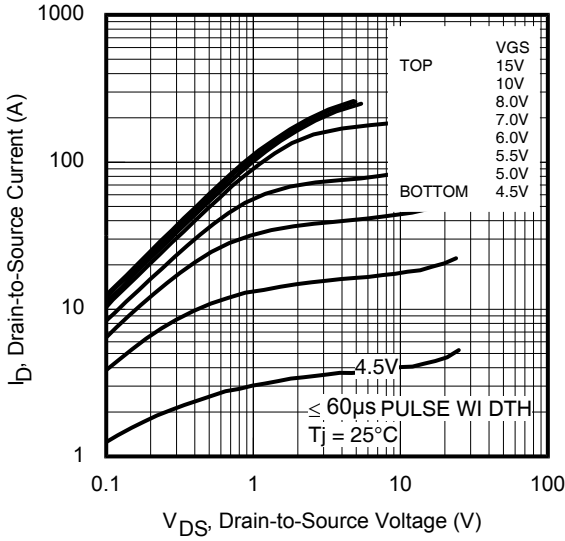
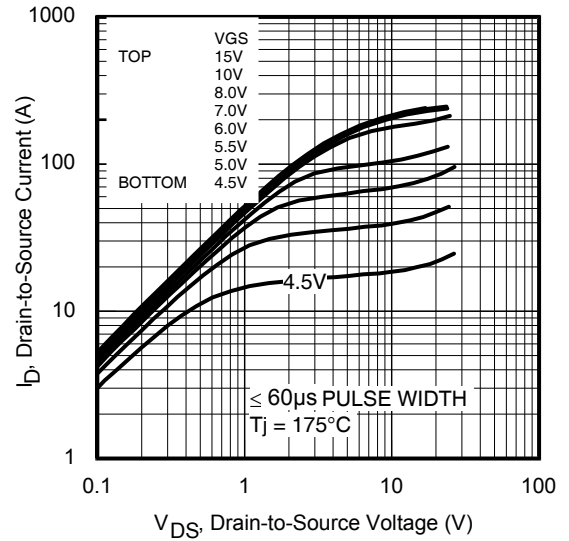
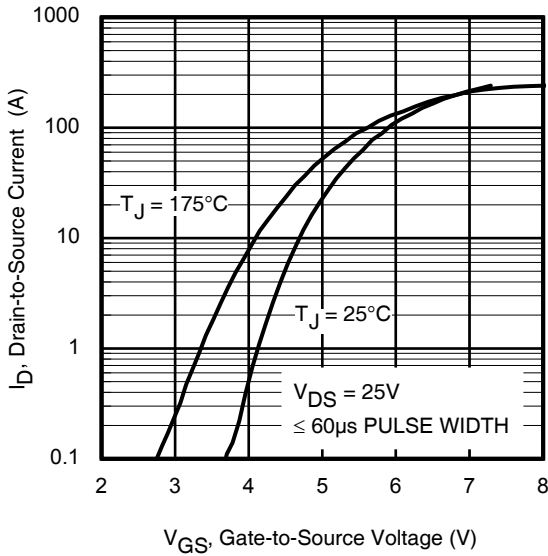
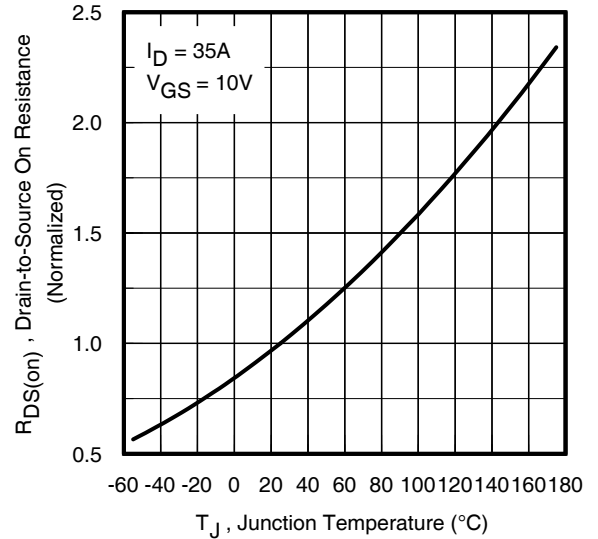
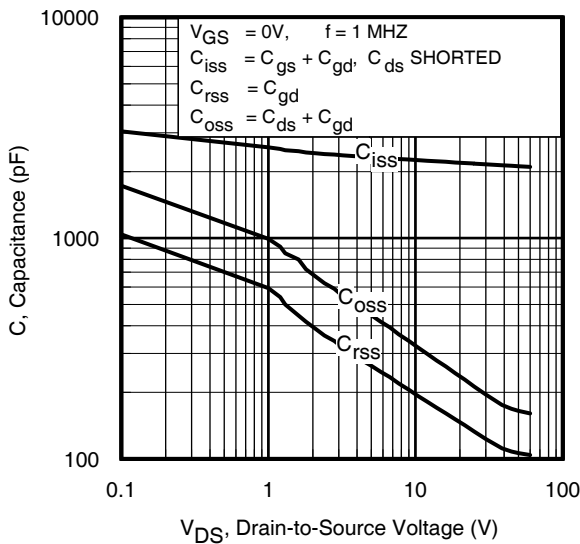
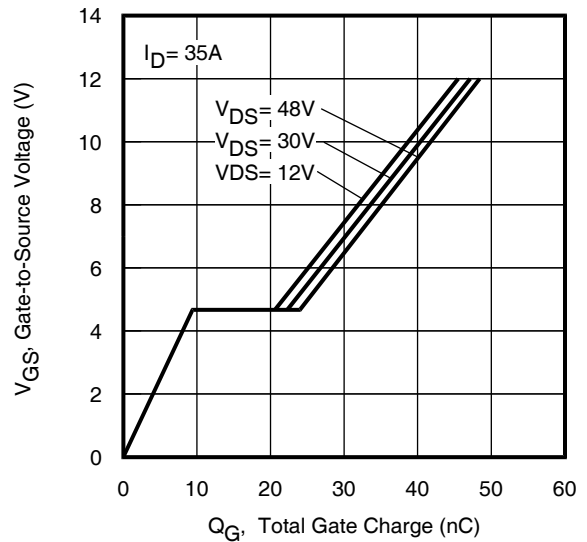
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.14\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 35\text{A}$, $V_{GS} = 10\text{V}$.
- ③ $I_{SD} \leq 35\text{A}$, $di/dt \leq 862\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ R_θ is measured at T_J approximately 90°C .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994. please refer to application note to AN-994: <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑨ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 16\text{A}$, $V_{GS} = 10\text{V}$.

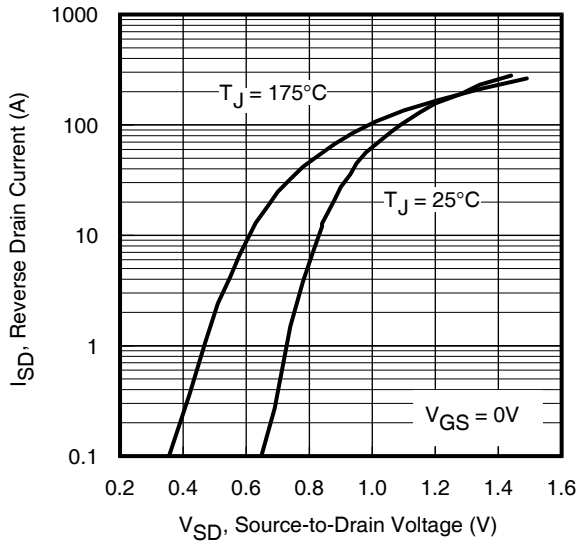
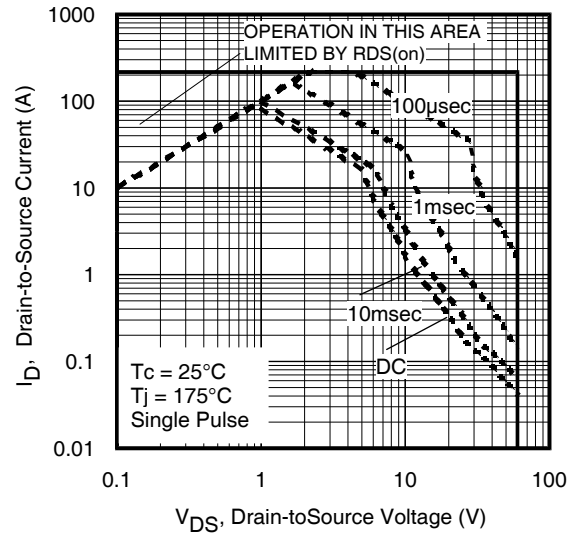
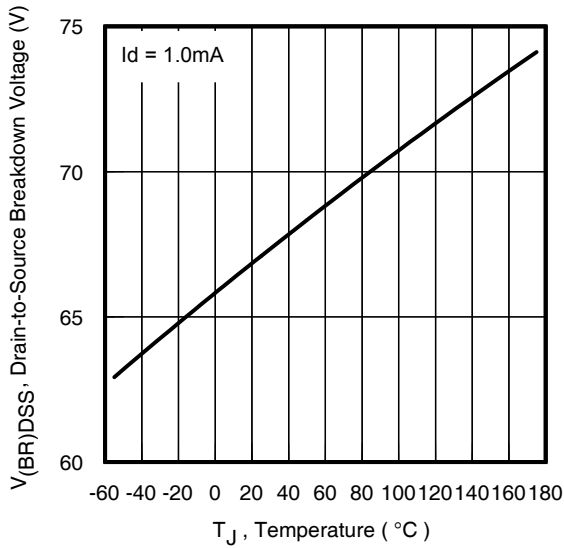
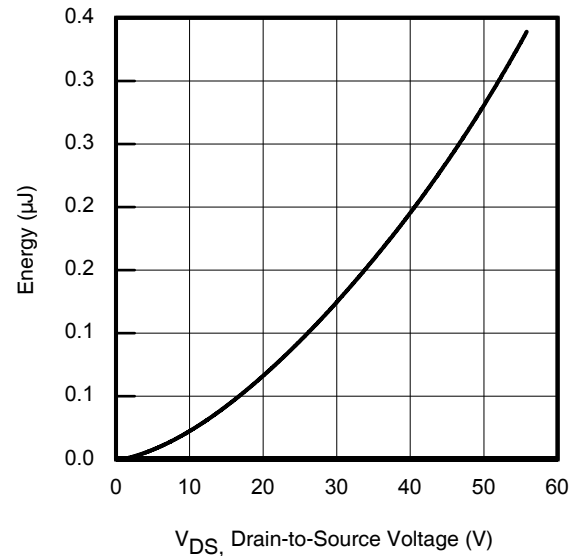
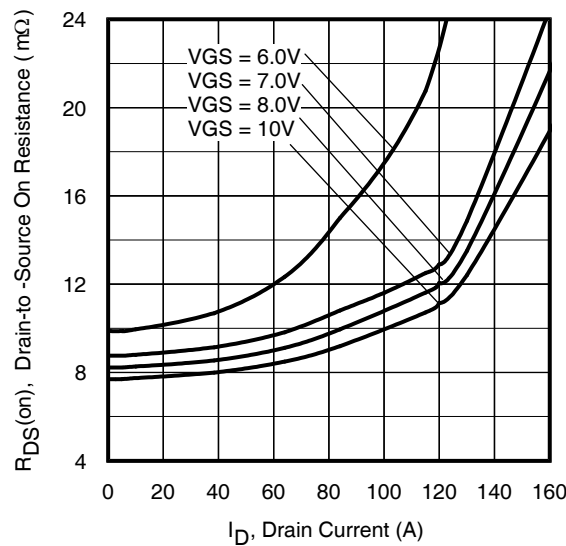
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

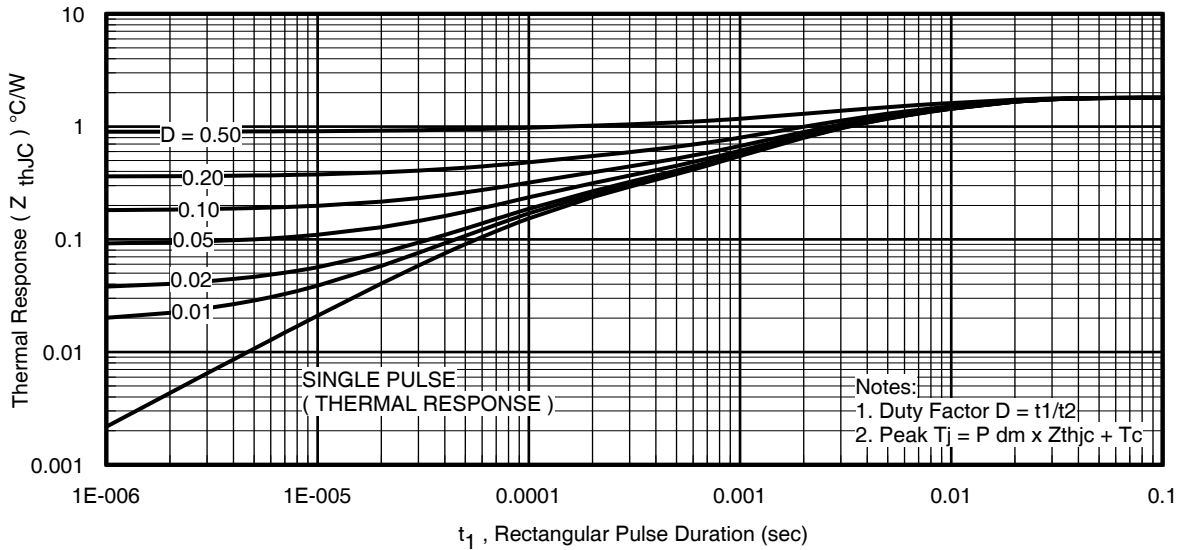
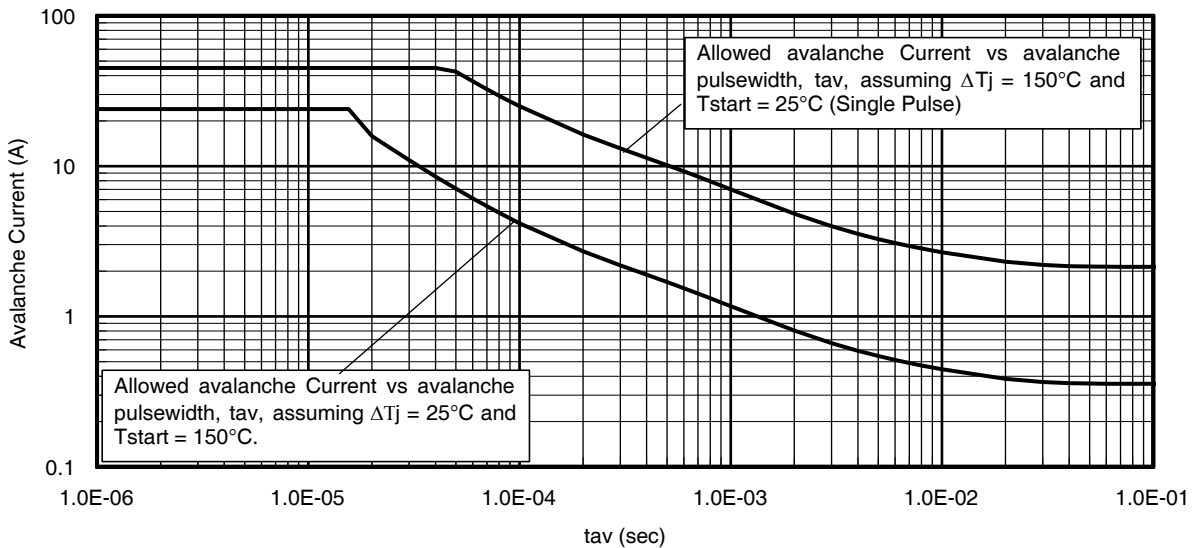
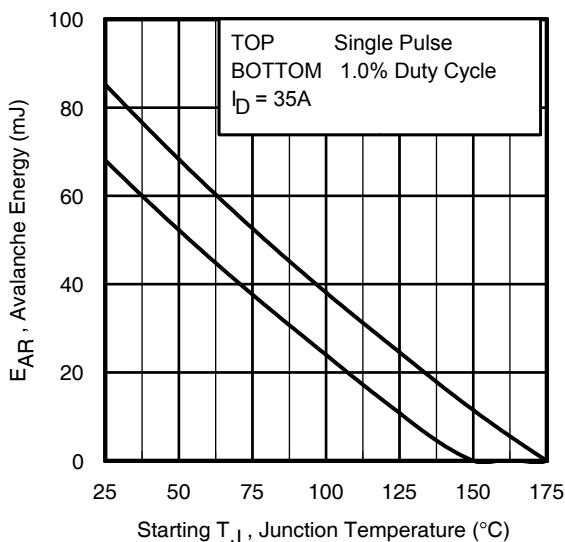
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	120	—	—	S	$V_{DS} = 10\text{V}, I_D = 35\text{A}$
Q_g	Total Gate Charge	—	40	66	nC	$I_D = 35\text{A}$ $V_{DS} = 30\text{V}$ $V_{GS} = 10\text{V}$
Q_{gs}	Gate-to-Source Charge	—	10	—		
Q_{gd}	Gate-to-Drain Charge	—	12	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	28	—		
$t_{d(on)}$	Turn-On Delay Time	—	7.6	—	ns	$V_{DD} = 30\text{V}$ $I_D = 35\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ④
t_r	Rise Time	—	29	—		
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		
t_f	Fall Time	—	12	—		
C_{iss}	Input Capacitance	—	2170	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$, See Fig. 7
C_{oss}	Output Capacitance	—	210	—		
C_{riss}	Reverse Transfer Capacitance	—	130	—		
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	228	—		
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	—	283	—		

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	58	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	217		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 35\text{A}, V_{GS} = 0\text{V}$ ④
dv/dt	Peak Diode Recovery dv/dt ③	—	18	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 35\text{A}, V_{DS} = 60\text{V}$
t_{rr}	Reverse Recovery Time	—	27	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 51\text{V}$
		—	30	—		$T_J = 125^\circ\text{C}$ $I_F = 35\text{A}$,
Q_{rr}	Reverse Recovery Charge	—	26	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ④
		—	33	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	1.7	—	A	$T_J = 25^\circ\text{C}$

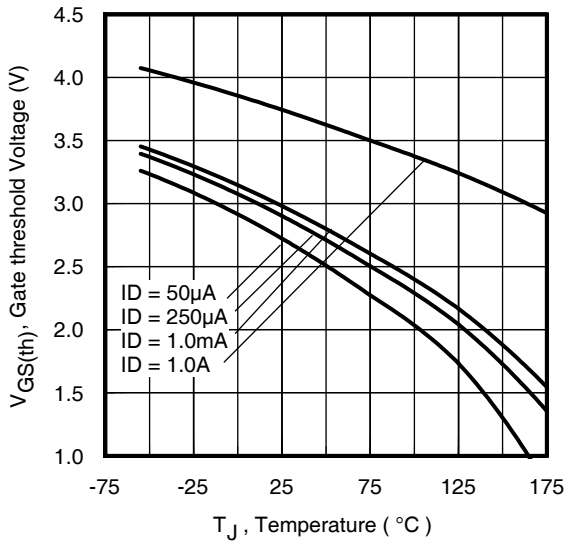
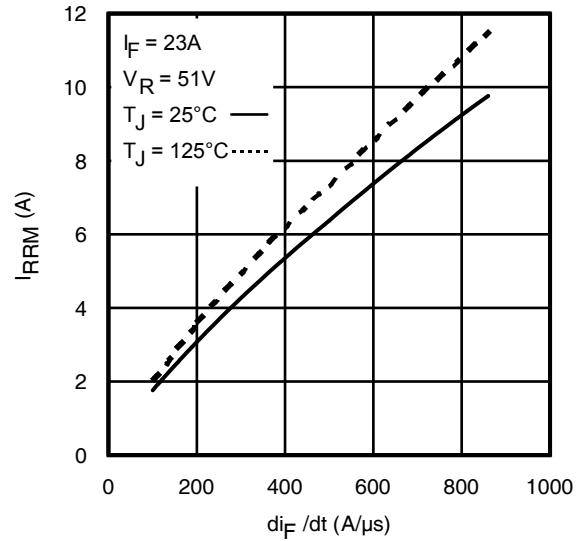
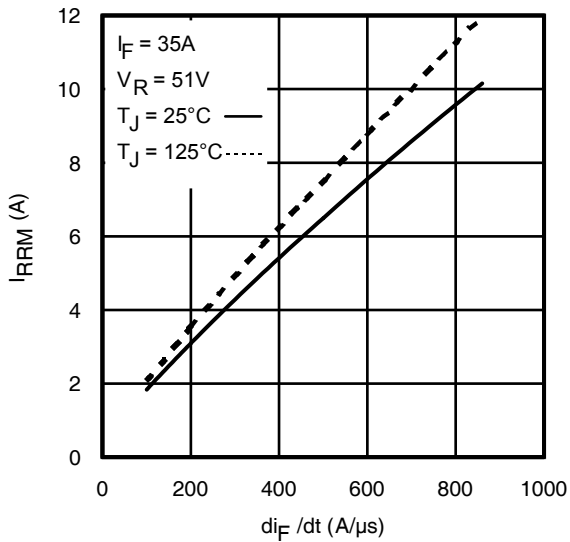
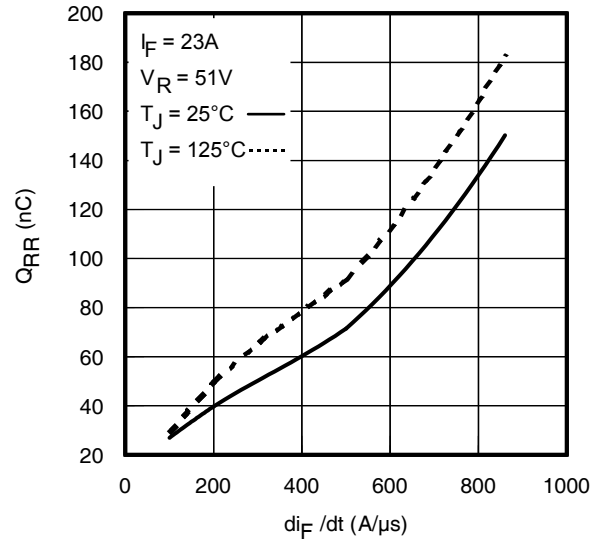
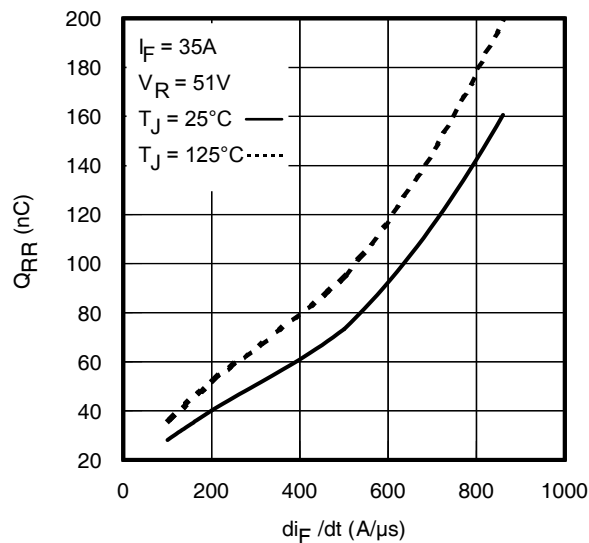

Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Normalized On-Resistance vs. Temperature

Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Gate Charge vs. Drain-to-Source Voltage

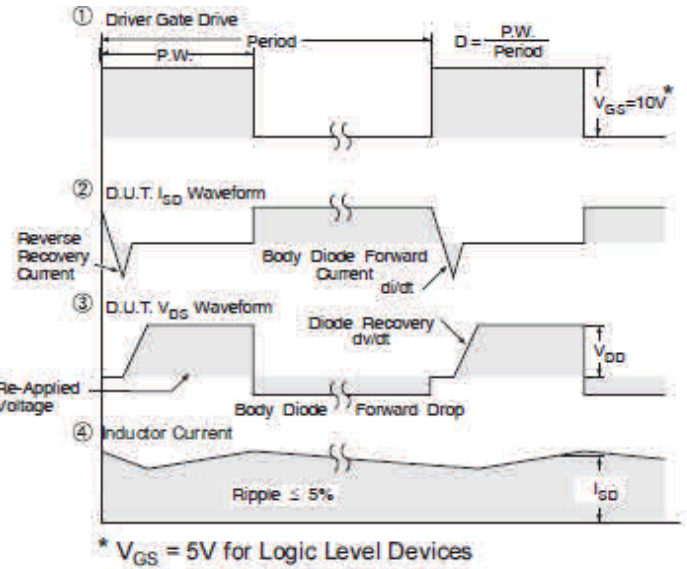
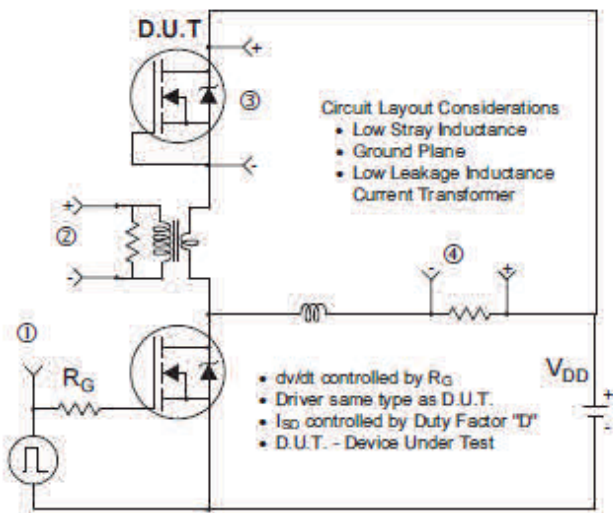
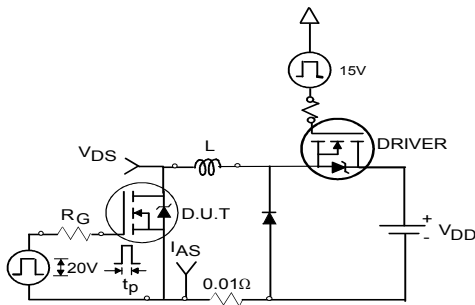
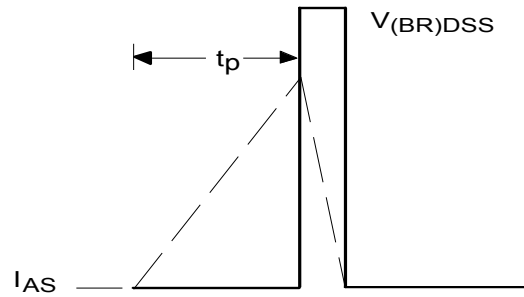
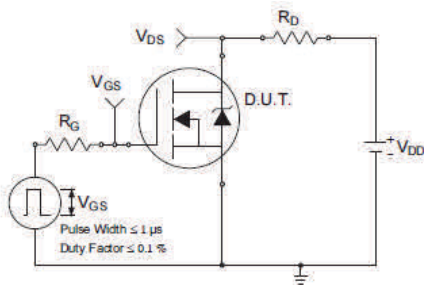
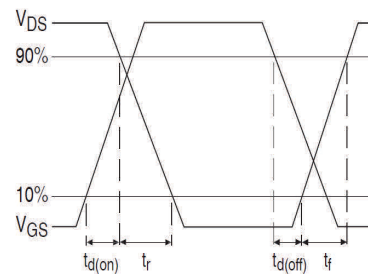
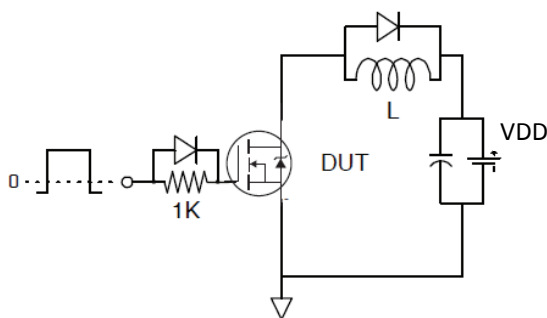
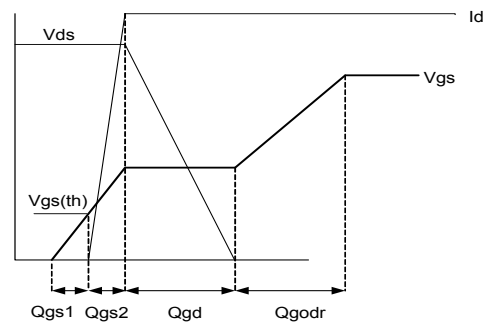

Fig 9. Typical Source-Drain Diode Forward Voltage

Fig 10. Maximum Safe Operating Area

Fig 11. Drain-to-Source Breakdown Voltage

Fig 12. Typical C_{oss} Stored Energy

Fig 13. Typical On-Resistance vs. Drain Current

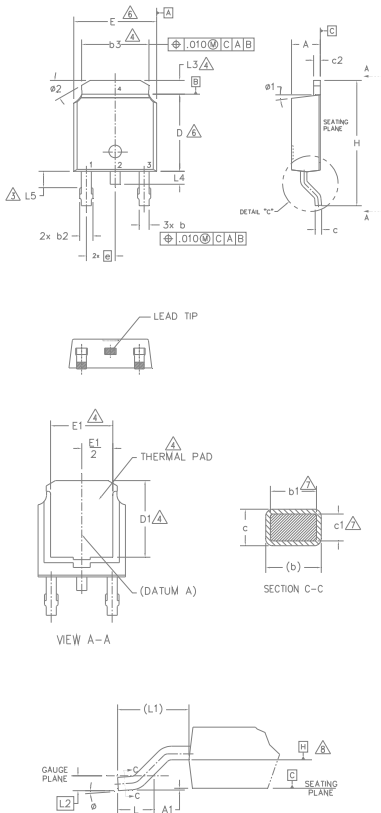

Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 15. Avalanche Current vs. Pulse Width

Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figures 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figure 14)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


Fig 17. Threshold Voltage vs. Temperature

Fig 18. Typical Recovery Current vs. dif/dt

Fig 19. Typical Recovery Current vs. dif/dt

Fig 20. Typical Stored Charge vs. dif/dt

Fig 21. Typical Stored Charge vs. dif/dt


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 23a. Unclamped Inductive Test Circuit

Fig 23b. Unclamped Inductive Waveforms

Fig 24a. Switching Time Test Circuit

Fig 24b. Switching Time Waveforms

Fig 25a. Gate Charge Test Circuit

Fig 25b. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline Dimensions are shown in millimeters (inches)

NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
- △ LEAD DIMENSION UNCONTROLLED IN L5.
- △△ DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- △△ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- △△ DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- △△ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
phi	0"	10"	0"	10"	
phi1	0"	15"	0"	15"	
phi2	25"	35"	25"	35"	

LEAD ASSIGNMENTS
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

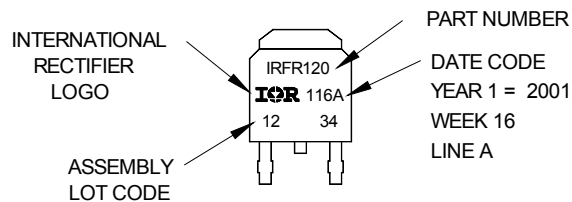
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

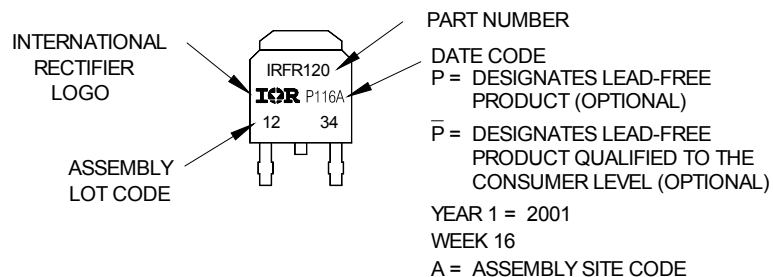
Note: "P" in assembly line position
indicates "Lead-Free"

"P" in assembly line position indicates
"Lead-Free" qualification to the consumer-level



PART NUMBER
DATE CODE
YEAR 1 = 2001
WEEK 16
LINE A

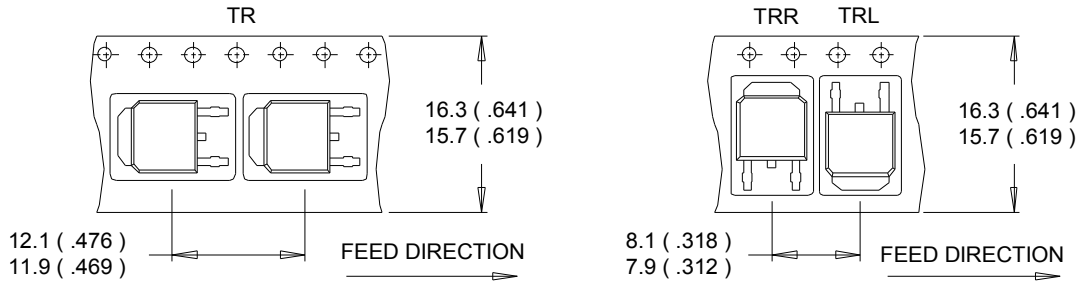
OR



PART NUMBER
DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
P̄ = DESIGNATES LEAD-FREE
PRODUCT QUALIFIED TO THE
CONSUMER LEVEL (OPTIONAL)
YEAR 1 = 2001
WEEK 16
A = ASSEMBLY SITE CODE

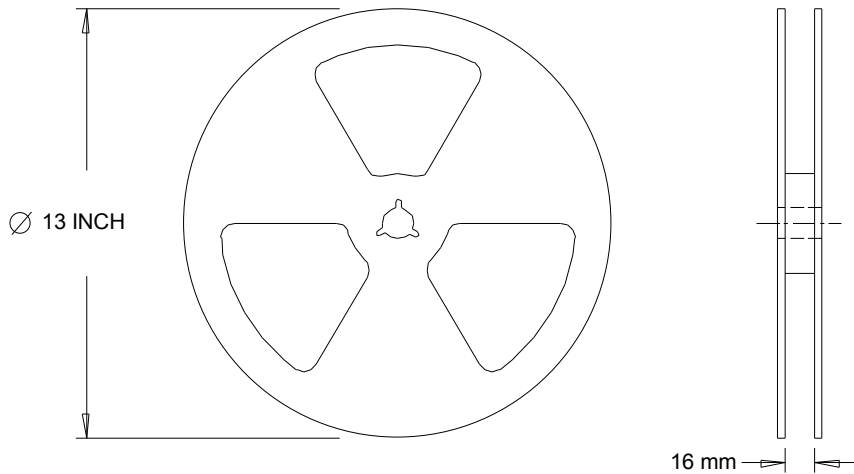
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D-Pak (TO-252AA) Tape & Reel Information Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	D-Pak	MSL1
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

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