

## MOSFET

### 500V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} \cdot Q_g$  and  $E_{oss}$
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

### Applications

Adapter, Charger and Lighting

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	550	V
$R_{DS(on),max}$	0.65	$\Omega$
$I_D$	9	A
$Q_{g,typ}$	15	nC
$I_{D,pulse}$	19	A
$E_{oss} @ 400V$	1.69	$\mu J$

Type / Ordering Code	Package	Marking	Related Links
IPN50R650CE	PG-SOT223	50S650	see Appendix A

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**1 Maximum ratings**  
 at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	9 5.7	A	$T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	19	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	102	mJ	$I_D = 2.3\text{A}$ ; $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	$E_{AR}$	-	-	0.15	mJ	$I_D = 2.3\text{A}$ ; $V_{DD} = 50\text{V}$
Avalanche current, repetitive	$I_{AR}$	-	-	2.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	$V_{GS}$	-20 -30	-	20 30	V	static; AC ( $f > 1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	5.0	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	1.8	A	$T_C = 25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	19.0	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j = 25^\circ\text{C}$ , $t_{cond} < 2\mu\text{s}$
Maximum diode commutation speed <sup>3)</sup>	di <sub>r</sub> /dt	-	-	500	A/ $\mu\text{s}$	$V_{DS} = 0 \dots 400\text{V}$ , $I_{SD} \leq I_S$ , $T_j = 25^\circ\text{C}$ , $t_{cond} < 2\mu\text{s}$

**2 Thermal characteristics**

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - solder point	$R_{thJS}$	-	-	22.5	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient for minimal footprint	$R_{thJA}$	-	-	160	$^\circ\text{C/W}$	minimal footprint
Thermal resistance, junction - ambient soldered on copper area	$R_{thJA}$	-	-	75	$^\circ\text{C/W}$	Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm <sup>2</sup> (one layer 70 $\mu\text{m}$ thick) copper area for drain connection and cooling. PCB is vertical without blown air.
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	$^\circ\text{C}$	reflow MSL3

1) DPAK equivalent. Limited by  $T_{j,max}$ . Maximum duty cycle  $D=0.5$

2) Pulse width  $t_p$  limited by  $T_{j,max}$

3)  $V_{DClink}=400\text{V}$ ;  $V_{DS,peak} < V_{(BR)DSS}$ ; identical low side and high side switch with identical  $R_G$

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{GS(th)}$	2.50	3	3.50	V	$V_{DS}=V_{GS}, I_D=0.15mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=500V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=500V, V_{GS}=0V, T_j=150^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.59	0.65	$\Omega$	$V_{GS}=13V, I_D=1.8A, T_j=25^\circ C$ $V_{GS}=13V, I_D=1.8A, T_j=150^\circ C$
Gate resistance	$R_G$	-	3	-	$\Omega$	$f=1\text{ MHz, open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	342	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Output capacitance	$C_{oss}$	-	26	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1MHz$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	21	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	80	-	pF	$I_D=constant, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A,$ $R_G=5.3\Omega$
Rise time	$t_r$	-	5	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A,$ $R_G=5.3\Omega$
Turn-off delay time	$t_{d(off)}$	-	27	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A,$ $R_G=5.3\Omega$
Fall time	$t_f$	-	13	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=2.3A,$ $R_G=5.3\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	1.8	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate to drain charge	$Q_{gd}$	-	8.1	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate charge total	$Q_g$	-	15	-	nC	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	$V_{DD}=400V, I_D=2.3A, V_{GS}=0\text{ to }10V$

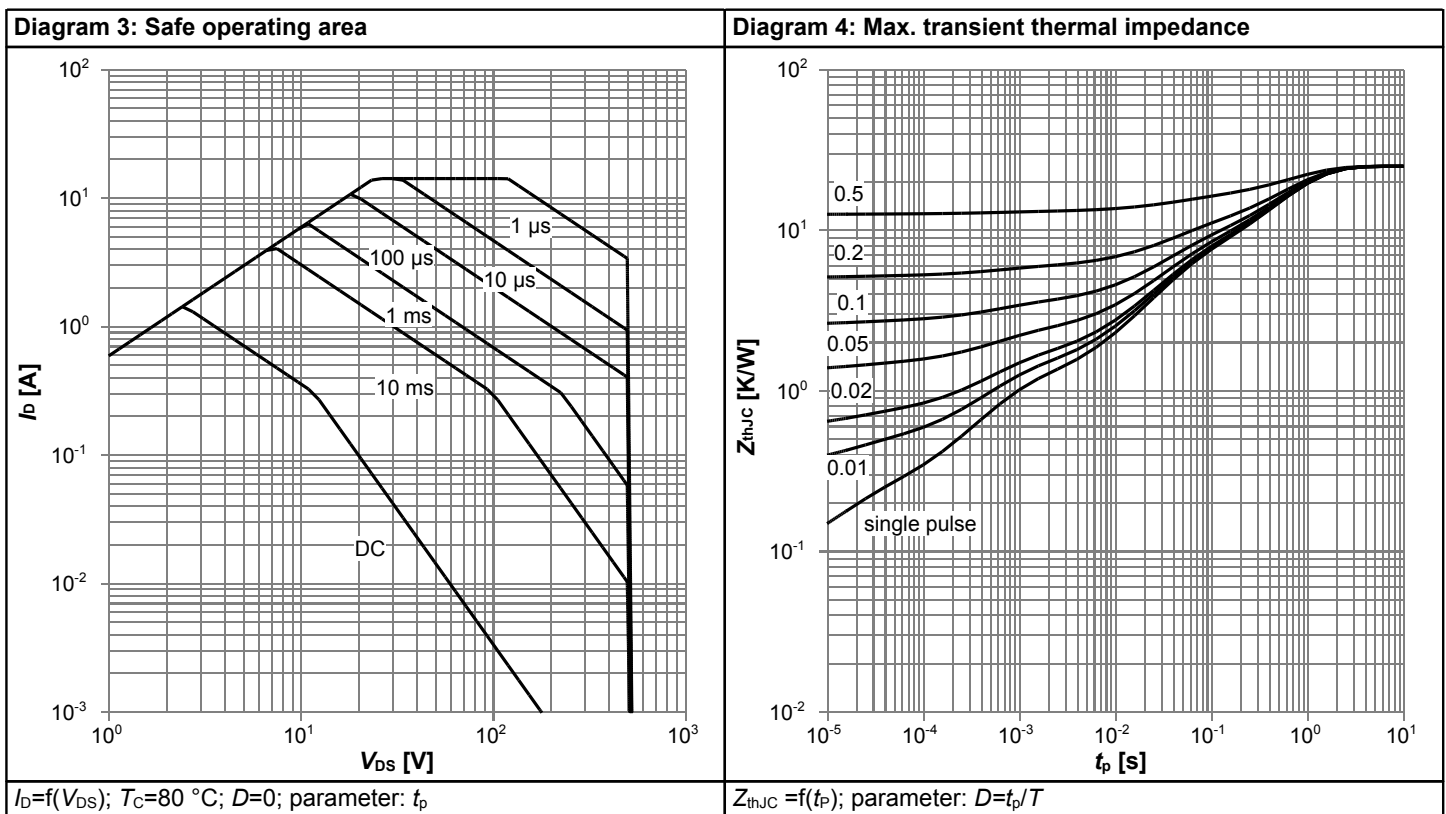
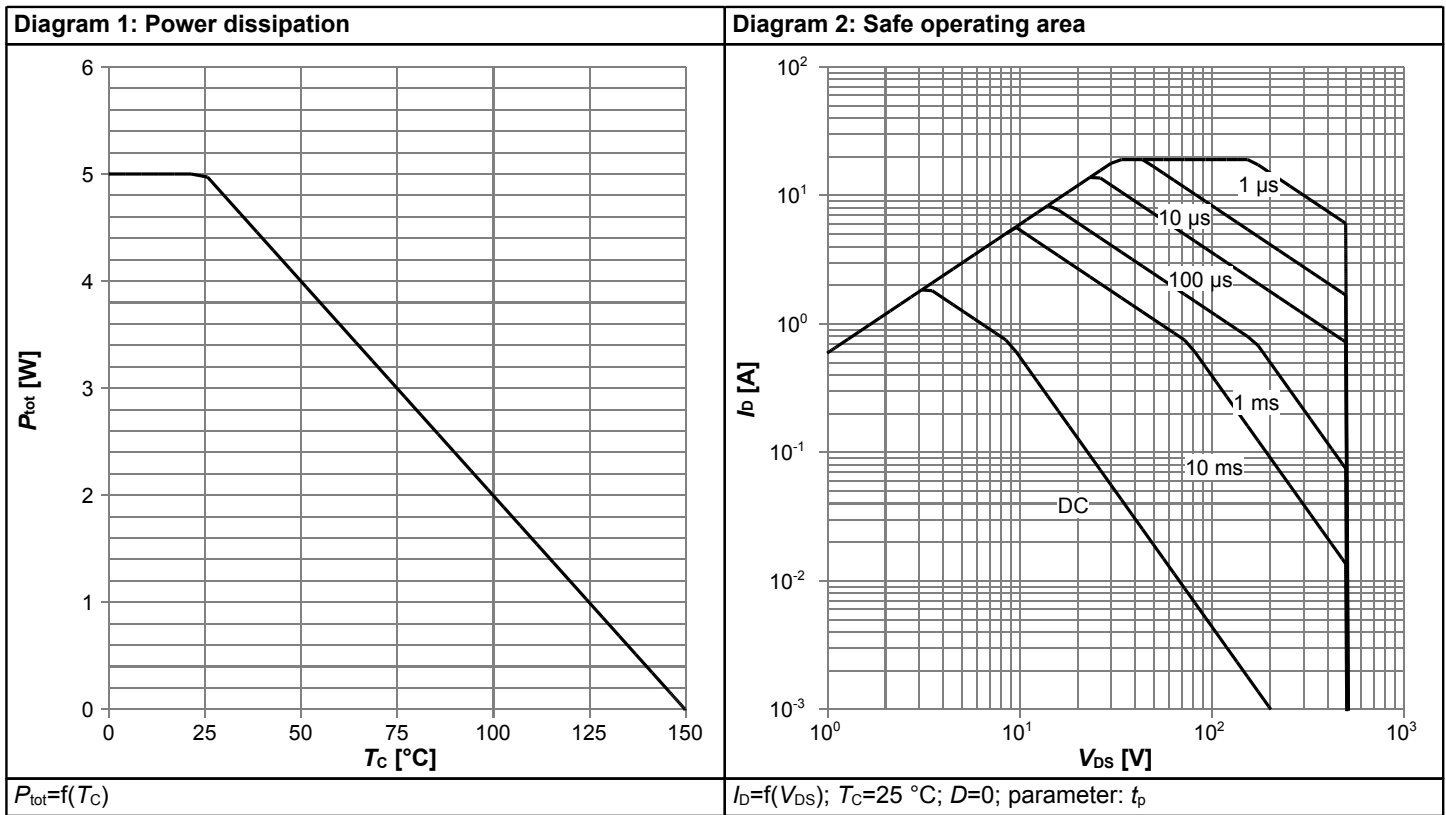
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.84	-	V	$V_{GS}=0V, I_F=2.3A, T_i=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	162	-	ns	$V_R=400V, I_F=2.3A, di_F/dt=100A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	1	-	$\mu C$	$V_R=400V, I_F=2.3A, di_F/dt=100A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	11.1	-	A	$V_R=400V, I_F=2.3A, di_F/dt=100A/\mu s$

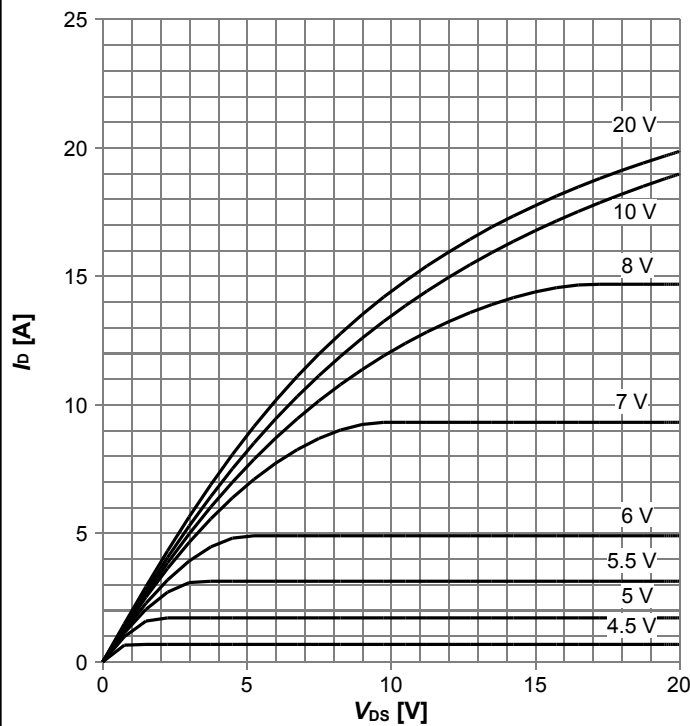
## 4 Electrical characteristics diagrams



# 500V CoolMOS™ CE Power Transistor

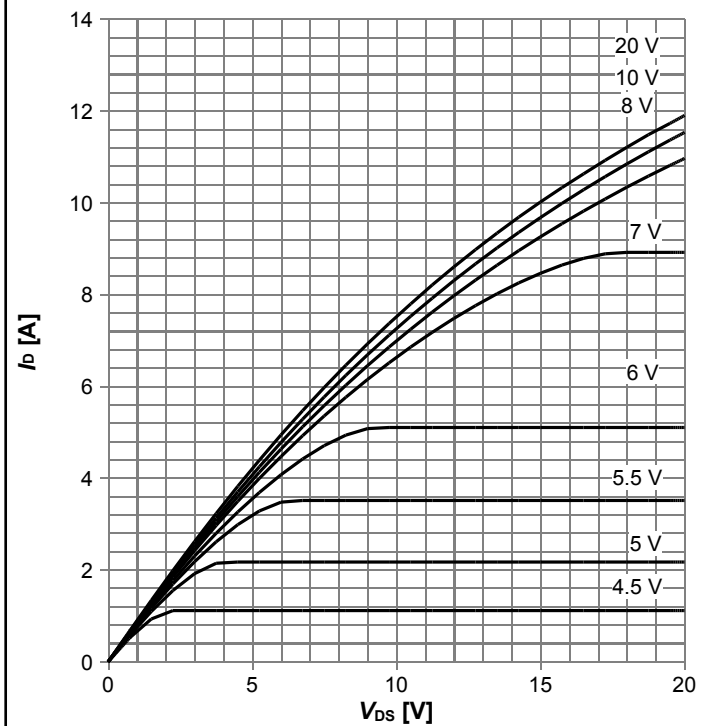
## IPN50R650CE

Diagram 5: Typ. output characteristics



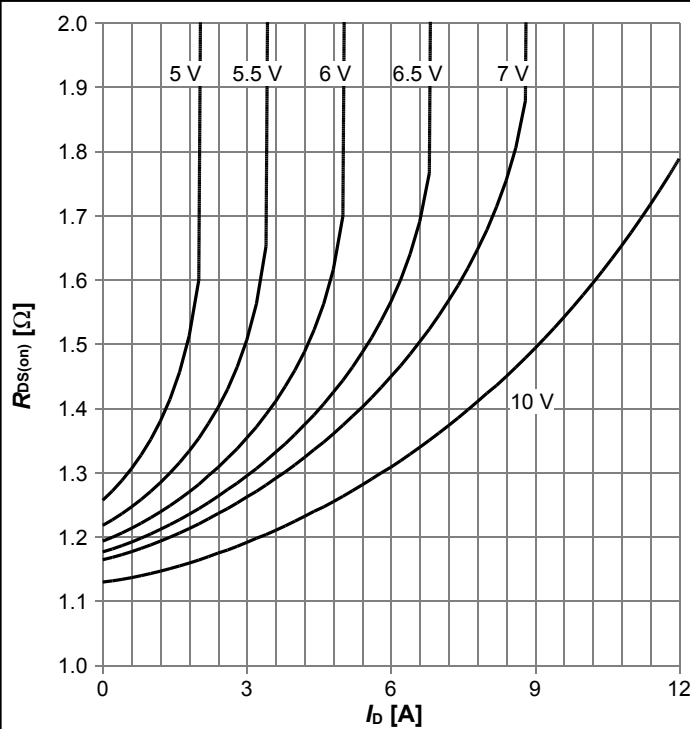
$I_D=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



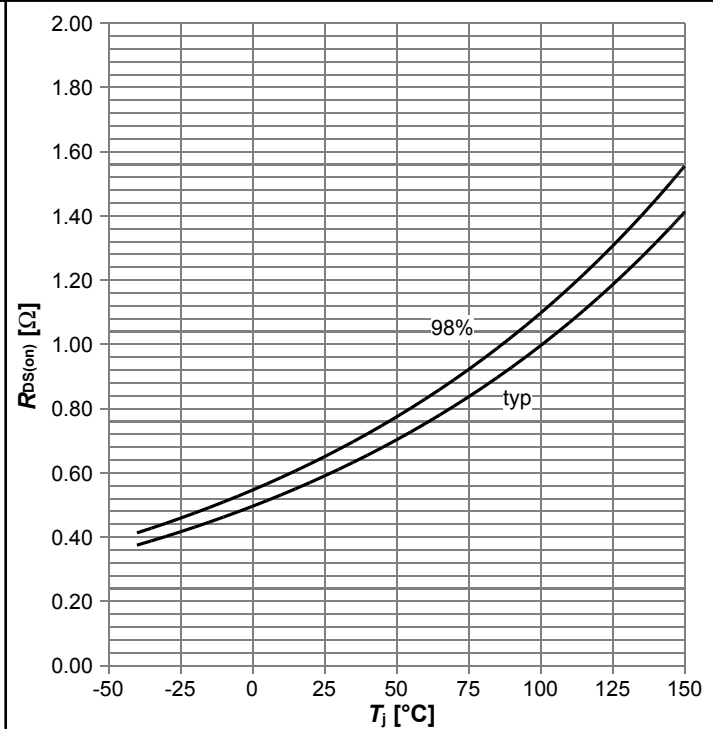
$I_D=f(V_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

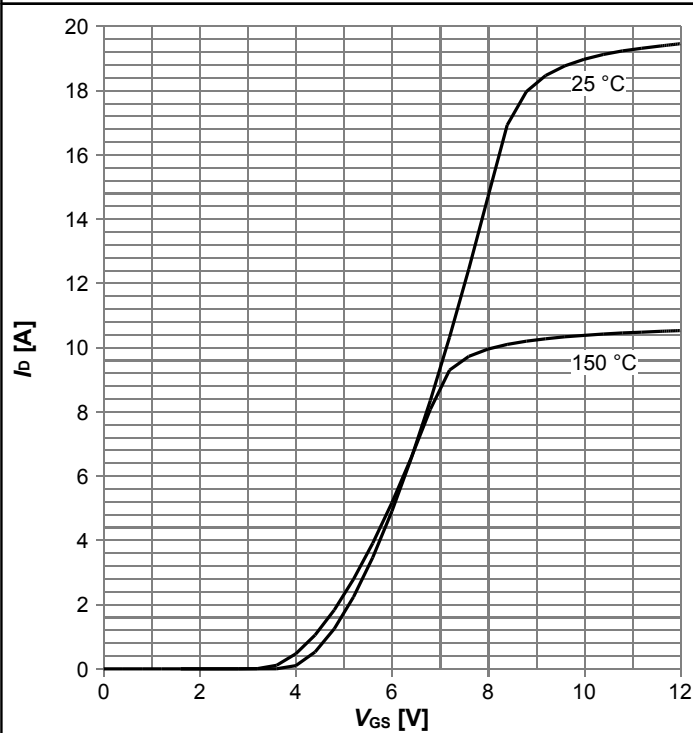
Diagram 8: Drain-source on-state resistance



$R_{DS(on)}=f(T_j)$ ;  $I_D=1.8\text{ A}$ ;  $V_{GS}=13\text{ V}$

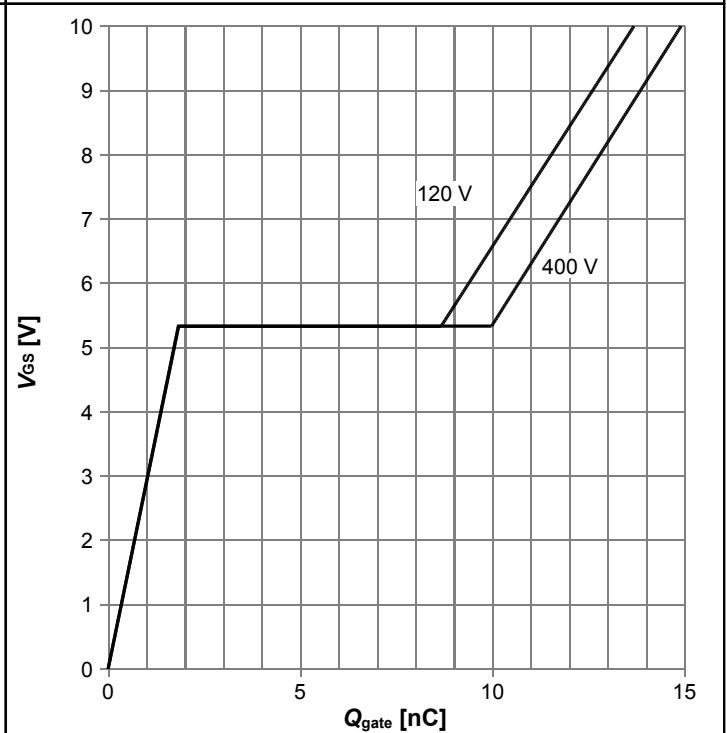
**500V CoolMOS™ CE Power Transistor**  
**IPN50R650CE**

**Diagram 9: Typ. transfer characteristics**



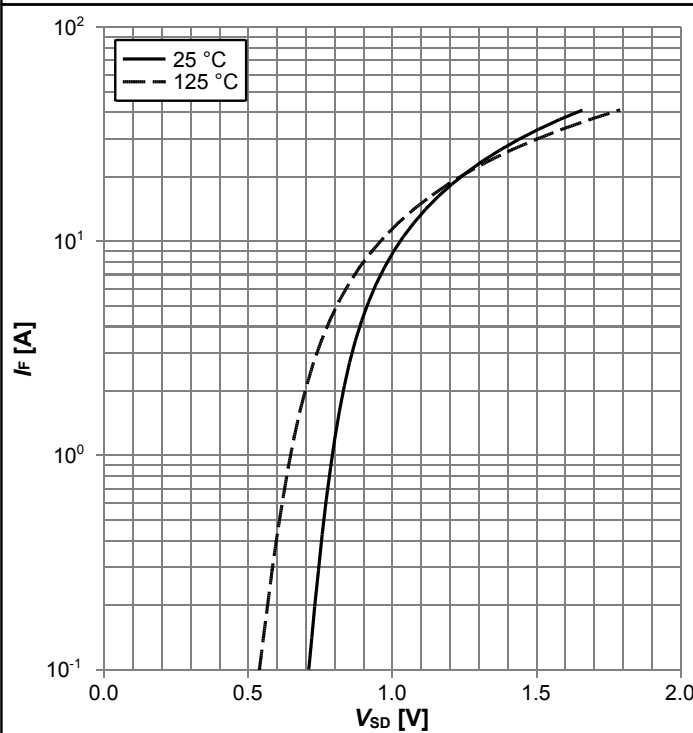
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

**Diagram 10: Typ. gate charge**



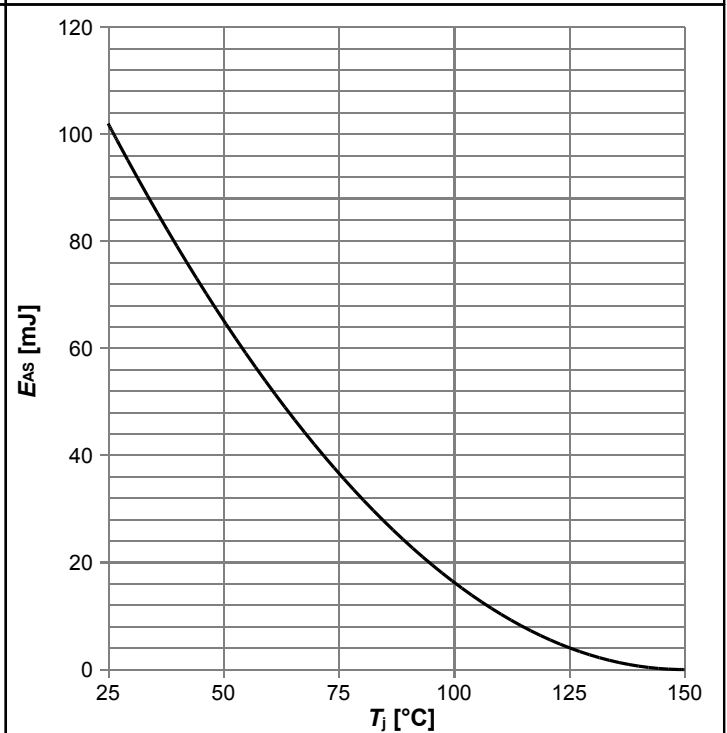
$V_{GS} = f(Q_{gate}); I_D = 2.3 \text{ A pulsed}; \text{parameter: } V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



$I_F = f(V_{SD}); \text{parameter: } T_j$

**Diagram 12: Avalanche energy**



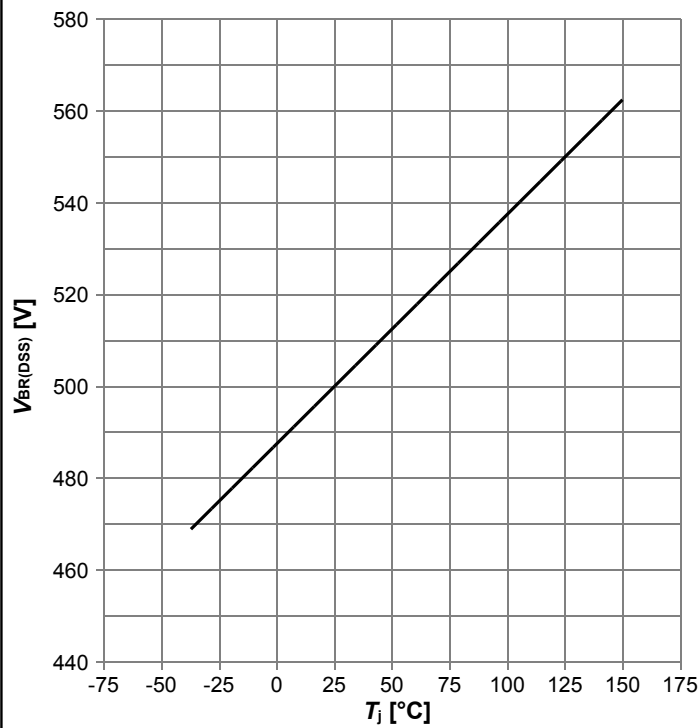
$E_{AS} = f(T_j); I_D = 0.8 \text{ A}; V_{DD} = 50 \text{ V}$



# 500V CoolMOS™ CE Power Transistor

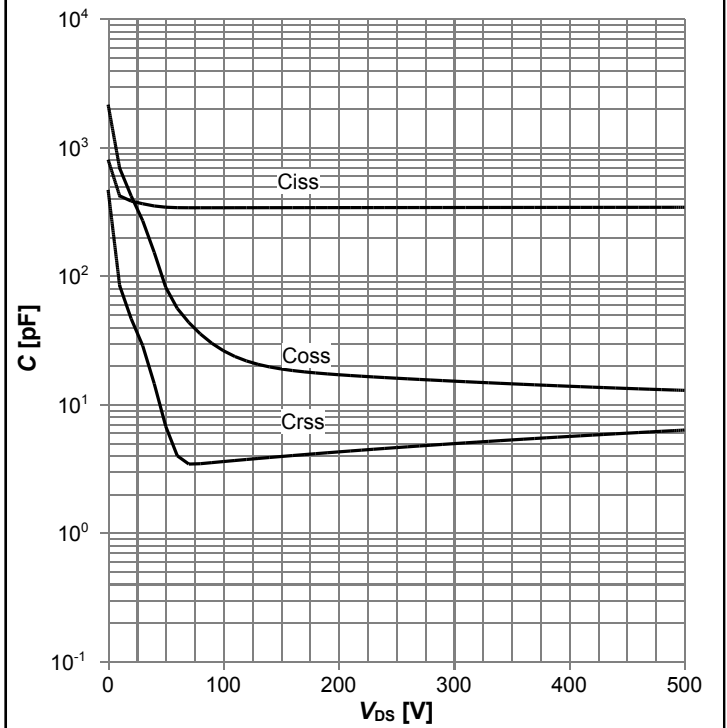
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Diagram 13: Drain-source breakdown voltage



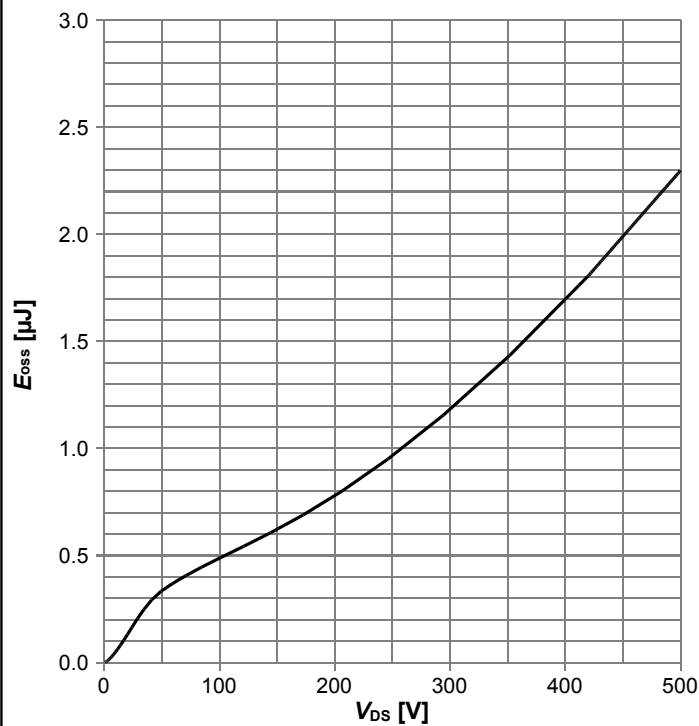
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
<p><math>R_{g1} = R_{g2}</math></p>	<p><math>t_{tr} = t_F + t_S</math>  <math>Q_{tr} = Q_F + Q_S</math></p>

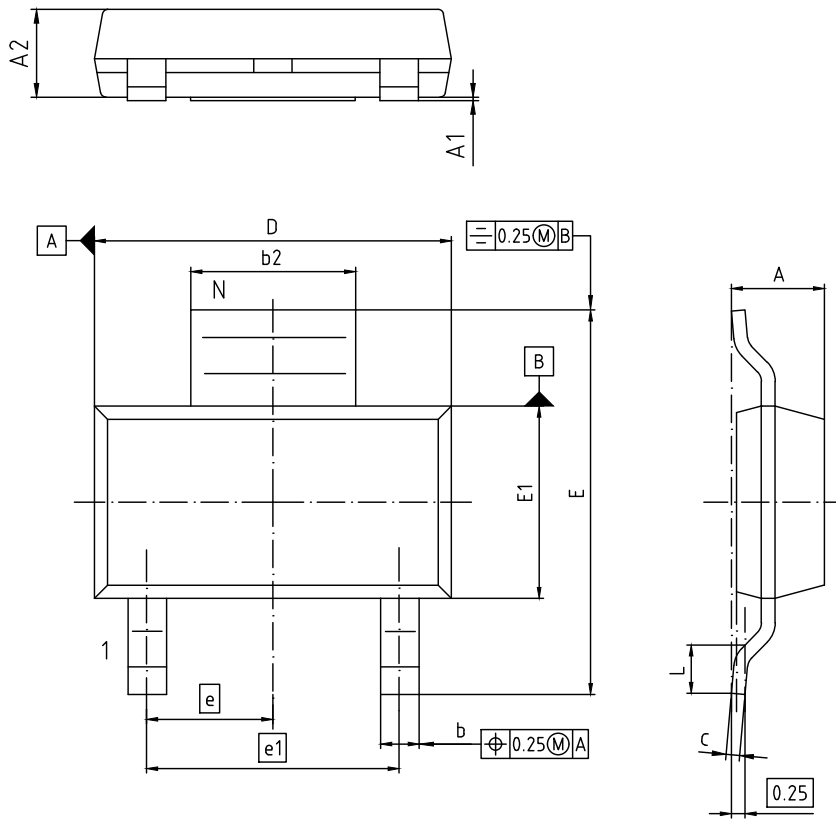
**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

## 6 Package Outlines



NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	1.80	0.060	0.071
A1	-	0.10	-	0.004
A2	1.50	1.70	0.059	0.067
b	0.60	0.80	0.024	0.031
b2	2.95	3.10	0.116	0.122
c	0.24	0.32	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.3 BASIC		0.091 BASIC	
e1	4.6 BASIC		0.181 BASIC	
L	0.75	1.10	0.030	0.043
N	3		3	
O	0°	10°	0°	10°

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Figure 1 Outline PG-SOT223, dimensions in mm/inches

## **7 Appendix A**

### **Table 11 Related Links**

- **IFX CoolMOS Webpage:** [www.infineon.com](http://www.infineon.com)
- **IFX Design tools:** [www.infineon.com](http://www.infineon.com)

## Revision History

IPN50R650CE

**Revision: 2016-06-13, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-04-29	Release of final version
2.1	2016-06-13	Updated ID ratings

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