

## 1. OUTLINE

### 1.1 Features

#### Ultra-low power consumption technology

- VDD = 1.6 V to 3.6 V
- HALT mode
- STOP mode
- SNOOZE mode

#### RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167  $\mu$ s: @ 24 MHz operation with high-speed on-chip oscillator) to ultra-low speed (66.6  $\mu$ s: @ 15 kHz operation with low-speed on-chip oscillator clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register  $\times$  8)  $\times$  4 banks
- On-chip RAM: 0.7 to 3 KB

#### Code flash memory

- Code flash memory: 8 to 32 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

#### Data flash memory

- Data flash memory: 2 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: VDD = 1.8 to 3.6 V

#### High-speed on-chip oscillator

- Select from 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy:  $\pm$ 1.0% (VDD = 1.8 to 3.6 V, TA = -20 to +85°C)

#### Middle-speed on-chip oscillator

- Selectable from 4 MHz, 2 MHz, and 1 MHz.

#### Operating ambient temperature

- TA = -40 to +105°C (G: Industrial applications)

#### Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 12 levels)

#### Data transfer controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

#### Event link controller (ELC)

- Event signals of 20 types can be linked to the specified peripheral function.

#### Serial interfaces

- CSI: 2 channels
- UART: 1 channel
- I<sup>2</sup>C/simplified I<sup>2</sup>C: 2 channels

#### Timers

- 16-bit timer: 4 channels
- 12-bit interval timer: 1 channel
- 8-bit interval timer: 4 channels
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel

#### A/D converter

- 8/12-bit resolution A/D converter (VDD = 1.6 to 3.6 V)
- Analog input: 6 to 17 channels
- Internal reference voltage (1.45 V) and temperature sensor

#### Comparator

- 2 channels
- Operating modes: Comparator high-speed mode, comparator low-speed mode, window mode

#### Operational amplifier

- 4 channels

#### I/O ports

- I/O port: 14 to 42 (N-ch open drain I/O [withstand voltage of 6 V]: 4, N-ch open drain I/O [VDD withstand voltage]: 3 to 7)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

#### Others

- On-chip BCD (binary-coded decimal) correction circuit
- On-chip data operation circuit

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

## ○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/I1D				
			20 pins	24 pins	30 pins	32 pins	48 pins
32 KB	2 KB	3 KB Note	—	—	R5F117AC	R5F117BC	R5F117GC
16 KB	2 KB	2 KB	R5F1176A	R5F1177A	R5F117AA	R5F117BA	R5F117GA
8 KB	2 KB	0.7 KB	R5F11768	R5F11778	R5F117A8	—	—

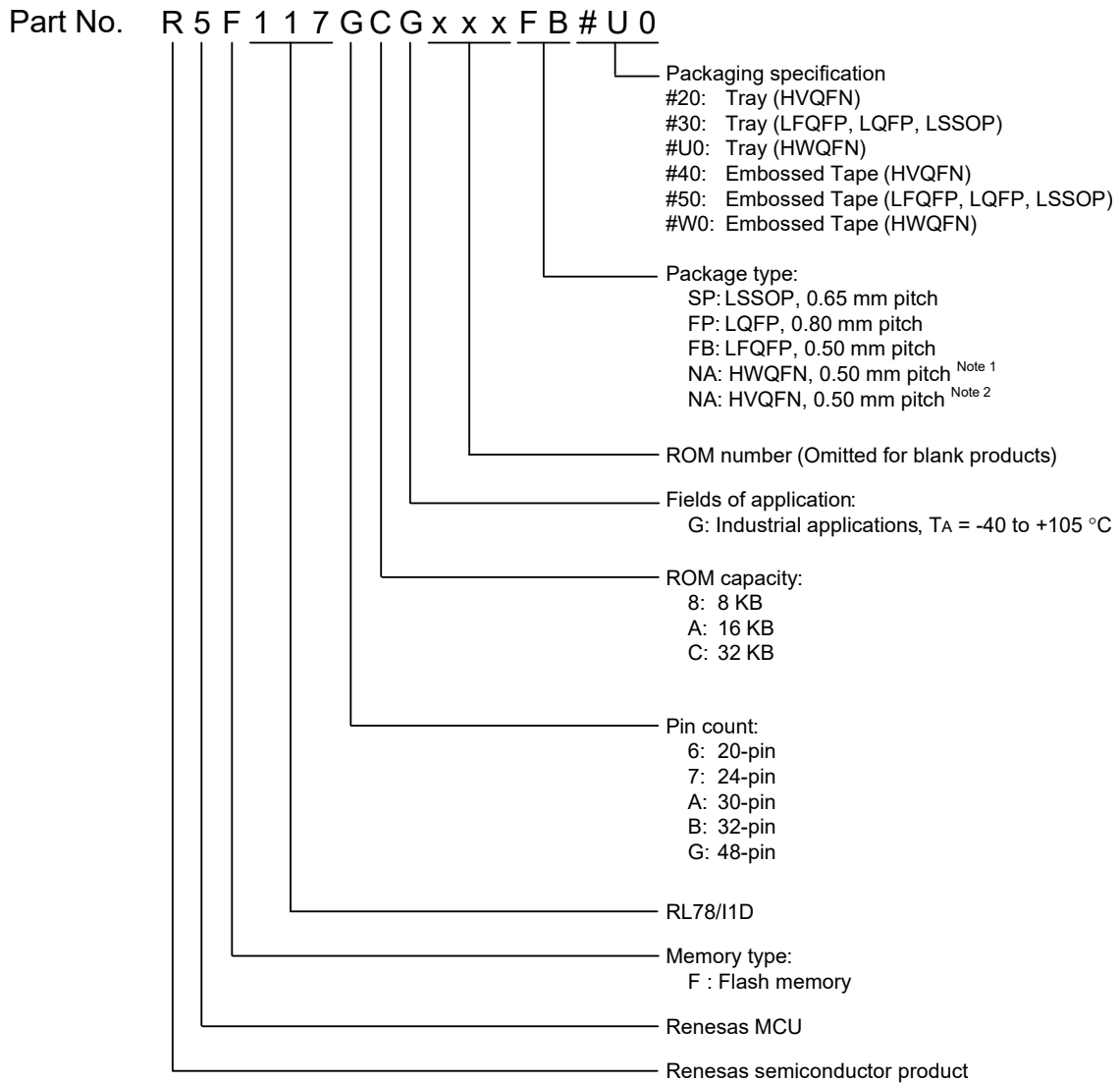
**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.  
The target products and start address of the RAM areas used by the flash library are shown below.

R5F117xC (x = A, B, G): Start address FF300H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

## 1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/I1D



**Note 1.** 24-pin products

**Note 2.** 32-pin products

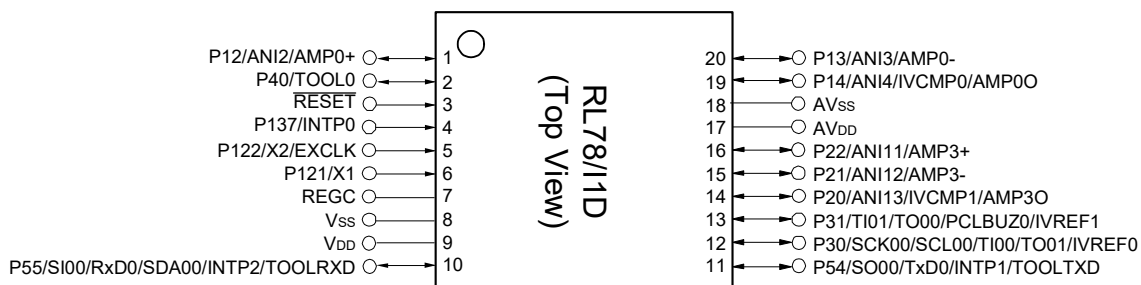
Pin count	Package	Ordering Part Number
20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)	R5F11768GSP#30, R5F1176AGSP#30, R5F11768GSP#50, R5F1176AGSP#50
24 pins	24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)	R5F11778GNA#U0, R5F1177AGNA#U0, R5F11778GNA#W0, R5F1177AGNA#W0
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	R5F117A8GSP#30, R5F117AAGSP#30, R5F117ACGSP#30, R5F117A8GSP#50, R5F117AAGSP#50, R5F117ACGSP#50
32 pins	32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)	R5F117BAGNA#20, R5F117BCGNA#20, R5F117BAGNA#40, R5F117BCGNA#40
	32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)	R5F117BAGFP#30, R5F117BCGFP#30, R5F117BAGFP#50, R5F117BCGFP#50
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	R5F117GAGFB#30, R5F117GCGFB#30, R5F117GAGFB#50, R5F117GCGFB#50

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

### 1.3 Pin Configuration (Top View)

#### 1.3.1 20-pin products

<R> • 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)



**Caution 1.** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

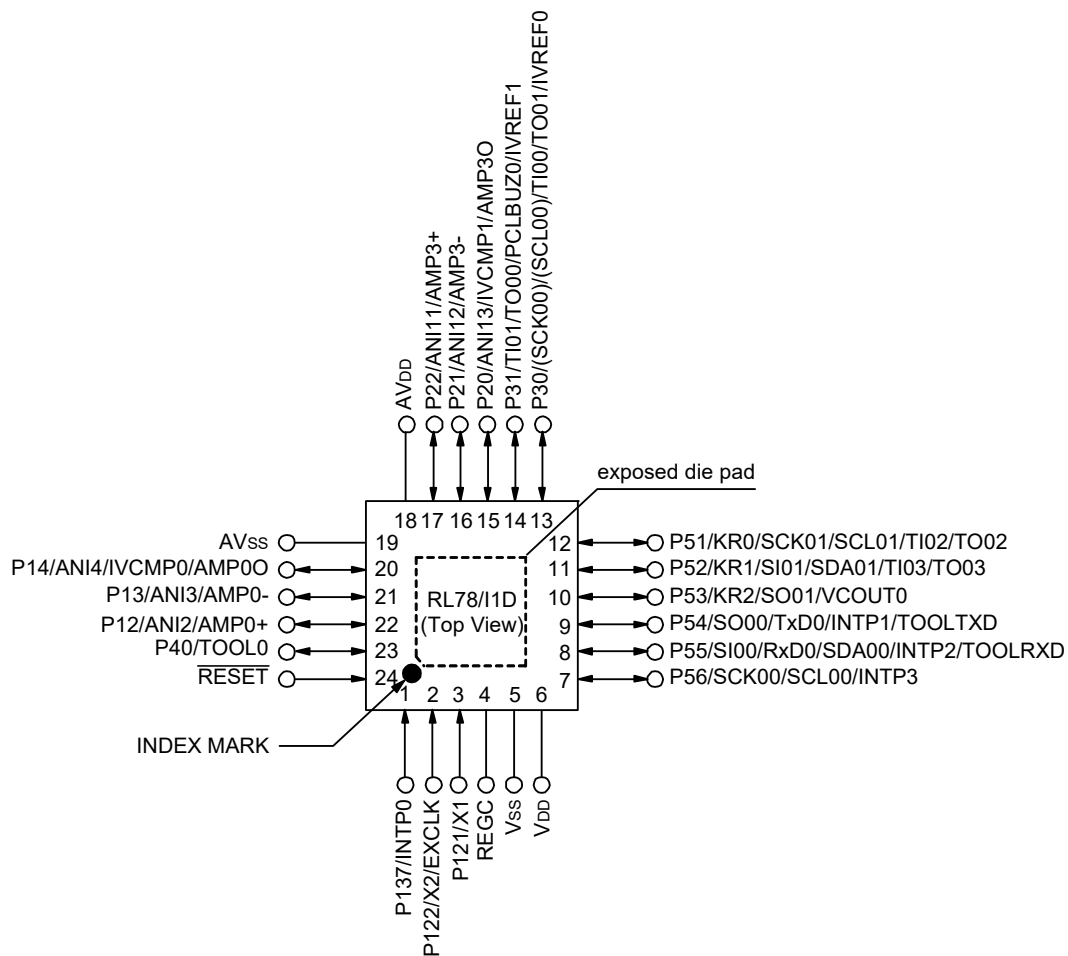
**Caution 2.** Make AVss pin the same potential as Vss pin.

**Caution 3.** Make AVDD pin the same potential as VDD pin.

**Remark** For pin identification, see 1.4 Pin Identification.

### 1.3.2 24-pin products

- <R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



**Caution 1.** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1  $\mu$ F).

**Caution 2.** Make AVss pin the same potential as Vss pin.

**Caution 3.** Make AVDD pin the same potential as VDD pin.

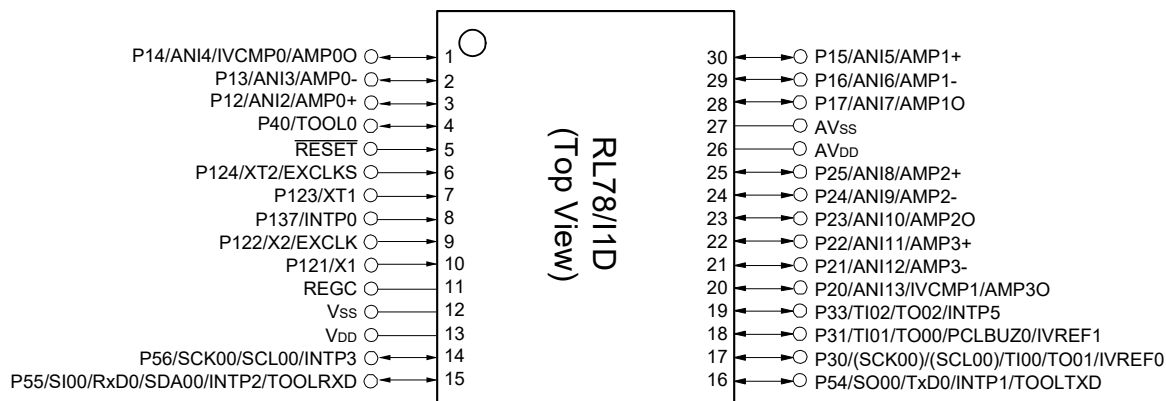
**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** It is recommended to connect an exposed die pad to Vss.

**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

### 1.3.3 30-pin products

<R> • 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



**Caution 1.** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1  $\mu$ F).

**Caution 2.** Make AVss pin the same potential as Vss pin.

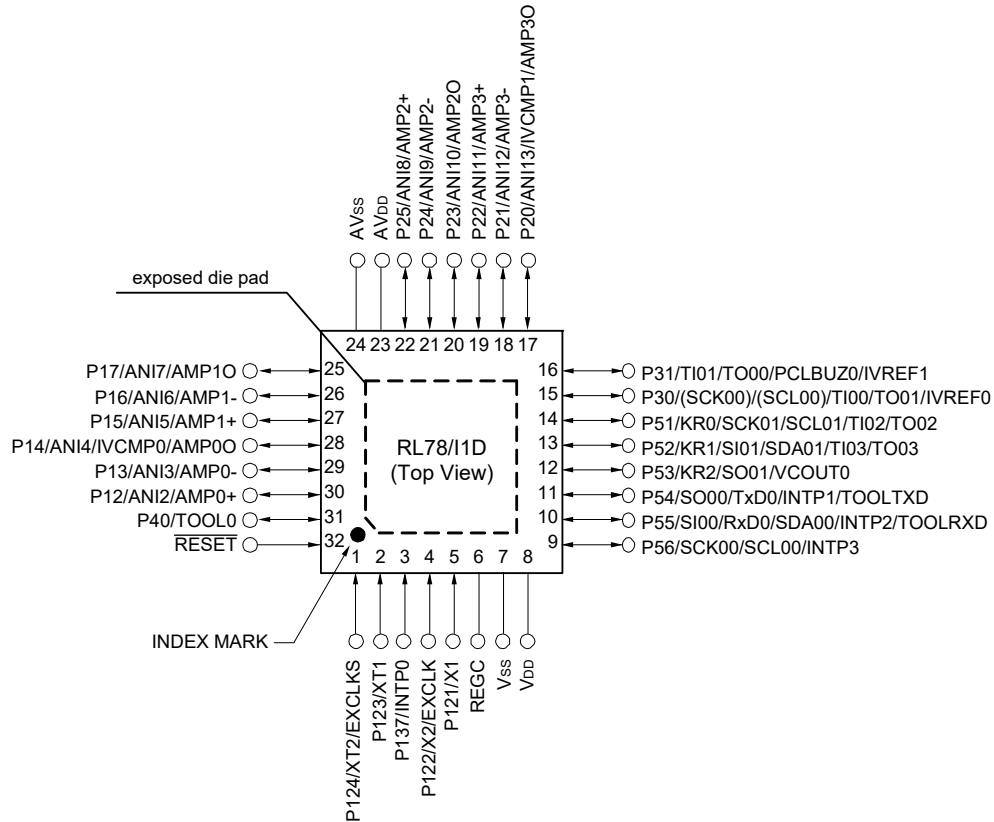
**Caution 3.** Make AVDD pin the same potential as VDD pin.

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

### 1.3.4 32-pin products

- <R> • 32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)



**Caution 1.** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

**Caution 2.** Make AVss pin the same potential as Vss pin.

**Caution 3.** Make AVdd pin the same potential as Vdd pin.

**Remark 1.** For pin identification, see 1.4 Pin Identification.

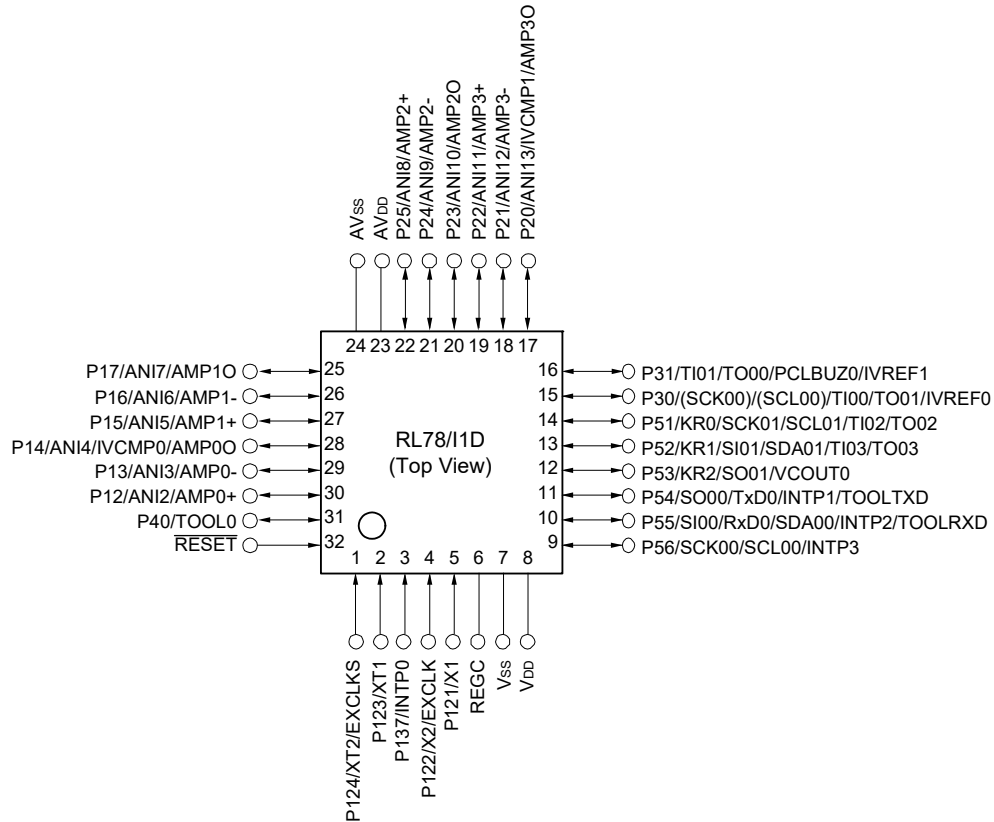
**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

**Remark 3.** It is recommended to connect an exposed die pad to Vss.



<R>

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



**Caution 1.** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

**Caution 2.** Make AVss pin the same potential as Vss pin.

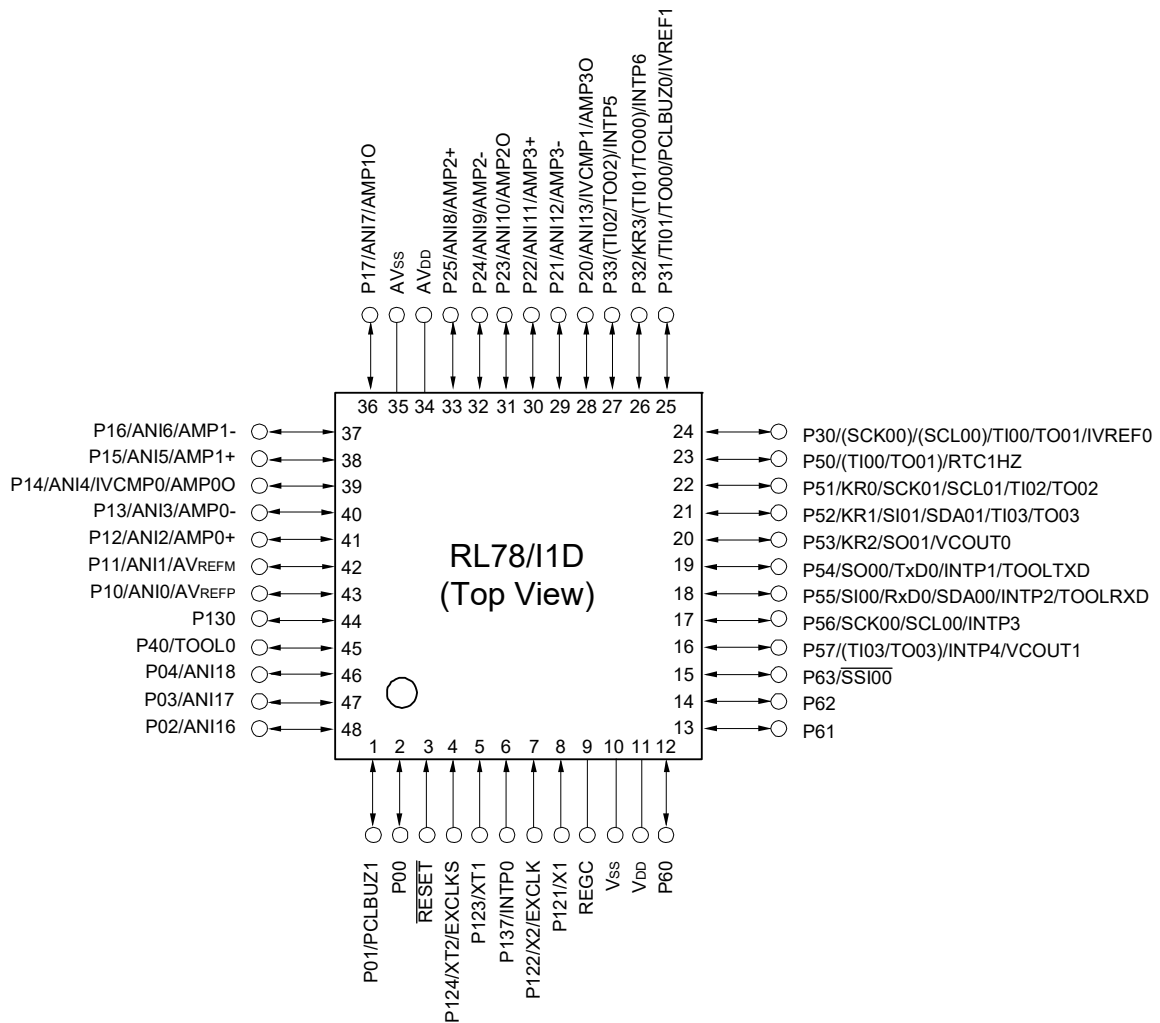
**Caution 3.** Make AVdb pin the same potential as Vdb pin.

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

### 1.3.5 48-pin products

- <R> • 48-pin plastic LQFP (7 × 7 mm, 0.5 mm pitch)



- Caution 1.** Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).
- Caution 2.** Make AVss pin the same potential as Vss pin.
- Caution 3.** Make AVDD pin the same potential as VDD pin.

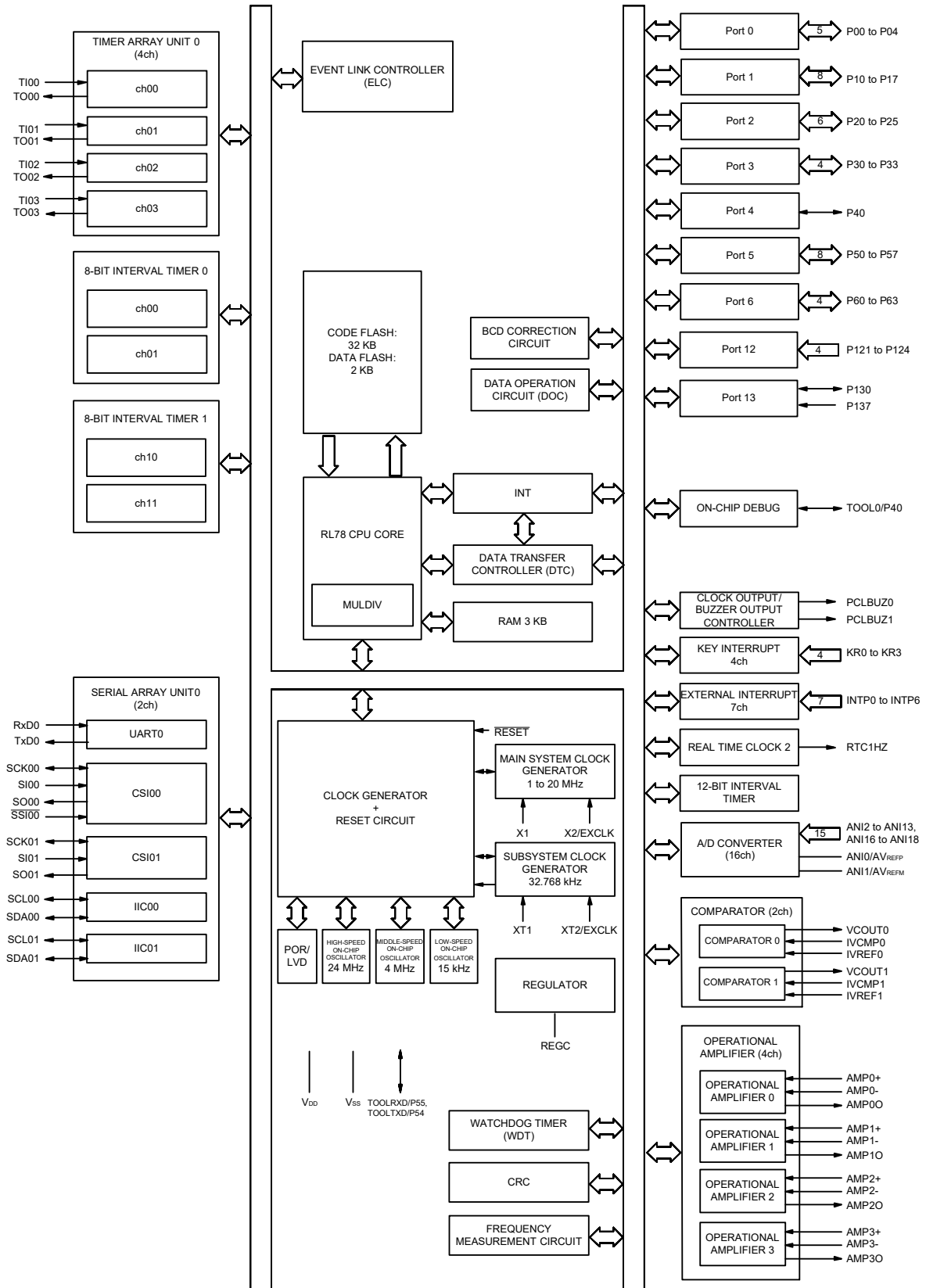
- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

## 1.4 Pin Identification

ANI0 to ANI13, ANI16 to ANI18	: Analog input	PCLBUZ0, PCLBUZ1	: Programmable clock output/buzzer output
AVDD	: Analog power supply	REGC	: Regulator capacitance
AVREFM	: A/D converter reference potential (- side) input	$\overline{\text{RESET}}$	: Reset
AVREFP	: A/D converter reference potential (+ side) input	RTC1HZ	: Real-time clock correction clock (1 Hz) output
AVss	: Analog ground	RxD0	: Receive data
EXCLK	: External clock input (main system clock)	SCK00, SCK01	: Serial clock input/output
EXCLKS	: External clock input (subsystem clock)	SCL00, SCL01	: Serial clock input/output
INTP0 to INTP6	: External interrupt input	SDA00, SDA01	: Serial data input/output
IVCMP0, IVCMP1	: Comparator input	SI00, SI01	: Serial data input
IVREF0, IVREF1	: Comparator reference input	SO00, SO01	: Serial data output
KR0 to KR3	: Key return	$\overline{\text{SSI00}}$	: Serial interface chip select input
P00 to P04	: Port 0	TI00 to TI03	: Timer input
P10 to P17	: Port 1	TO00 to TO03	: Timer output
P20 to P25	: Port 2	TOOL0	: Data input/output for tool
P30 to P33	: Port 3	TOOLRXD, TOOLTXD	: Data input/output for external device
P40	: Port 4	TxD0	: Transmit data
P50 to P57	: Port 5	VCOU0, VCOU1	: Comparator output
P60 to P63	: Port 6	AMP0+, AMP1+, AMP2+, AMP3+	: Operational amplifier (+side) input
P121 to P124	: Port 12	AMP0-, AMP1-, AMP2-, AMP3-	: Operational amplifier (-side) input
P130, P137	: Port 13	AMP0O, AMP1O, AMP2O, AMP3O	: Operational amplifier output
		VDD	: Power supply
		Vss	: Ground
		X1, X2	: Crystal oscillator (main system clock)
		XT1, XT2	: Crystal oscillator (subsystem clock)

## 1.5 Block Diagram

### 1.5.1 48-pin products



## 1.6 Outline of Functions

**Remark** This outline describes the functions at the time when Peripheral I/O redirection register 0 (PIOR0) are set to 00H.

(1/2)

Item		20-pin	24-pin	30-pin	32-pin	48-pin
		R5F1176x (x = 8, A)	R5F1177x (x = 8, A)	R5F117Ax (x = 8, A, C)	R5F117Bx (x = A, C)	R5F117Gx (x = A, C)
Code flash memory (KB)		8 to 16 KB	8 to 16 KB	8 to 32 KB	16 to 32 KB	16 to 32 KB
Data flash memory (KB)		2 KB	2 KB	2 KB	2 KB	2 KB
RAM		0.7 to 2.0 KB	0.7 to 2.0 KB	0.7 to 3.0 KB Note	2.0 to 3.0 KB Note	2.0 to 3.0 KB Note
Address space		1 MB				
<R>	Main system clock	High-speed system clock (f <sub>MX</sub> ) X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V <sub>DD</sub> = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 3.6 V), LP (Low-power main) mode: 1 MHz (V <sub>DD</sub> = 1.8 to 3.6 V)				
	High-speed on-chip oscillator clock (f <sub>IH</sub> ) Max: 24 MHz	HS (High-speed main) mode: 1 to 24 MHz (V <sub>DD</sub> = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 3.6 V), LP (Low-power main) mode: 1 MHz (V <sub>DD</sub> = 1.8 to 3.6 V)				
	Middle-speed on-chip oscillator clock (f <sub>IM</sub> ) Max: 4 MHz	HS (High-speed main) mode: 1 to 24 MHz (V <sub>DD</sub> = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 3.6 V), LP (Low-power main) mode: 1 MHz (V <sub>DD</sub> = 1.8 to 3.6 V)				
Subsystem clock	Subsystem clock oscillator (f <sub>SX</sub> , f <sub>SXR</sub> )	—		XT1 (crystal) oscillation 32.768 kHz (TYP.): V <sub>DD</sub> = 1.6 to 3.6 V		
	Low-speed on-chip oscillator clock (f <sub>IL</sub> )	15 kHz (TYP.): V <sub>DD</sub> = 1.6 to 3.6 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f <sub>IH</sub> = 24 MHz operation)				
		0.05 μs (High-speed system clock: f <sub>MX</sub> = 20 MHz operation)				
		—		30.5 μs (Subsystem clock oscillator clock: f <sub>SX</sub> = 32.768 kHz operation)		
Instruction set		<ul style="list-style-type: none"> <li>• Data transfer (8/16 bits)</li> <li>• Adder and subtractor/logical operation (8/16 bits)</li> <li>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)</li> <li>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)</li> <li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li> </ul>				
I/O port	Total	14	18	24	26	42
	CMOS I/O	11	15	19	21	33
	CMOS input	3	3	5	5	5
	N-ch open-drain I/O (6 V tolerance)	—	—	—	—	4
Timer	16-bit timer	4 channels				
	Watchdog timer	1 channel				
	Real-time clock	1 channel				
	12-bit interval timer	1 channel				
	8/16-bit interval timer	4 channels (8 bit) / 2 channels (16 bit)				
	Timer output	2	4	3	4	4
	RTC output	—		1 channel • 1 Hz (subsystem clock generator and RTC/other clock: f <sub>SX</sub> = 32.768 kHz)		

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F117xC (x = A, B, G): Start address FF300H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

Item	20-pin	24-pin	30-pin	32-pin	48-pin
	R5F1176x (x = 8, A)	R5F1177x (x = 8, A)	R5F117Ax (x = 8, A, C)	R5F117Bx (x = A, C)	R5F117Gx (x = A, C)
Clock output/buzzer output	1	1	1	1	2
	[20-pin, 24-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f <sub>MAIN</sub> = 20 MHz operation) [30-pin, 32-pin, 48-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f <sub>MAIN</sub> = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (subsystem clock generator and RTC/other clock: f <sub>SXR</sub> = 32.768 kHz operation)				
12-bit resolution A/D converter	6 channels	6 channels	12 channels	12 channels	17 channels
Comparator (Window Comparator)	2 channels				
Operational amplifier	2 channels		4 channels		
Data Operation Circuit (DOC)	Comparison, addition, and subtraction of 16-bit data				
Serial interface	[20-pin, 30-pin products] • CSI: 1 channel/UART: 1 channel/simplified I <sup>2</sup> C: 1 channel [24-pin, 32-pin, 48-pin products] • CSI: 2 channels/UART: 1 channel/simplified I <sup>2</sup> C: 2 channels				
Data transfer controller (DTC)	16 sources	20 sources	19 sources	20 sources	22 sources
Event link controller (ELC)	Event input: 15 Event trigger output: 5	Event input: 17 Event trigger output: 5	Event input: 17 Event trigger output: 7	Event input: 17 Event trigger output: 7	Event input: 20 Event trigger output: 7
Vectored interrupt sources	Internal	22	22	24	24
	External	3	5	5	5
Key interrupt	—	3	—	3	4
Reset	<ul style="list-style-type: none"> <li>• Reset by <u>RESET</u> pin</li> <li>• Internal reset by watchdog timer</li> <li>• Internal reset by power-on-reset</li> <li>• Internal reset by voltage detector</li> <li>• Internal reset by illegal instruction execution <sup>Note</sup></li> <li>• Internal reset by RAM parity error</li> <li>• Internal reset by illegal-memory access</li> </ul>				
Power-on-reset circuit	<ul style="list-style-type: none"> <li>• Power-on-reset: 1.51 ± 0.04V (T<sub>A</sub> = -40 to +85°C)</li> <li>• Power-down-reset: 1.50 ± 0.04 V (T<sub>A</sub> = -40 to +85°C)</li> </ul>				
Voltage detector	Power on	1.67 V to 3.13 V (12 stages)			
	Power down	1.63 V to 3.06 V (12 stages)			
On-chip debug function	Provided (Enable to tracing)				
Power supply voltage	V <sub>DD</sub> = 1.6 to 3.6 V				
Operating ambient temperature	T <sub>A</sub> = -40 to +105°C				

The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

## 2. ELECTRICAL SPECIFICATIONS

**Caution 1.** The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

**Caution 2.** The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/I1D User's Manual.

**Caution 3.** Please contact Renesas Electronics sales office for derating of operation under  $T_A = +85$  to  $+105^\circ\text{C}$ . Derating is the systematic reduction of load for the sake of improved reliability.

**Caution 4.** When operating temperature exceeds  $85^\circ\text{C}$ , only HS (high-speed main) mode can be used as the flash operation mode. Regulator mode should be used with the normal setting (MCSEL = 0).

## 2.1 Absolute Maximum Ratings

### Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$ , $AV_{DD}$	$V_{DD} = AV_{DD}$	-0.3 to + 4.6	V
	$AV_{REFP}$		0.3 to $AV_{DD} + 0.3$ Note 2	V
	$AV_{SS}$		-0.5 to + 0.3	V
	$AV_{REFM}$		-0.3 to $AV_{DD} + 0.3$ Note 2 and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	$V_{IREGC}$	REGC	-0.3 to + 2.8 and -0.3 to $V_{DD} + 0.3$ Note 1	V
Input voltage	$V_{I1}$	P00 to P04, P30 to P33, P40, P50 to P57, P121 to P124, P130, P137, EXCLK, EXCLKS, $\overline{RESET}$	-0.3 to $V_{DD} + 0.3$ Note 2	V
	$V_{I2}$	P60 to P63 (N-ch open-drain)	-0.3 to + 6.5	V
	$V_{I3}$	P10 to P17, P20 to P25	-0.3 to $AV_{DD} + 0.3$ Note 2	V
Output voltage	$V_{O1}$	P00 to P04, P30 to P33, P40, P50 to P57, P60 to P63, P130	-0.3 to $V_{DD} + 0.3$ Note 2	V
	$V_{O2}$	P10 to P17, P20 to P25	-0.3 to $AV_{DD} + 0.3$ Note 2	V
Analog input voltage	$V_{AI1}$	ANI16 to ANI18	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3$ Notes 2, 3	V
	$V_{AI2}$	ANI0 to ANI13	-0.3 to $AV_{DD} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3$ Notes 2, 3	V
	$V_{AI3}$	Operational amplifier input pin	-0.3 to $AV_{DD} + 0.3$ Note 2	V

**Note 1.** Connect the REGC pin to  $V_{SS}$  via a capacitor (0.47 to 1  $\mu$ F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Must be 4.6 V or lower.

**Note 3.** Do not exceed  $AV_{REF}(+) + 0.3$  V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.**  $AV_{REF}(+)$ : + side reference voltage of the A/D converter.

**Remark 3.**  $V_{SS}$ : Reference voltage



**Absolute Maximum Ratings****(2/2)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P04, P30 to P33, P40, P50 to P57, P130	-40	mA
		Total of all pins -170 mA	P00 to P04, P40, P130	-70	mA
			P30 to P33, P50 to P57	-100	mA
	IOH2	Per pin	P10 to P17, P20 to P25	-0.1	mA
		Total of all pins		-1.4	mA
	Output current, low	IOL1	Per pin	P00 to P04, P30 to P33, P40, P50 to P57, P60 to P63, P130	40
Total of all pins 170 mA			P00 to P04, P40, P130	70	mA
			P30 to P33, P50 to P57, P60 to P63	100	mA
IOL2		Per pin	P10 to P17, P20 to P25	0.4	mA
		Total of all pins		5.6	mA
Operating ambient temperature		TA	In normal operation mode		-40 to +105
	In flash memory programming mode				
Storage temperature	Tstg			-65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 characteristics

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f <sub>X</sub> ) <sup>Note</sup>	Ceramic resonator/ crystal resonator	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V	1.0		20.0	MHz
		2.4 V ≤ V <sub>DD</sub> < 2.7 V	1.0		16.0	
		1.8 V ≤ V <sub>DD</sub> < 2.4 V	1.0		8.0	
		1.6 V ≤ V <sub>DD</sub> < 1.8 V	1.0		4.0	
XT1 clock oscillation frequency (f <sub>XT</sub> ) <sup>Note</sup>	Crystal resonator		32	32.768	35	kHz

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/I1D User's Manual.

### 2.2.2 On-chip oscillator characteristics

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit	
High-speed on-chip oscillator clock frequency <sup>Notes 1, 2</sup>	f <sub>IH</sub>		1		24	MHz	
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V	-1.0		+1.0	%
			1.6 V ≤ V <sub>DD</sub> < 1.8 V	-5.0		+5.0	
		-40 to -20°C	1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V	-1.5		+1.5	%
			1.6 V ≤ V <sub>DD</sub> < 1.8 V	-5.5		+5.5	
+85 to +105°C	2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V	-2.0		+2.0	%		
Middle-speed on-chip oscillator oscillation frequency <sup>Note 2</sup>	f <sub>IM</sub>		1		4	MHz	
Middle-speed on-chip oscillator oscillation frequency accuracy		1.8V ≤ V <sub>DD</sub> ≤ 3.6V	-12		+12	%	
Low-speed on-chip oscillator clock frequency <sup>Note 2</sup>	f <sub>IL</sub>			15		kHz	
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%	

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high Note 1	IOH1	Per pin for P00 to P04, P30 to P33, P40, P50 to P57, P130	TA = -40 to +85°C			-10.0 Note 2	mA
			TA = +85 to +105°C			-3.0 Note 2	mA
	Total of P00 to P04, P40, P130 (When duty ≤ 70% Note 3)		2.7 V ≤ VDD ≤ 3.6 V			-10.0	mA
			1.8 V ≤ VDD < 2.7 V			-5.0	mA
			1.6 V ≤ VDD < 1.8 V			-2.5	mA
	Total of P30 to P33, P50 to P57 (When duty ≤ 70% Note 3)		2.7 V ≤ VDD ≤ 3.6 V			-19.0	mA
			1.8 V ≤ VDD < 2.7 V			-10.0	mA
			1.6 V ≤ VDD < 1.8 V			-5.0	mA
	Total of all pins (When duty ≤ 70% Note 3)					-29.0	mA
	IOH2	Per pin for P10 to P17, P20 to P25				-0.1 Note 2	mA
Total of all pins (When duty ≤ 70% Note 3)			1.6 V ≤ VDD ≤ 3.6 V			-1.4	mA

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the VDD pin to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOH = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Caution** P30 and P51 to P56 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

( $T_A = +85$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P04, P30 to P33, P40, P50 to P57, P130	$T_A = -40$ to $+85^\circ\text{C}$		20.0 Note 2	mA
			$T_A = +85$ to $+105^\circ\text{C}$		8.5 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40, P130 (When duty $\leq 70\%$ Note 3)	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		15.0	mA
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		9.0	mA
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		4.5	mA
		Total of P30 to P33, P50 to P57, P60 to P63 (When duty $\leq 70\%$ Note 3)	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		35.0	mA
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$		20.0	mA
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		10.0	mA
		Total of all pins (When duty $\leq 70\%$ Note 3)			50.0	mA
	IOL2	Per pin for P10 to P17, P20 to P25			0.4 Note 2	mA
			$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$		5.6	mA

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the Vss pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor  $\leq 70\%$ .

The output current value that has changed to the duty factor  $> 70\%$  the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins =  $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

( $T_A = +85$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	$V_{IH1}$	P00 to P04, P30 to P33, P40, P50 to P57, P130	Normal input buffer	$0.8 V_{DD}$		$V_{DD}$	V
	$V_{IH2}$	P30, P32, P33, P51, P52, P54 to P57	TTL input buffer $3.3\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	2.0		$V_{DD}$	V
			TTL input buffer $1.6\text{ V} \leq V_{DD} < 3.3\text{ V}$	1.5		$V_{DD}$	V
	$V_{IH3}$	P10 to P17, P20 to P25		$0.7 AV_{DD}$		$AV_{DD}$	V
	$V_{IH4}$	P60 to P63		$0.7 V_{DD}$		6.0	V
	$V_{IH5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		$0.8 V_{DD}$		$V_{DD}$	V
Input voltage, low	$V_{IL1}$	P00 to P04, P30 to P33, P40, P50 to P57, P130	Normal input buffer	0		$0.2 V_{DD}$	V
	$V_{IL2}$	P30, P32, P33, P51, P52, P54 to P57	TTL input buffer $3.3\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	0		0.5	V
			TTL input buffer $1.6\text{ V} \leq V_{DD} < 3.3\text{ V}$	0		0.32	V
	$V_{IL3}$	P10 to P17, P20 to P25		0		$0.3 AV_{DD}$	V
	$V_{IL4}$	P60 to P63		0		$0.3 V_{DD}$	V
	$V_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		$0.2 V_{DD}$	V

**Caution** The maximum value of  $V_{IH}$  of pins P30 and P51 to P56 is  $V_{DD}$ , even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

( $T_A = +85$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, high	VOH1	P00 to P04, P30 to P33, P40, P50 to P57, P130	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OH} = -2.0\text{ mA}$			$V_{DD} - 0.6$	V
			$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ Note 3, $I_{OH} = -1.5\text{ mA}$			$V_{DD} - 0.5$	V
			$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ Note 1, $I_{OH} = -1.0\text{ mA}$			$V_{DD} - 0.5$	V
	VOH2	P10 to P17, P20 to P25	$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ Note 2, $I_{OH} = -100\text{ }\mu\text{A}$			$AV_{DD} - 0.5$	V
Output voltage, low	VOL1	P00 to P04, P30 to P33, P40, P50 to P57, P130	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 3.0\text{ mA}$			0.6	V
			$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 1.5\text{ mA}$			0.4	V
			$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ Note 3, $I_{OL} = 0.6\text{ mA}$			0.4	V
			$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ Note 1, $I_{OL} = 0.3\text{ mA}$			0.4	V
	VOL2	P10 to P17, P20 to P25	$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ Note 2, $I_{OL} = 400\text{ }\mu\text{A}$			0.4	V
	VOL3	P60 to P63	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 3.0\text{ mA}$			0.4	V
			$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ Note 3, $I_{OL} = 2.0\text{ mA}$			0.4	V
			$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ Note 1, $I_{OL} = 1.0\text{ mA}$			0.4	V

**Note 1.** Only  $T_A = -40$  to  $+85^\circ\text{C}$  is guaranteed.

**Note 2.** The condition that  $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$  is guaranteed when  $+85^\circ\text{C} < T_A \leq +105^\circ\text{C}$ .

**Note 3.** The condition that  $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  is guaranteed when  $+85^\circ\text{C} < T_A \leq +105^\circ\text{C}$ .

**Caution** P30 and P51 to P56 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	ILI1H1	P00 to P04, P30 to P33, P40, P50 to P57, P60 to P63, P130, P137	VI = VDD		1	μA		
	ILI1H2	RESET	VI = VDD		1	μA		
	ILI1H3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI = VDD		1	μA		
			In input port or external clock input		10	μA		
ILI1H4	P10 to P17, P20 to P25	VI = AVDD		1	μA			
Input leakage current, low	ILI1L1	P00 to P04, P30 to P33, P40, P50 to P57, P60 to P63, P130, P137	VI = VSS		-1	μA		
	ILI1L2	RESET	VI = VSS		-1	μA		
	ILI1L3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI = VSS		-1	μA		
			In input port or external clock input		-10	μA		
ILI1L4	P10 to P17, P20 to P25	VI = AVSS		-1	μA			
On-chip pull-up resistance	RU	P00 to P04, P30 to P33, P40, P50 to P57, P130	VI = VSS, In input port		10	20	100	kΩ

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 2.3.2 Supply current characteristics

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f <sub>HI</sub> = 24 MHz Note 3, T <sub>A</sub> = -40 to +105°C	Basic operation	V <sub>DD</sub> = 3.0 V		1.4		mA	
			HS (high-speed main) mode	f <sub>HI</sub> = 24 MHz Note 3, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V		3.2	6.3	mA	
				f <sub>HI</sub> = 24 MHz Note 3, T <sub>A</sub> = +85 to +105°C	Normal operation	V <sub>DD</sub> = 3.0 V			6.7	mA	
				f <sub>HI</sub> = 16 MHz Note 3, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V		2.4	4.6	mA	
				f <sub>HI</sub> = 16 MHz Note 3, T <sub>A</sub> = +85 to +105°C	Normal operation	V <sub>DD</sub> = 3.0 V			4.9	mA	
				LS (low-speed main) mode (MCSEL = 0)	f <sub>HI</sub> = 8 MHz Note 3, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V		1.1	2.0	mA
						V <sub>DD</sub> = 2.0 V		1.1	2.0	mA	
			LS (low-speed main) mode (MCSEL = 1)	f <sub>HI</sub> = 4 MHz Note 3, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V		0.72	1.30	mA	
						V <sub>DD</sub> = 2.0 V		0.72	1.30	mA	
				f <sub>IM</sub> = 4 MHz Note 7, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V		0.58	1.10	mA	
						V <sub>DD</sub> = 2.0 V		0.58	1.10	mA	
			LV (low-voltage main) mode	f <sub>HI</sub> = 3 MHz Note 3, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V		1.2	1.8	mA	
						V <sub>DD</sub> = 2.0 V		1.2	1.8	mA	
			LP (low-power main) mode Note 5 (MCSEL = 1)	f <sub>HI</sub> = 1 MHz Note 3, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V		290	480	μA	
						V <sub>DD</sub> = 2.0 V		290	480	μA	
				f <sub>IM</sub> = 1 MHz Note 5, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V		124	230	μA	
						V <sub>DD</sub> = 2.0 V		124	230	μA	
			HS (high-speed main) mode	f <sub>MX</sub> = 20 MHz Note 2, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V	Square wave input		2.7	5.3	mA
							Resonator connection		2.8	5.5	mA
				f <sub>MX</sub> = 20 MHz Note 2, T <sub>A</sub> = +85 to +105°C	Normal operation	V <sub>DD</sub> = 3.0 V	Square wave input			5.7	mA
							Resonator connection			5.8	mA
				f <sub>MX</sub> = 10 MHz Note 2, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V	Square wave input		1.8	3.1	mA
							Resonator connection		1.9	3.2	mA
				f <sub>MX</sub> = 10 MHz Note 2, T <sub>A</sub> = +85 to +105°C	Normal operation	V <sub>DD</sub> = 3.0 V	Square wave input			3.4	mA
							Resonator connection			3.5	mA
			LS (low-speed main) mode (MCSEL = 0)	f <sub>MX</sub> = 8 MHz Note 2, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V	Square wave input		0.9	1.9	mA
							Resonator connection		1.0	2.0	mA
				f <sub>MX</sub> = 8 MHz Note 2, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 2.0 V	Square wave input		0.9	1.9	mA
Resonator connection		1.0					2.0	mA			
LS (low-speed main) mode (MCSEL = 1)	f <sub>MX</sub> = 4 MHz Note 2, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V	Square wave input		0.6	1.1	mA			
				Resonator connection		0.6	1.2	mA			
	f <sub>MX</sub> = 4 MHz Note 2, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 2.0 V	Square wave input		0.6	1.1	mA			
				Resonator connection		0.6	1.2	mA			
LP (low-power main) mode (MCSEL = 1)	f <sub>MX</sub> = 1 MHz Note 2, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 3.0 V	Square wave input		100	190	μA			
				Resonator connection		136	250	μA			
	f <sub>MX</sub> = 1 MHz Note 2, T <sub>A</sub> = -40 to +85°C	Normal operation	V <sub>DD</sub> = 2.0 V	Square wave input		100	190	μA			
				Resonator connection		136	250	μA			

(Notes and Remarks are listed on the next page.)



(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD1	Operating mode	Subsystem clock operation	f <sub>SX</sub> = 32.768 kHz, T <sub>A</sub> = -40°C Note 4	Normal operation	Square wave input		3.2	6.1	μA
						Resonator connection		3.3	6.1	
				f <sub>SX</sub> = 32.768 kHz, T <sub>A</sub> = +25°C Note 4	Normal operation	Square wave input		3.4	6.1	
						Resonator connection		3.6	6.1	
				f <sub>SX</sub> = 32.768 kHz, T <sub>A</sub> = +50°C Note 4	Normal operation	Square wave input		3.5	6.7	
						Resonator connection		3.7	6.7	
				f <sub>SX</sub> = 32.768 kHz, T <sub>A</sub> = +70°C Note 4	Normal operation	Square wave input		3.7	7.5	
						Resonator connection		3.9	7.5	
				f <sub>SX</sub> = 32.768 kHz, T <sub>A</sub> = +85°C Note 4	Normal operation	Square wave input		4.0	8.9	
						Resonator connection		4.2	8.9	
				f <sub>SX</sub> = 32.768 kHz, T <sub>A</sub> = +105°C Note 4	Normal operation	Square wave input		4.5	21.0	
						Resonator connection		4.7	21.1	
f <sub>IL</sub> = 15 kHz, T <sub>A</sub> = -40°C Note 6	Normal operation			1.8	5.9					
f <sub>IL</sub> = 15 kHz, T <sub>A</sub> = +25°C Note 6	Normal operation			1.9	5.9					
f <sub>IL</sub> = 15 kHz, T <sub>A</sub> = +85°C Note 6	Normal operation			2.3	8.7					
f <sub>IL</sub> = 15 kHz, T <sub>A</sub> = +105°C Note 6	Normal operation			3.0	20.9					

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- Note 1.** Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, operational amplifier, comparator, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
- Note 2.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.
- Note 3.** When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.
- Note 4.** When the high-speed system clock, high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped. When ultra-low-power consumption oscillation is set (AMPHS1, AMPHS0) = (1, 0). The values do not include the current flowing into the real-time clock, 12-bit interval timer, and watchdog timer.
- Note 5.** When the high-speed system clock, high-speed on-chip oscillator clock, sub clock, and low-speed on-chip oscillator clock are stopped. The MAX values include the current of peripheral operation except BGO operation, and the STOP leakage current. However, the real time clock, watchdog timer, LVD circuit, and A/D converter are stopped.
- Note 6.** When the high-speed system clock, high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and sub clock are stopped.
- Note 7.** When the high-speed system clock, high-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.
- Remark 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f<sub>IH</sub>: High-speed on-chip oscillator clock frequency (24 MHz max.)
- Remark 3.** f<sub>IM</sub>: Middle-speed on-chip oscillator clock frequency (4 MHz max.)
- Remark 4.** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
- Remark 5.** f<sub>SX</sub>: Sub clock frequency (XT1 clock oscillation frequency)
- Remark 6.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency or low-speed on-chip oscillator clock frequency)
- Remark 7.** Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode	f <sub>IH</sub> = 24 MHz Note 4, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	0.37	1.83	mA
				f <sub>IH</sub> = 24 MHz Note 4, T <sub>A</sub> = +85 to +105°C	V <sub>DD</sub> = 3.0 V		2.85	
				f <sub>IH</sub> = 16 MHz Note 4, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	0.36	1.38	
				f <sub>IH</sub> = 16 MHz Note 4, T <sub>A</sub> = +85 to +105°C	V <sub>DD</sub> = 3.0 V		2.08	
		LS (low-speed main) mode (MCSEL = 0)	f <sub>IH</sub> = 8 MHz Note 4, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	250	710	μA	
				V <sub>DD</sub> = 2.0 V	250	710		
		LS (low-speed main) mode (MCSEL = 1)	f <sub>IH</sub> = 4 MHz Note 4, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	204	400	μA	
				V <sub>DD</sub> = 2.0 V	204	400		
			f <sub>IM</sub> = 4 MHz Note 7, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	40	250		
				V <sub>DD</sub> = 2.0 V	40	250		
		LV (low-voltage main) mode	f <sub>IH</sub> = 3 MHz Note 4, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	425	800	μA	
				V <sub>DD</sub> = 2.0 V	425	800		
		LP (low-power main) mode (MCSEL = 1)	f <sub>IH</sub> = 1 MHz Note 4, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	192	400	μA	
				V <sub>DD</sub> = 2.0 V	192	400		
			f <sub>IM</sub> = 1 MHz Note 7, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	27	100		
				V <sub>DD</sub> = 2.0 V	27	100		
		HS (high-speed main) mode	f <sub>MX</sub> = 20 MHz Note 3, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	Square wave input	0.20	1.55	mA
					Resonator connection	0.40	1.74	
				V <sub>DD</sub> = 3.0 V	Square wave input		2.45	
					Resonator connection		2.57	
				V <sub>DD</sub> = 3.0 V	Square wave input	0.15	0.86	
					Resonator connection	0.30	0.93	
			f <sub>MX</sub> = 10 MHz Note 3, T <sub>A</sub> = +85 to +105°C	V <sub>DD</sub> = 3.0 V	Square wave input		1.28	
					Resonator connection		1.36	
				V <sub>DD</sub> = 3.0 V	Square wave input	68	550	
					Resonator connection	120	590	
				V <sub>DD</sub> = 2.0 V	Square wave input	68	550	
					Resonator connection	120	590	
LS (low-speed main) mode (MCSEL = 0)	f <sub>MX</sub> = 8 MHz Note 3, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	Square wave input	23	128	μA		
			Resonator connection	65	200			
	f <sub>MX</sub> = 4 MHz Note 3, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 2.0 V	Square wave input	23	128			
			Resonator connection	65	200			
LS (low-speed main) mode (MCSEL = 1)	f <sub>MX</sub> = 4 MHz Note 3, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 3.0 V	Square wave input	10	64	μA		
			Resonator connection	48	150			
	f <sub>MX</sub> = 1 MHz Note 3, T <sub>A</sub> = -40 to +85°C	V <sub>DD</sub> = 2.0 V	Square wave input	10	64			
			Resonator connection	48	150			
Subsystem clock operation	fs <sub>X</sub> = 32.768 kHz, T <sub>A</sub> = -40°C Note 5	V <sub>DD</sub> = 3.0 V	Square wave input	0.24	0.57	μA		
			Resonator connection	0.42	0.76			
		V <sub>DD</sub> = 3.0 V	Square wave input	0.30	0.57			
			Resonator connection	0.54	0.76			
		V <sub>DD</sub> = 3.0 V	Square wave input	0.35	1.17			
			Resonator connection	0.60	1.36			
		V <sub>DD</sub> = 3.0 V	Square wave input	0.42	1.97			
			Resonator connection	0.70	2.16			
		V <sub>DD</sub> = 3.0 V	Square wave input	0.80	3.37			
			Resonator connection	0.95	3.56			
		V <sub>DD</sub> = 3.0 V	Square wave input	1.80	17.10			
			Resonator connection	2.20	17.50			
		f <sub>L</sub> = 15 kHz, T <sub>A</sub> = -40°C Note 6	V <sub>DD</sub> = 3.0 V	Square wave input	0.40		1.22	
				Resonator connection	0.47		1.22	
				Square wave input	0.80		3.30	
				Resonator connection	2.00		17.30	

(Notes and Remarks are listed on the next page.)

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- Note 1.** Total current flowing into V<sub>DD</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub> or V<sub>SS</sub>. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, operational amplifier, comparator, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
- Note 2.** When the HALT instruction is executed in the flash memory.
- Note 3.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.
- Note 4.** When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.
- Note 5.** When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and high-speed on-chip oscillator clock are stopped. When RTCLPC = 1 and ultra-low-power consumption oscillation is set (AMPHS1, AMPHS0) = (1, 0). The values include the current flowing into the real-time clock. However, the values do not include the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, high-speed system clock, and sub clock are stopped.
- Note 7.** When the high-speed system clock, high-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.
- Remark 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f<sub>IH</sub>: High-speed on-chip oscillator clock frequency (24 MHz max.)
- Remark 3.** f<sub>IM</sub>: Middle-speed on-chip oscillator clock frequency (4 MHz max.)
- Remark 4.** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
- Remark 5.** f<sub>SX</sub>: Sub clock frequency (XT1 clock oscillation frequency)
- Remark 6.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency or low-speed on-chip oscillator clock frequency)
- Remark 7.** Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

( $T_A = +85$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD3 Note 2	STOP mode Note 3	$T_A = -40^\circ\text{C}$		0.16	0.51	$\mu\text{A}$
			$T_A = +25^\circ\text{C}$		0.22	0.51	
			$T_A = +50^\circ\text{C}$		0.27	1.10	
			$T_A = +70^\circ\text{C}$		0.37	1.90	
			$T_A = +85^\circ\text{C}$		0.60	3.30	
			$T_A = +105^\circ\text{C}$		1.50	17.00	

- <R> **Note 1.** Total current flowing into  $V_{DD}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$  or  $V_{SS}$ . The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, operational amplifier, comparator, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
- Note 2.** The values do not include the current flowing into the real-time clock, 12-bit interval timer, and watchdog timer.
- Note 3.** For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

## Peripheral Functions (Common to all products)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3	fsx = 32.768 kHz			0.02		μA
12-bit interval timer operating current	ITMKA Notes 1, 2, 4	fsx = 32.768 kHz			0.04		μA
8-bit interval timer operating current	ITMT Notes 1, 9	fsx = 32.768 kHz fMAIN stopped (per unit)	8-bit counter mode × 2-channel operation		0.12		μA
			16-bit counter mode operation		0.10		μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fil = 15 kHz			0.22		μA
A/D converter operating current	IADC Notes 6, 10	During maximum-speed conversion	AVDD = 3.0 V		420	720	μA
AVREF(+) current	IAREF Note 11	AVREFP = 3.0 V, ADREFP1 = 0, ADREFP0 = 1			14.0	25.0	μA
Internal reference voltage (1.45 V) current	IADREF Notes 1, 12				85.0		μA
Temperature sensor operating current	ITMPS Note 1				85.0		μA
Comparator operating current	ICMP Notes 8, 10	AVDD = 3.6 V, Regulator output voltage = 2.1 V	Comparator high-speed mode Window mode		12.5		μA
			Comparator low-speed mode Window mode		3.0		
			Comparator high-speed mode Standard mode		6.5		
			Comparator low-speed mode Standard mode		1.7		
		AVDD = 3.6 V, Regulator output voltage = 1.8 V	Comparator high-speed mode Window mode		8.0		
			Comparator low-speed mode Window mode		2.2		
			Comparator high-speed mode Standard mode		4.0		
			Comparator low-speed mode Standard mode		1.3		
Operational amplifier operating current	IAMP Notes 10, 13	Low-power consumption mode	One operational amplifier unit operates Note 14		2.5	4.0	μA
			Two operational amplifier units operate Note 14		4.5	8.0	
			Three operational amplifier units operate Note 14		6.5	11.0	
			Four operational amplifier units operate Note 14		8.5	14.0	
		High-speed mode	One operational amplifier unit operates Note 14		140	220	
			Two operational amplifier units operate Note 14		280	410	
			Three operational amplifier units operate Note 14		420	600	
			Four operational amplifier units operate Note 14		560	780	
LVD operating current	ILVD Notes 1, 7				0.10		μA

(Notes and Remarks are listed on the next page.)

- Note 1.** Current flowing to VDD.
- Note 2.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and high-speed system clock are stopped.
- <R> **Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.
- Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.
- Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is in operation.
- Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter operates in an operation mode or the HALT mode.
- Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
- Note 8.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2, or IDD3 and ICMP when the comparator circuit is in operation.
- Note 9.** Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the 8-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.
- Note 10.** Current flowing to AVDD.
- Note 11.** Current flowing into AVREFP.
- Note 12.** Current consumed by generating the internal reference voltage (1.45 V).
- Note 13.** Current flowing only to the operational amplifier. The current value of the RL78 microcontrollers is the sum of IDD1, IDD2, or IDD3 and IAMP when the operational amplifier is operating in operating mode, HALT mode, or STOP mode.
- Note 14.** The values include the operating current of the operational amplifier reference current circuit.
- Remark 1.** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency
- Remark 2.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 3.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency
- Remark 4.** Temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Self-programming operating current	IFSP Notes 1, 3				2.0	12.20	mA
BGO current	IBGO Notes 1, 2				2.0	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation AVREFF = VDD = 3.0 V TA = -40 to +85°C	The mode is performed Note 5		0.50	0.60	mA
			The A/D conversion operations are performed Note 1		0.60	0.75	mA
			The A/D conversion operations are performed Note 4		420	720	μA
		ADC operation AVREFF = VDD = 3.0 V TA = +85 to +105°C	The mode is performed Note 5		0.50	1.10	mA
			The A/D conversion operations are performed Note 1		0.60	1.34	mA
			The A/D conversion operations are performed Note 4		420	720	μA
		CSI/UART operation	TA = -40 to +85°C		0.70	0.84	mA
			TA = +85 to +105°C		0.70	1.54	mA

**Note 1.** Current flowing to VDD.**Note 2.** Current flowing during programming of the data flash.**Note 3.** Current flowing during self-programming.**Note 4.** Current flowing to AVDD.**Note 5.** For shift time to the SNOOZE mode, see 23.3.3 SNOOZE mode in the RL78/I1D User's Manual.**Remark 1.** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency**Remark 2.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)**Remark 3.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency**Remark 4.** Temperature condition of the TYP. value is TA = 25°C

## 2.4 AC Characteristics

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

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Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V	0.04167		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V PMMC. MCSEL = 0	0.125		1	μs
				1.8 V ≤ VDD ≤ 3.6 V PMMC. MCSEL = 1	0.25		1	μs
			LP (low-power main) mode	1.8 V ≤ VDD ≤ 3.6 V	1			μs
			LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 3.6 V	0.25		1	μs
		1.6 V ≤ VDD < 1.8 V		0.34		1	μs	
		Subsystem clock (fSUB) operation	fsx	1.8 V ≤ VDD ≤ 3.6 V	28.5	30.5	31.3	μs
			fil	1.8 V ≤ VDD ≤ 3.6 V		66.7		μs
		In the self- programming mode	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V	0.04167		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V	0.125		1	μs
LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 3.6 V		0.25		1	μs		
External system clock frequency	fEX	2.7 V ≤ VDD ≤ 3.6 V		1.0		20.0	MHz	
		2.4 V ≤ VDD < 2.7 V		1.0		16.0	MHz	
		1.8 V ≤ VDD < 2.4 V		1		8	MHz	
		1.6 V ≤ VDD < 1.8 V		1		4	MHz	
	fEXS			32		35	kHz	
External system clock input high-level width, low-level width	tEXH, tEXL	2.7 V ≤ VDD ≤ 3.6 V		24			ns	
		2.4 V ≤ VDD < 2.7 V		30			ns	
		1.8 V ≤ VDD < 2.4 V		60			ns	
		1.6 V ≤ VDD < 1.8 V		120			ns	
	tEXHS, tEXLS			13.7			μs	
Ti00 to Ti03 input high-level width, low-level width	tTIH, tTIL			1/fMCK + 10			ns	

**Remark** fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))



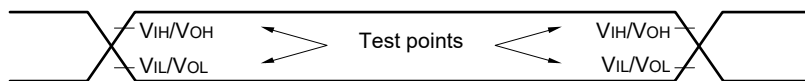
(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

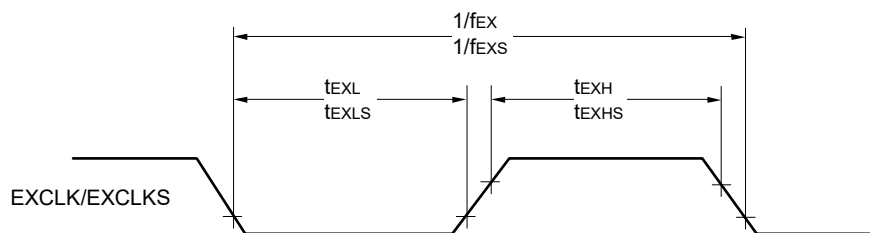
(2/2)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
TO00 to TO03 output frequency	fro	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V			8	MHz
			2.4 V ≤ VDD < 2.7 V			4	
		LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V			4	
		LP (low-power main) mode	1.8 V ≤ VDD ≤ 3.6 V			0.5	
		LV (low-voltage main) mode	1.6 V ≤ VDD ≤ 3.6 V			2	
PCLBUZ0, PCLBUZ1 output frequency	fpCL	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V			8	MHz
			2.4 V ≤ VDD < 2.7 V			4	
		LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V			4	
		LP (low-power main) mode	1.8 V ≤ VDD ≤ 3.6 V			1	
		LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 3.6 V			4	
			1.6 V ≤ VDD < 1.8 V			2	
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0 to INTP6	1.6 V ≤ VDD ≤ 3.6 V	1		μs	
Key interrupt input low-level width	tkR	KR0 to KR3	1.8 V ≤ VDD ≤ 3.6 V	250		ns	
			1.6 V ≤ VDD < 1.8 V	1		μs	
RESET low-level width	trSL			10		μs	

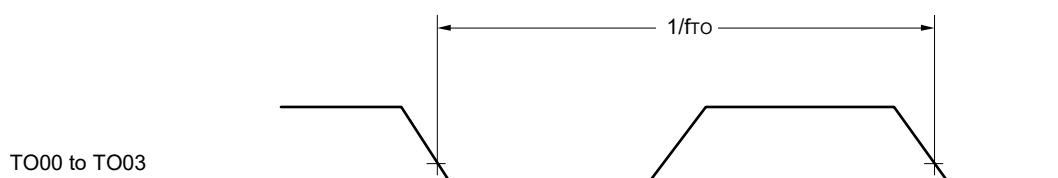
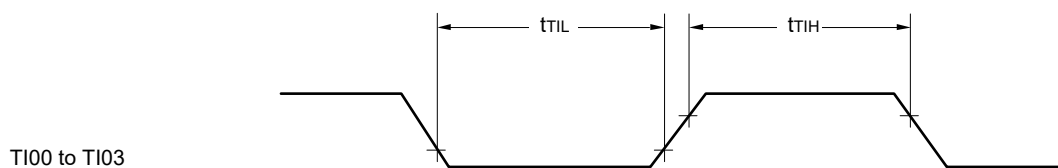
AC Timing Test Points



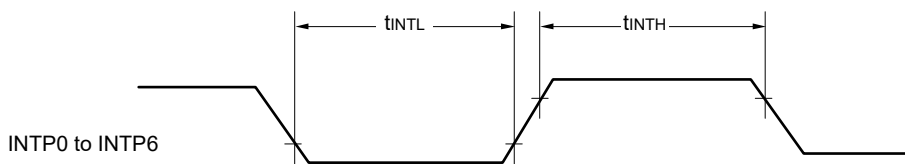
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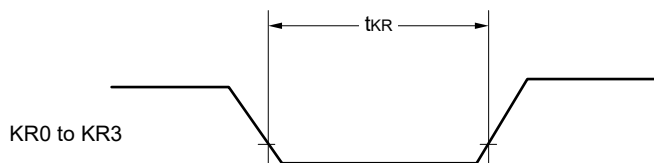
TI/TO Timing



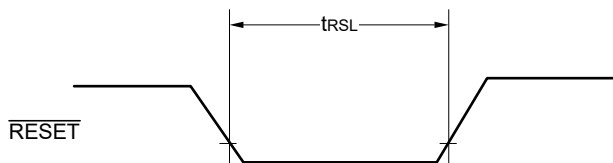
Interrupt Request Input Timing



Key Interrupt Input Timing

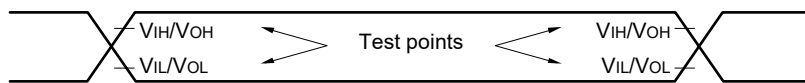


$\overline{\text{RESET}}$  Input Timing



## 2.5 Peripheral Functions Characteristics

AC Timing Test Points



## 2.5.1 Serial array unit

### (1) During communication at same potential (UART mode)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ VDD ≤ 3.6 V		f <sub>MCK</sub> /6		f <sub>MCK</sub> /6		f <sub>MCK</sub> /6		f <sub>MCK</sub> /6	bps
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> Note 2		4.0		1.3		0.1		0.6	Mbps
		1.8 V ≤ VDD ≤ 3.6 V		—		f <sub>MCK</sub> /6		f <sub>MCK</sub> /6		f <sub>MCK</sub> /6	bps
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> Note 2		—		1.3		0.1		0.6	Mbps
		1.7 V ≤ VDD ≤ 3.6 V		—		—		—		f <sub>MCK</sub> /6	bps
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> Note 2		—		—		—		0.6	Mbps
1.6 V ≤ VDD ≤ 3.6 V		—		—		—		—	f <sub>MCK</sub> /6	bps	
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> Note 2		—		—		—		0.6	Mbps

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f<sub>CLK</sub>) are:

HS (high-speed main) mode:	24 MHz (2.7 V ≤ VDD ≤ 3.6 V)
	16 MHz (2.4 V ≤ VDD ≤ 3.6 V)
LS (low-speed main) mode:	8 MHz (1.8 V ≤ VDD ≤ 3.6 V)
LP (low-power main) mode:	1 MHz (1.8 V ≤ VDD ≤ 3.6 V)
LV (low-voltage main) mode:	4 MHz (1.6 V ≤ VDD ≤ 3.6 V)

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ VDD ≤ 3.6 V		f <sub>MCK</sub> /12	bps
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> Note 2		2.0	Mbps

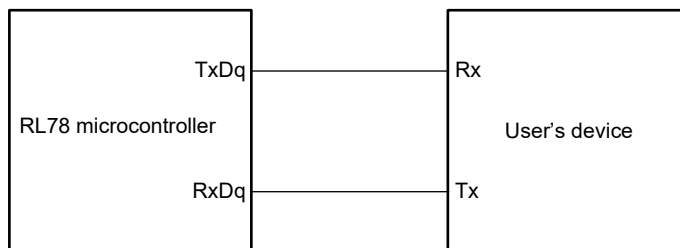
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f<sub>CLK</sub>) are:

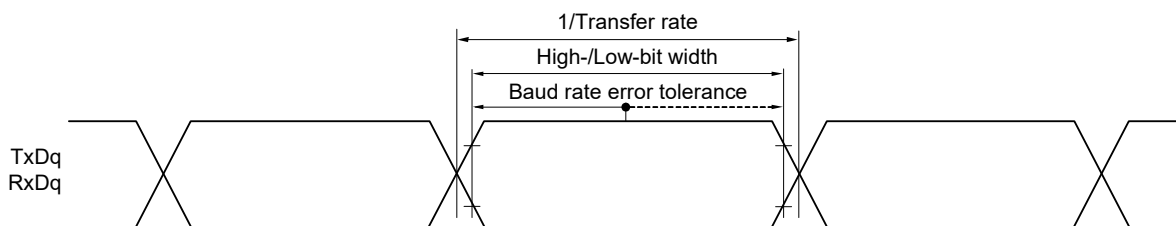
HS (high-speed main) mode:	24 MHz (2.7 V ≤ VDD ≤ 3.6 V)
	16 MHz (2.4 V ≤ VDD ≤ 3.6 V)

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**UART mode connection diagram (during communication at same potential)**



**UART mode bit width (during communication at same potential) (reference)**



**Remark 1.** q: UART number (q = 0), g: PIM and POM number (g = 5)

**Remark 2.** f<sub>MCK</sub>: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(TA = -40 to +85°C, 2.7 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ f <sub>CLK</sub> /2	83.3		250		2000		500		ns
SCKp high-/low-level width	t <sub>KL1</sub>		t <sub>KCY1</sub> /2 - 10		t <sub>KCY1</sub> /2 - 50		t <sub>KCY1</sub> /2 - 50		t <sub>KCY1</sub> /2 - 50		ns
Slp setup time (to SCKp↑) Note 1	t <sub>SIK1</sub>		33		110		110		110		ns
Slp hold time (from SCKp↑) Note 2	t <sub>SI1</sub>		10		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t <sub>KSO1</sub>	C = 20 pF Note 4		10		20		20		20	ns

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

**Remark 2.** f<sub>MCK</sub>: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)****(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ fCLK/4	2.7 V ≤ VDD ≤ 3.6 V	167		500		4000		1000		ns
			2.4 V ≤ VDD ≤ 3.6 V	250								
			1.8 V ≤ VDD ≤ 3.6 V	—								
			1.7 V ≤ VDD ≤ 3.6 V	—		—		—				
			1.6 V ≤ VDD ≤ 3.6 V	—		—		—				
SCKp high-/low-level width	tkH1, tkL1	2.7 V ≤ VDD ≤ 3.6 V	2.7 V ≤ VDD ≤ 3.6 V	tkCY1/2 - 18		tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns
			2.4 V ≤ VDD ≤ 3.6 V	tkCY1/2 - 38								
			1.8 V ≤ VDD ≤ 3.6 V	—								
			1.7 V ≤ VDD ≤ 3.6 V	—		—		—		tkCY1/2 - 100		
			1.6 V ≤ VDD ≤ 3.6 V	—		—		—				
Slp setup time (to SCKp↑) Note 1	tsIK1	2.7 V ≤ VDD ≤ 3.6 V	2.7 V ≤ VDD ≤ 3.6 V	58		110		110		110		ns
			2.4 V ≤ VDD ≤ 3.6 V	75								
			1.8 V ≤ VDD ≤ 3.6 V	—								
			1.7 V ≤ VDD ≤ 3.6 V	—		—		—		220		
			1.6 V ≤ VDD ≤ 3.6 V	—		—		—				
Slp hold time (from SCKp↑) Note 2	tkSI1	2.4 V ≤ VDD ≤ 3.6 V	2.4 V ≤ VDD ≤ 3.6 V	19		19		19		19		ns
			1.8 V ≤ VDD ≤ 3.6 V	—								
			1.6 V ≤ VDD ≤ 3.6 V	—		—		—				
Delay time from SCKp↓ to SOp output Note 3	tkSO1	C = 30 pF Note 4	2.4 V ≤ VDD ≤ 3.6 V		33.4		33.4		33.4		33.4	ns
			1.8 V ≤ VDD ≤ 3.6 V		—		—		—			
			1.6 V ≤ VDD ≤ 3.6 V		—		—		—			

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

**Remark 2.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))



**(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)****(TA = +85 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ fCLK/4 2.7 V ≤ VDD ≤ 3.6 V	250		ns
			500		ns
SCKp high-/low-level width	tkH1, tkL1	2.7 V ≤ VDD ≤ 3.6 V	tkCY1/2 - 36		ns
		2.4 V ≤ VDD ≤ 3.6 V	tkCY1/2 - 76		ns
Slp setup time (to SCKp↑) Note 1	tSIK1	2.7 V ≤ VDD ≤ 3.6 V	66		ns
		2.4 V ≤ VDD ≤ 3.6 V	133		ns
Slp hold time (from SCKp↑) Note 2	tkSI1		38		ns
Delay time from SCKp↓ to SOp output Note 3	tkSO1	C = 30 pF Note 4		50	ns

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

**Remark 2.** fMCK: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	tkcy2	2.7 V ≤ VDD ≤ 3.6 V	fMCK > 16 MHz	8/fMCK	—	—	—	—	—	—	ns	
			fMCK ≤ 16 MHz	6/fMCK	6/fMCK	6/fMCK	6/fMCK	6/fMCK				
		2.4 V ≤ VDD ≤ 3.6 V		6/fMCK and 500	6/fMCK	6/fMCK	6/fMCK	6/fMCK	6/fMCK			
		1.8 V ≤ VDD ≤ 3.6 V		—	6/fMCK	6/fMCK	6/fMCK	6/fMCK				
		1.7 V ≤ VDD ≤ 3.6 V		—	—	—	—	—				
		1.6 V ≤ VDD ≤ 3.6 V		—	—	—	—	—				
SCKp high-/low-level width	tkH2, tkL2	2.7 V ≤ VDD ≤ 3.6 V		tkcy2/2 - 8	tkcy2/2 - 8	tkcy2/2 - 8	tkcy2/2 - 8	tkcy2/2 - 8	tkcy2/2 - 8	ns		
		2.4 V ≤ VDD ≤ 3.6 V		tkcy2/2 - 18	tkcy2/2 - 18	tkcy2/2 - 18	tkcy2/2 - 18	tkcy2/2 - 18				
		1.8 V ≤ VDD ≤ 3.6 V		—	—	—	—	—				
		1.7 V ≤ VDD ≤ 3.6 V		—	—	—	—	tkcy2/2 - 66				
		1.6 V ≤ VDD ≤ 3.6 V		—	—	—	—	—				
Slp setup time (to SCKp↓) Note 1	tsik2	2.7 V ≤ VDD ≤ 3.6 V		1/fMCK + 20	1/fMCK + 30	1/fMCK + 30	1/fMCK + 30	1/fMCK + 30	ns			
		2.4 V ≤ VDD ≤ 3.6 V		1/fMCK + 30	—	—	—	—				
		1.8 V ≤ VDD ≤ 3.6 V		—	—	—	—	—				
		1.7 V ≤ VDD ≤ 3.6 V		—	—	—	—	1/fMCK + 40				
		1.6 V ≤ VDD ≤ 3.6 V		—	—	—	—	—				
Slp hold time (from SCKp↑) Note 2	tkSiz	2.4 V ≤ VDD ≤ 3.6 V		1/fMCK + 31	1/fMCK + 31	1/fMCK + 31	1/fMCK + 31	1/fMCK + 31	ns			
		1.8 V ≤ VDD ≤ 3.6 V		—	—	—	—	—				
		1.7 V ≤ VDD ≤ 3.6 V		—	—	—	—	1/fMCK + 250				
		1.6 V ≤ VDD ≤ 3.6 V		—	—	—	—	—				
Delay time from SCKp↓ to SOp output Note 3	tkSO2	C = 30 pF Note 4	2.7 V ≤ VDD ≤ 3.6 V	2/fMCK + 44	2/fMCK + 110	2/fMCK + 110	2/fMCK + 110	2/fMCK + 110	ns			
			2.4 V ≤ VDD ≤ 3.6 V	2/fMCK + 75	—	—	—	—				
			1.8 V ≤ VDD ≤ 3.6 V	—	—	—	—	—				
			1.7 V ≤ VDD ≤ 3.6 V	—	—	—	—	2/fMCK + 220				
			1.6 V ≤ VDD ≤ 3.6 V	—	—	—	—	—				

- Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** C is the load capacitance of the SOp output lines.
- Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

**Remark 2.** fMCK: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

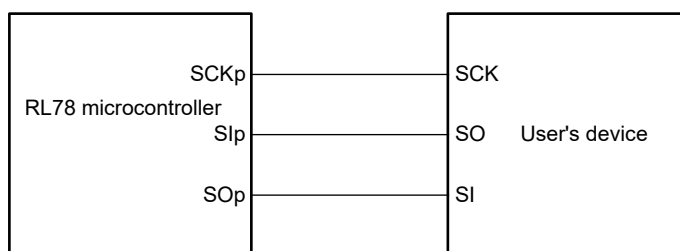
(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SSi00 setup time	tssik	DAPmn = 0	2.7 V ≤ VDD ≤ 3.6 V	120		120		120		120	ns
			2.4 V ≤ VDD < 2.7 V	200		200		200		200	
			1.8 V ≤ VDD < 2.4 V	—		—		—		—	
			1.6 V ≤ VDD < 1.8 V	—		—		—		400	
		DAPmn = 1	2.7 V ≤ VDD ≤ 3.6 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			2.4 V ≤ VDD < 2.7 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	
			1.8 V ≤ VDD < 2.4 V	—		—		—		—	
			1.6 V ≤ VDD < 1.8 V	—		—		—		1/fMCK + 400	
SSi00 hold time	tkssi	DAPmn = 0	2.7 V ≤ VDD ≤ 3.6 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			2.4 V ≤ VDD < 2.7 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	
			1.8 V ≤ VDD < 2.4 V	—		—		—		—	
			1.6 V ≤ VDD < 1.8 V	—		—		—		1/fMCK + 400	
		DAPmn = 1	2.7 V ≤ VDD ≤ 3.6 V	120		120		120		120	ns
			2.4 V ≤ VDD < 2.7 V	200		200		200		200	
			1.8 V ≤ VDD < 2.4 V	—		—		—		—	
			1.6 V ≤ VDD < 1.8 V	—		—		—		400	

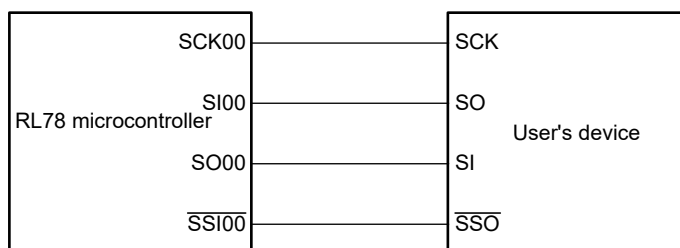
**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

**CSI mode connection diagram (during communication at same potential)**



**CSI mode connection diagram (during communication at same potential)  
(Slave Transmission of slave select input function (CSI00))**



**Remark 1.** p: CSI number (p = 00, 01)

**Remark 2.** m: Unit number, n: Channel number (mn = 00, 01)

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)****(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit	
			MIN.	MAX.		
SCKp cycle time Note 5	tkcy2	2.7 V ≤ VDD < 3.6 V	fMCK > 16 MHz	16/fMCK	ns	
			fMCK ≤ 16 MHz	12/fMCK	ns	
		2.4 V ≤ VDD < 2.7 V	12/fMCK and 1000	ns		
SCKp high-/low-level width	tkH2, tkL2	2.7 V ≤ VDD ≤ 3.6 V	tkcy2/2 - 16		ns	
		2.4 V ≤ VDD < 2.7 V	tkcy2/2 - 36		ns	
Slp setup time (to SCKp↑) Note 1	tsIK2	2.7 V ≤ VDD ≤ 3.6 V	1/fMCK + 40		ns	
		2.4 V ≤ VDD < 2.7 V	1/fMCK + 60		ns	
Slp hold time (from SCKp↑) Note 2	tkS12		1/fMCK + 62		ns	
Delay time from SCKp↓ to SOp output Note 3	tkSO2	C = 30 pF Note 4	2.7 V ≤ VDD ≤ 3.6 V		2/fMCK + 66	ns
			2.4 V ≤ VDD < 2.7 V		2/fMCK + 113	ns

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

**Remark 2.** fMCK: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

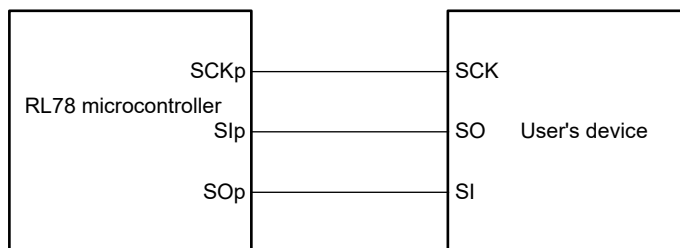
(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit	
			MIN.	MAX.		
SSI00 setup time	tssik	DAPmn = 0	2.7 V ≤ VDD ≤ 3.6 V	240		ns
			2.4 V ≤ VDD < 2.7 V	400		ns
		DAPmn = 1	2.7 V ≤ VDD ≤ 3.6 V	1/fMCK + 240		ns
			2.4 V ≤ VDD < 2.7 V	1/fMCK + 400		ns
SSI00 hold time	tkssi	DAPmn = 0	2.7 V ≤ VDD ≤ 3.6 V	1/fMCK + 240		ns
			2.4 V ≤ VDD < 2.7 V	1/fMCK + 400		ns
		DAPmn = 1	2.7 V ≤ VDD ≤ 3.6 V	240		ns
			2.4 V ≤ VDD < 2.7 V	400		ns

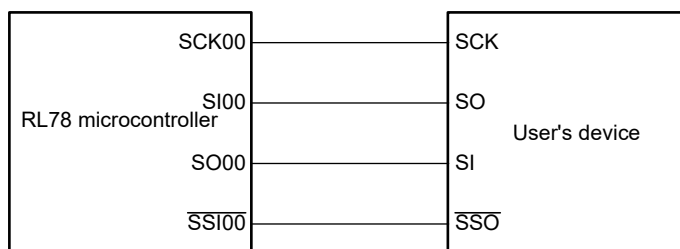
**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

CSI mode connection diagram (during communication at same potential)



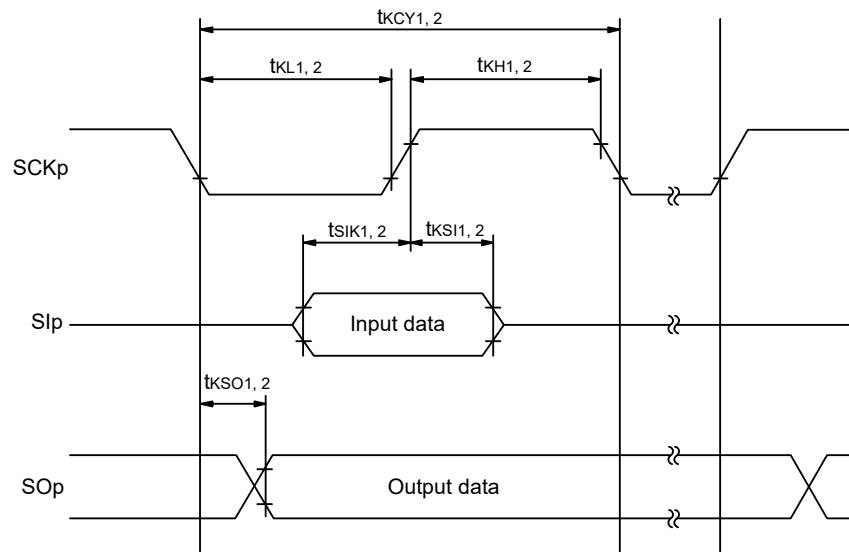
CSI mode connection diagram (during communication at same potential)  
(Slave Transmission of slave select input function (CSI00))



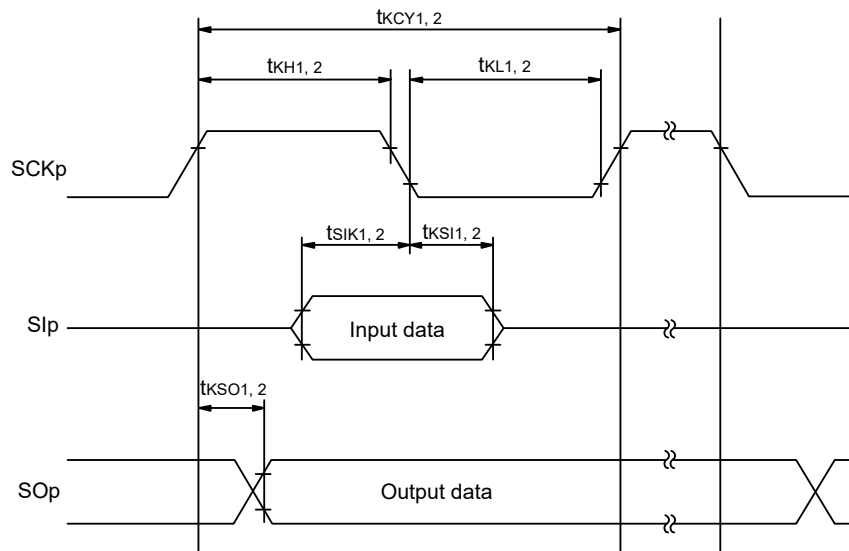
**Remark 1.** p: CSI number (p = 00, 01)

**Remark 2.** m: Unit number, n: Channel number (mn = 00, 01)

**CSI mode serial transfer timing (during communication at same potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark 1.** p: CSI number (p = 00, 01)

**Remark 2.** m: Unit number, n: Channel number (mn = 00, 01)

(5) During communication at same potential (simplified I<sup>2</sup>C mode)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCLr clock frequency	f <sub>SCL</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ		1000 Note 1		400 Note 1		250 Note 1		400 Note 1	kHz	
		1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ		—								
		1.8 V ≤ V <sub>DD</sub> < 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ		—		300 Note 1		250 Note 1		300 Note 1		
		1.7 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ		—		—		—		250 Note 1		
		1.6 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ		—		—		—		—		
Hold time when SCLr = "L"	t <sub>LOW</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475			1150		1150		1150	ns	
		1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	—									
		1.8 V ≤ V <sub>DD</sub> < 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		1550		1550		1550			
		1.7 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		—		—		1850			
		1.6 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		—		—		—			
Hold time when SCLr = "H"	t <sub>HIGH</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475			1150		1150		1150	ns	
		1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	—									
		1.8 V ≤ V <sub>DD</sub> < 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		1550		1550		1550			
		1.7 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		—		—		1850			
		1.6 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		—		—		—			
Data setup time (reception)	t <sub>SU: DAT</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 85 Note 2			1/f <sub>MCK</sub> + 145 Note 2		1/f <sub>MCK</sub> + 145 Note 2		1/f <sub>MCK</sub> + 145 Note 2	ns	
		1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	—									
		1.8 V ≤ V <sub>DD</sub> < 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		1/f <sub>MCK</sub> + 230 Note 2		1/f <sub>MCK</sub> + 230 Note 2		1/f <sub>MCK</sub> + 230 Note 2			
		1.7 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		—		—		1/f <sub>MCK</sub> + 290 Note 2			
		1.6 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—		—		—		—			
Data hold time (transmission)	t <sub>HD: DAT</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305		0	305	0	305	0	305	ns
		1.8 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	—	—			355		355		355	
		1.8 V ≤ V <sub>DD</sub> < 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—	—			—		—		—	
		1.7 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—	—			—		—		405	
		1.6 V ≤ V <sub>DD</sub> < 1.8 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ	—	—			—		—		—	

(Notes and Caution are listed on the next page.)

**Note 1.** The value must also be equal to or less than  $f_{MCK}/4$ .

**Note 2.** Set the  $f_{MCK}$  value to keep the hold time of  $SCLr = "L"$  and  $SCLr = "H"$ .

**Caution** Select the normal input buffer and the N-ch open drain output ( $V_{DD}$  tolerance) mode for the  $SDAr$  pin and the normal output mode for the  $SCLr$  pin by using port input mode register g (PIMg) and port output mode register h (POMh).



**(5) During communication at same potential (simplified I<sup>2</sup>C mode)****(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

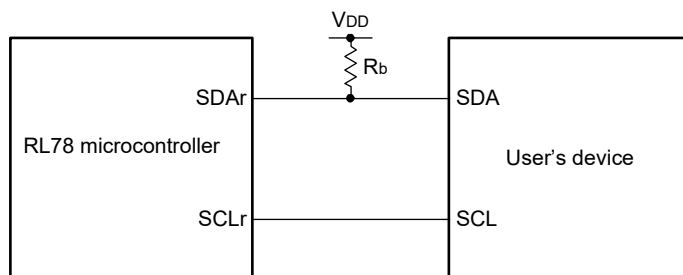
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f <sub>SCL</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1200		ns
		2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1200		ns
		2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	4600		ns
Data setup time (reception)	t <sub>SU: DAT</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 220 Note 2		ns
		2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	1/f <sub>MCK</sub> + 580 Note 2		ns
Data hold time (transmission)	t <sub>HD: DAT</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	770	ns
		2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ	0	1420	ns

**Note 1.** The value must also be equal to or less than f<sub>MCK</sub>/4.

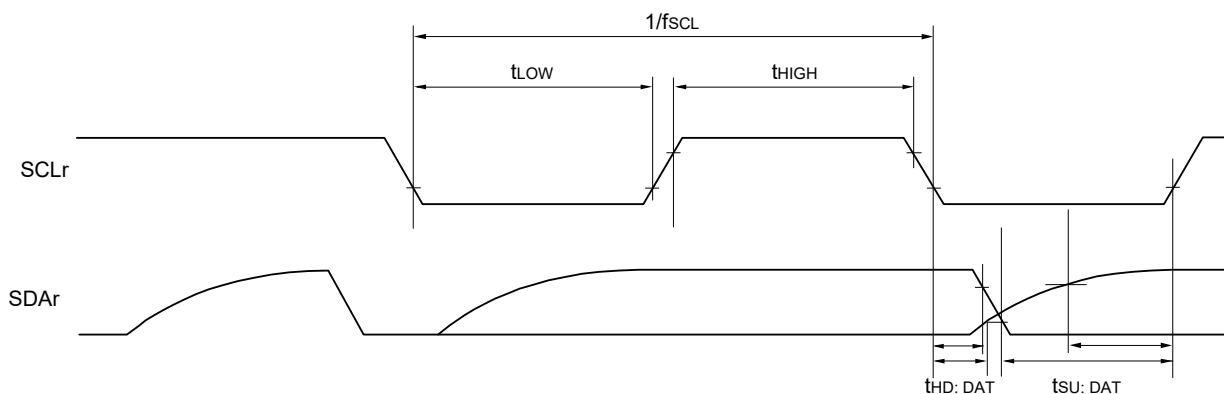
**Note 2.** Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the normal input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

**Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)**



**Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)**



- Remark 1.**  $R_b[\Omega]$ : Communication line (SDAr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance
- Remark 2.** r: IIC number (r = 00, 01), g: PIM number (g = 5), h: POM number (h = 5)
- Remark 3.**  $f_{mck}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

**(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output)****(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.				
Transfer rate Notes 1, 2		reception	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V			fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1		bps		
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 3			4.0		1.3		0.1		0.6	Mbps	
			1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V			fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2		bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 3			4.0		1.3		0.1		0.6	Mbps	

**Note 1.** Transfer rate in the SNOOZE mode is 4,800 bps only.

**Note 2.** Use it with VDD ≥ Vb.

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 3.6 V)  
16 MHz (2.4 V ≤ VDD ≤ 3.6 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 3.6 V)

LP (low-power main) mode: 1 MHz (1.8 V ≤ VDD ≤ 3.6 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 3.6 V)

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

**Remark 1.** Vb[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0), g: PIM and POM number (g = 5)

**Remark 3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
n: Channel number (mn = 00, 01)

**(6) Communication at different potential (1.8 V, 2.5V) (UART mode) (dedicated baud rate generator output)****(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Transfer rate Note 2		Transmission	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V			Note 1		Note 1		Note 1	Note 1	bps	
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V			1.2 Note 2		1.2 Note 2		1.2 Note 2		1.2 Note 2	Mbps
			1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V			Notes 3, 4		Notes 3, 4		Notes 3, 4		Notes 3, 4	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V			0.43 Note 5		0.43 Note 5		0.43 Note 5		0.43 Note 5	Mbps

**Note 1.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  and  $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}} \times 3 \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 2.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** Use it with  $V_{DD} \geq V_b$ .

**Note 4.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}} \times 3 \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 [\%]$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 5.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

**(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output)****(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit	
			MIN.	MAX.		
Transfer rate Notes 1, 2		Reception	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V		fMCK/12 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		2.0	Mbps
			2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		fMCK/12 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		0.66	Mbps

**Note 1.** Transfer rate in the SNOOZE mode is 4,800 bps only.

**Note 2.** Use it with VDD ≥ Vb.

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:  
 HS (high-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 3.6 V)  
 16 MHz (2.4 V ≤ VDD ≤ 3.6 V)

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

**Remark 1.** Vb[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0), g: PIM and POM numbers (g = 5)

**Remark 3.** fMCK: Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
 n: Channel number (mn = 00, 01))

**(6) Communication at different potential (1.8 V, 2.5V) (UART mode) (dedicated baud rate generator output)****(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit	
			MIN.	MAX.		
Transfer rate <sup>Note 2</sup>		Transmission	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V		Note 1	bps
			Theoretical value of the maximum transfer rate C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ, V <sub>b</sub> = 2.3 V		1.2 <sup>Note 2</sup>	Mbps
			2.4 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V		Notes 3, 4	bps
			Theoretical value of the maximum transfer rate C <sub>b</sub> = 50 pF, R <sub>b</sub> = 5.5 kΩ, V <sub>b</sub> = 1.6 V		0.43 <sup>Note 5</sup>	Mbps

**Note 1.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$  and  $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 2.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** Use it with  $V_{DD} \geq V_b$ .

**Note 4.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

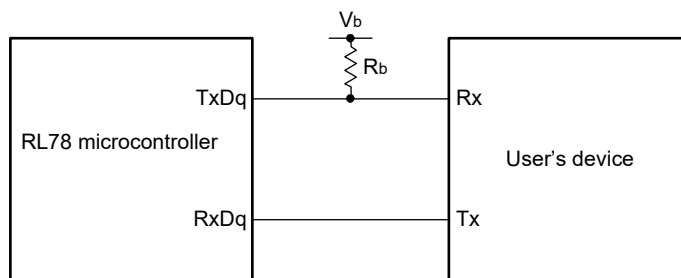
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides

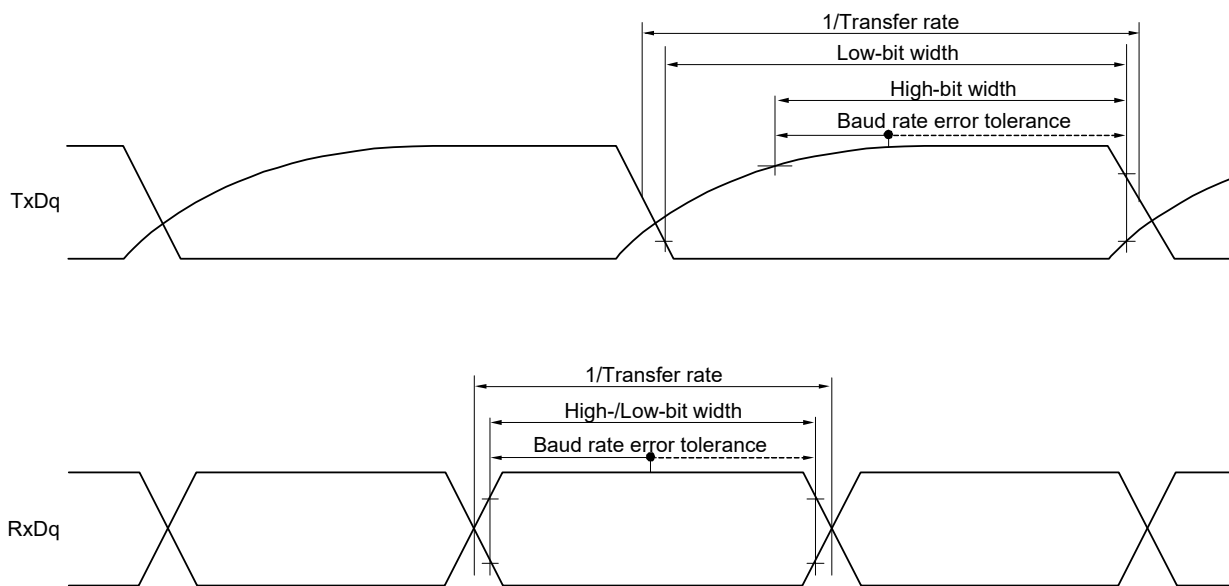
**Note 5.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V<sub>DD</sub> tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

**UART mode connection diagram (during communication at different potential)**



**UART mode bit width (during communication at different potential) (reference)**



- Remark 1.**  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  $C_b[F]$ : Communication line (TxDq) load capacitance,  $V_b[V]$ : Communication line voltage
- Remark 2.** q: UART number (q = 0), g: PIM and POM number (g = 5)
- Remark 3.**  $f_{mck}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**(7) Communication at different potential (2.5 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**

**(TA = -40 to +85°C, 2.7 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ fCLK/2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	300		1500		1500		1500		ns
SCKp high-level width	tkH1		2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 120		tkCY1/2 - 120		tkCY1/2 - 120		tkCY1/2 - 120		ns
SCKp low-level width	tkL1		2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 10		tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑) <i>Note 1</i>	tsIK1		2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	121		479		479		479		ns
Slp hold time (from SCKp↑) <i>Note 1</i>	tkSI1		2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		10		ns
Delay time from SCKp↓ to SOp output <i>Note 1</i>	tkSO1		2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		130		130		130		130	ns
Slp setup time (to SCKp↓) <i>Note 2</i>	tsIK1		2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	33		110		110		110		ns
Slp hold time (from SCKp↓) <i>Note 2</i>	tkSI1		2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		10		ns
Delay time from SCKp↑ to SOp output <i>Note 2</i>	tkSO1		2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		10		10		10		10	ns

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

**Remark 1.** Rb[i]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 5)

**Remark 3.** fмск: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))



**(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)****(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCKp cycle time	tkCY1	tkCY1 ≥ fCLK/4	2.7V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		500		1150		1150		1150	ns
			1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note, Cb = 30 pF, Rb = 5.5 kΩ		1150		1150		1150		1150	ns
SCKp high-level width	tkH1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		tkCY1/2 - 170		tkCY1/2 - 170		tkCY1/2 - 170		tkCY1/2 - 170	ns	
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note, Cb = 30 pF, Rb = 5.5 kΩ		tkCY1/2 - 458		tkCY1/2 - 458		tkCY1/2 - 458		tkCY1/2 - 458	ns	
SCKp low-level width	tkL1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		tkCY1/2 - 18		tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50	ns	
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note, Cb = 30 pF, Rb = 5.5 kΩ		tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50	ns	

**Note** Use it with VDD ≥ Vb.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)****(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, Vss = AVss = 0 V)****(2/2)**

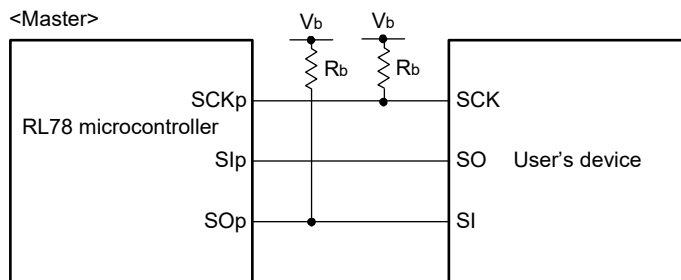
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	tsIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		479		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		479		ns
Slp hold time (from SCKp↓) Note 1	tkSH1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		19		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tkSO1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195		195	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		483		483		483		483	ns
Slp setup time (to SCKp↓) Note 2	tsIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		110		110		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		110		ns
Slp hold time (from SCKp↓) Note 2	tkSH1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		19		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		19		ns
Delay time from SCKp↑ to SOp output Note 2	tkSO1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25		25	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		25		25		25		25	ns

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 3.** Use it with VDD ≥ Vb.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

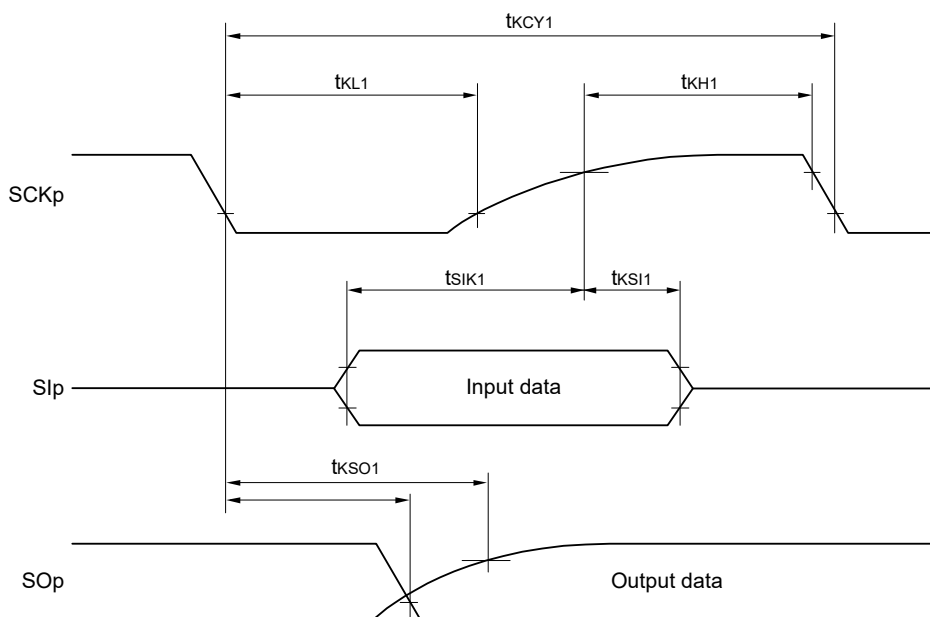
(Remarks are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

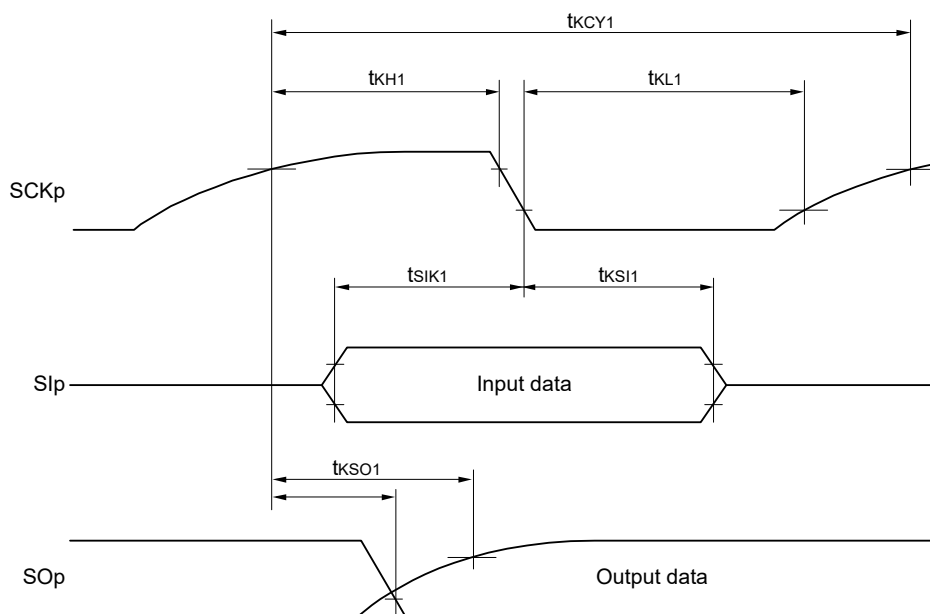


- Remark 1.**  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[F]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[V]$ : Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)
- Remark 3.**  $f_{mck}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

**(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)****(TA = +85 to 105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ fCLK/4 2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	1000		ns
			2300		ns
SCKp high-level width	tkH1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 340		ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 916		ns
SCKp low-level width	tkL1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 36		ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 100		ns

**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)****(TA = +85 to 105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(2/2)**

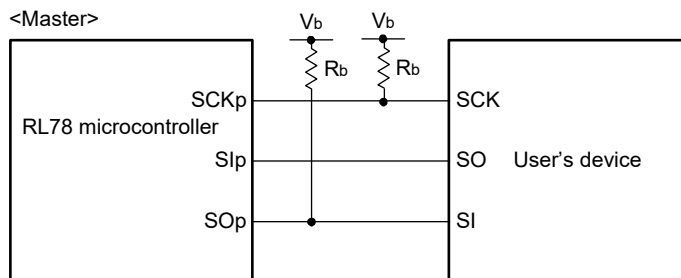
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↑) <sup>Note 1</sup>	tSIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	354		ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 3</sup> , Cb = 30 pF, Rb = 5.5 kΩ	958		ns
Slp hold time (from SCKp↑) <sup>Note 1</sup>	tKS11	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	38		ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 3</sup> , Cb = 30 pF, Rb = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output <sup>Note 1</sup>	tKS01	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		390	ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 3</sup> , Cb = 30 pF, Rb = 5.5 kΩ		966	ns
Slp setup time (to SCKp↓) <sup>Note 2</sup>	tSIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	88		ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 3</sup> , Cb = 30 pF, Rb = 5.5 kΩ	220		ns
Slp hold time (from SCKp↓) <sup>Note 2</sup>	tKS11	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	38		ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 3</sup> , Cb = 30 pF, Rb = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output <sup>Note 2</sup>	tKS01	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		50	ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 3</sup> , Cb = 30 pF, Rb = 5.5 kΩ		50	ns

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 3.** Use it with VDD ≥ Vb.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

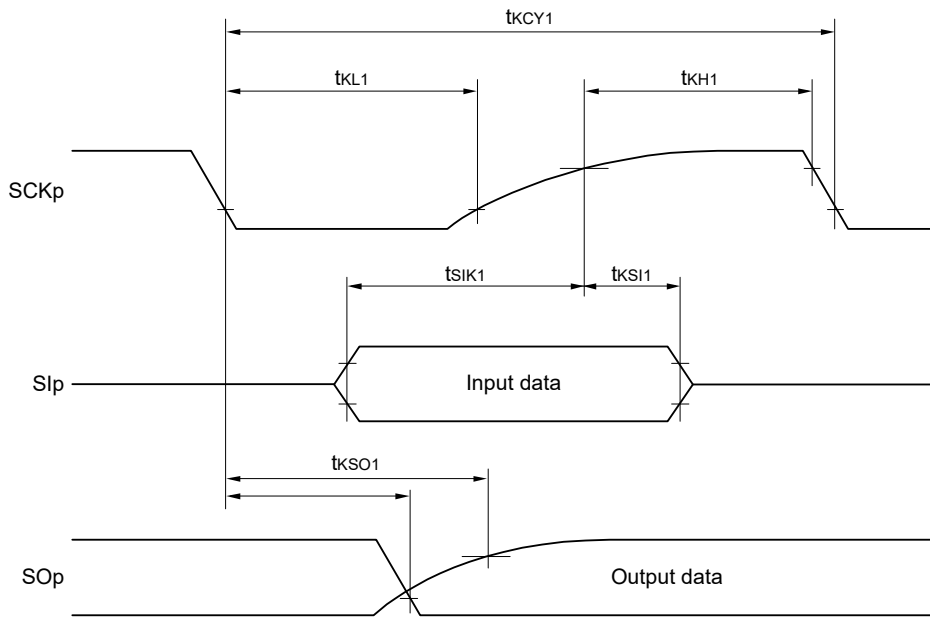


**Remark 1.**  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[F]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[V]$ : Communication line voltage

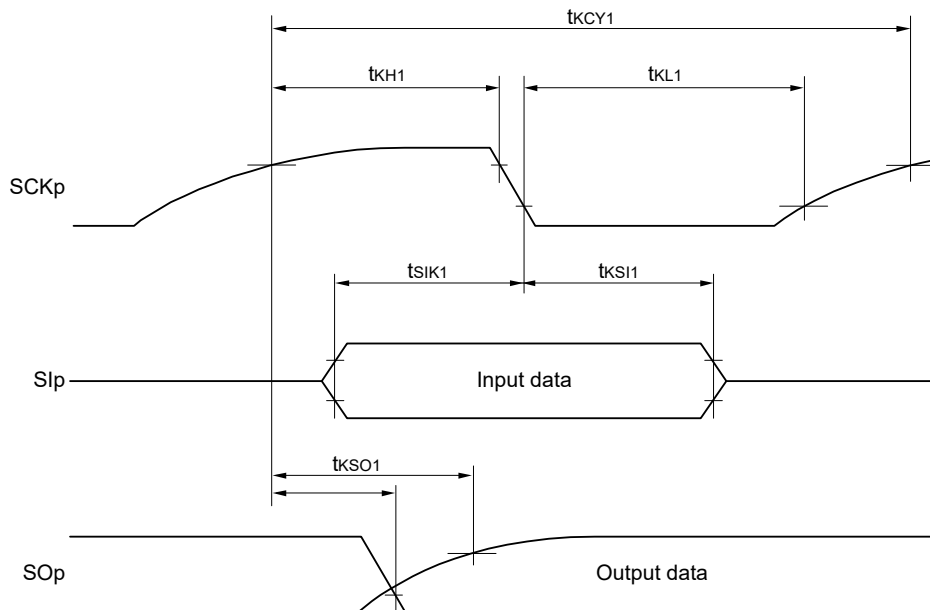
**Remark 2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

**Remark 3.**  $f_{mck}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)  
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)



**(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)**

**(TA = -40 to 85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

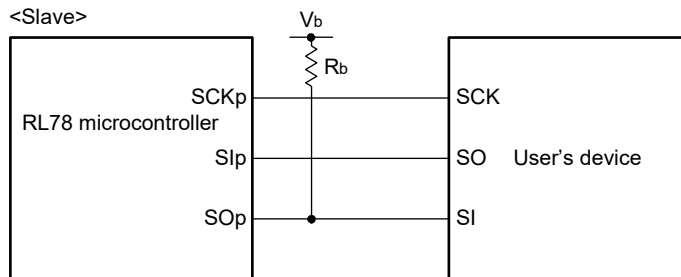
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCKp cycle time Note 1	tkcy2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V	20 MHz < fMCK ≤ 24 MHz	16/fMCK		—		—		—		ns
			16 MHz < fMCK ≤ 20 MHz	14/fMCK		—		—		—		ns
			8 MHz < fMCK ≤ 16 MHz	12/fMCK		—		—		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		16/fMCK		—		—		ns
			fMCK ≤ 4 MHz	6/fMCK		10/fMCK		10/fMCK		10/fMCK		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	20 MHz < fMCK ≤ 24 MHz	36/fMCK		—		—		—		ns
			16 MHz < fMCK ≤ 20 MHz	32/fMCK		—		—		—		ns
			8 MHz < fMCK ≤ 16 MHz	26/fMCK		—		—		—		ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK		16/fMCK		—		—		ns
			fMCK ≤ 4 MHz	10/fMCK		10/fMCK		10/fMCK		10/fMCK		ns
SCKp high-/low-level width	tkH2, tkL2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V	tkcy2/2 - 18		tkcy2/2 - 50		tkcy2/2 - 50		tkcy2/2 - 50		ns	
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	tkcy2/2 - 50		tkcy2/2 - 50		tkcy2/2 - 50		tkcy2/2 - 50		ns	
Slp setup time (to SCKp↑) Note 3	tsik2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V	1/fMCK + 20		1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		ns	
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		ns	
Slp hold time (from SCKp↑) Note 4	tkS12		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns	
Delay time from SCKp↓ to SOp output Note 5	tkSO2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		2/fMCK + 214		2/fMCK + 573		2/fMCK + 573		2/fMCK + 573	ns	
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ		2/fMCK + 573		2/fMCK + 573		2/fMCK + 573		2/fMCK + 573	ns	

(Notes and Caution are listed on the next page. Remarks are listed on the page after the next page.)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with  $V_{DD} \geq V_b$ .
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution** **Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output ( $V_{DD}$  tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.**

(Remarks are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

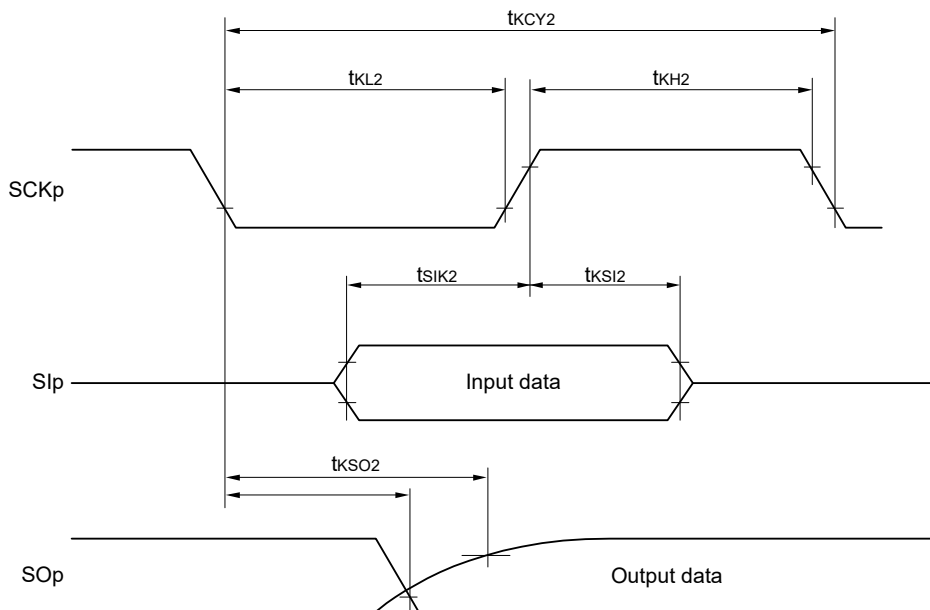


**Remark 1.**  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[F]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[V]$ : Communication line voltage

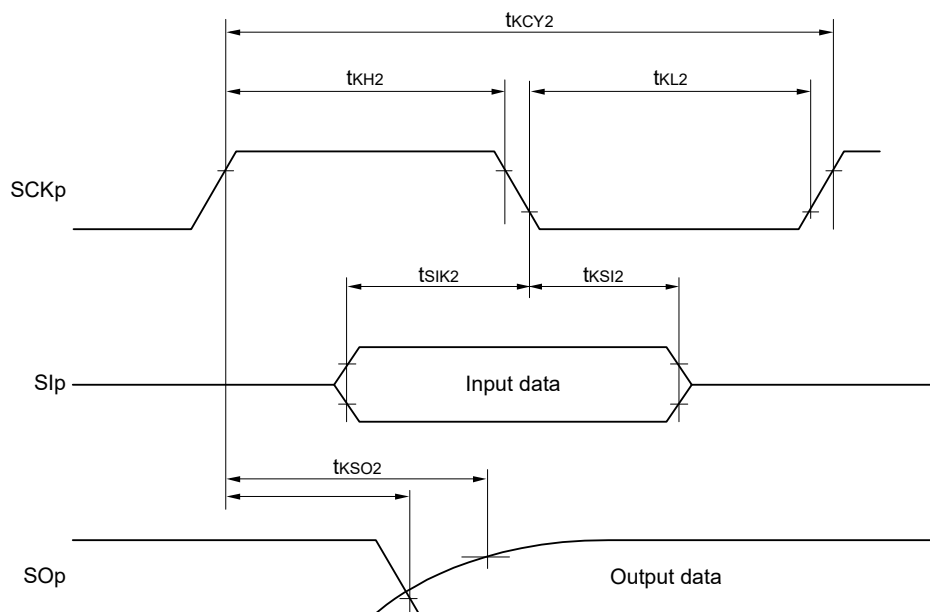
**Remark 2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

**Remark 3.**  $f_{MCK}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

**(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)****(TA = +85 to 105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

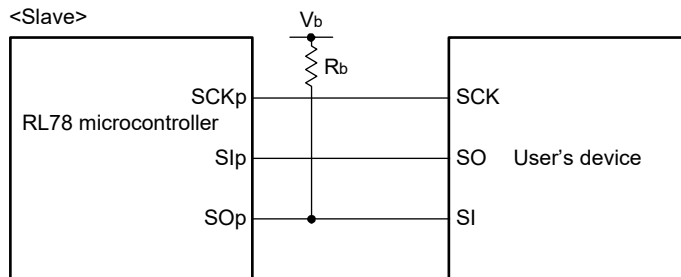
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit	
			MIN.	MAX.		
SCKp cycle time <sup>Note 1</sup>	tkCY2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V	20 MHz < fMCK ≤ 24 MHz	32/fMCK		ns
			16 MHz < fMCK ≤ 20 MHz	28/fMCK		ns
			8 MHz < fMCK ≤ 16 MHz	24/fMCK		ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK		ns
			fMCK ≤ 4 MHz	12/fMCK		ns
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup>	20 MHz < fMCK ≤ 24 MHz	72/fMCK		ns
			16 MHz < fMCK ≤ 20 MHz	64/fMCK		ns
			8 MHz < fMCK ≤ 16 MHz	52/fMCK		ns
			4 MHz < fMCK ≤ 8 MHz	32/fMCK		ns
			fMCK ≤ 4 MHz	20/fMCK		ns
SCKp high-/low-level width	tkH2, tkL2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V	tkCY2/2 - 36		ns	
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup>	tkCY2/2 - 100		ns	
Slp setup time (to SCKp↑) <sup>Note 3</sup>	tsIK2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V	1/fMCK + 40		ns	
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup>	1/fMCK + 60		ns	
Slp hold time (from SCKp↑) <sup>Note 4</sup>	tkSI2		1/fMCK + 62		ns	
Delay time from SCKp↓ to SOp output <sup>Note 5</sup>	tkSO2	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V Cb = 30 pF, Rb = 2.7 kΩ		2/fMCK + 428	ns	
		2.4 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> Cb = 30 pF, Rb = 5.5 kΩ		2/fMCK + 1146	ns	

(Notes and Caution are listed on the next page. Remarks are listed on the page after the next page.)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with  $V_{DD} \geq V_b$ .
- Note 3.** When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The  $Slp$  setup time becomes "to  $SCKp\downarrow$ " when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
- Note 4.** When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The  $Slp$  hold time becomes "from  $SCKp\downarrow$ " when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
- Note 5.** When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The delay time to  $SOp$  output becomes "from  $SCKp\uparrow$ " when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
- Caution** **Select the TTL input buffer for the  $Slp$  pin and  $SCKp$  pin and the N-ch open drain output ( $V_{DD}$  tolerance) mode for the  $SOp$  pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.**

(Remarks are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**

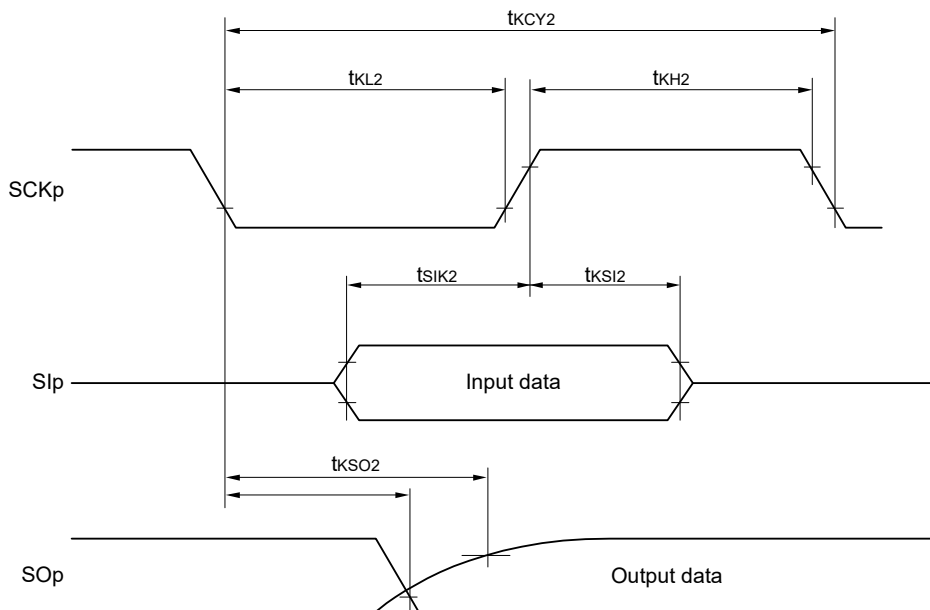


**Remark 1.** R<sub>b</sub>[Ω]: Communication line (SO<sub>p</sub>) pull-up resistance, C<sub>b</sub>[F]: Communication line (SO<sub>p</sub>) load capacitance, V<sub>b</sub>[V]: Communication line voltage

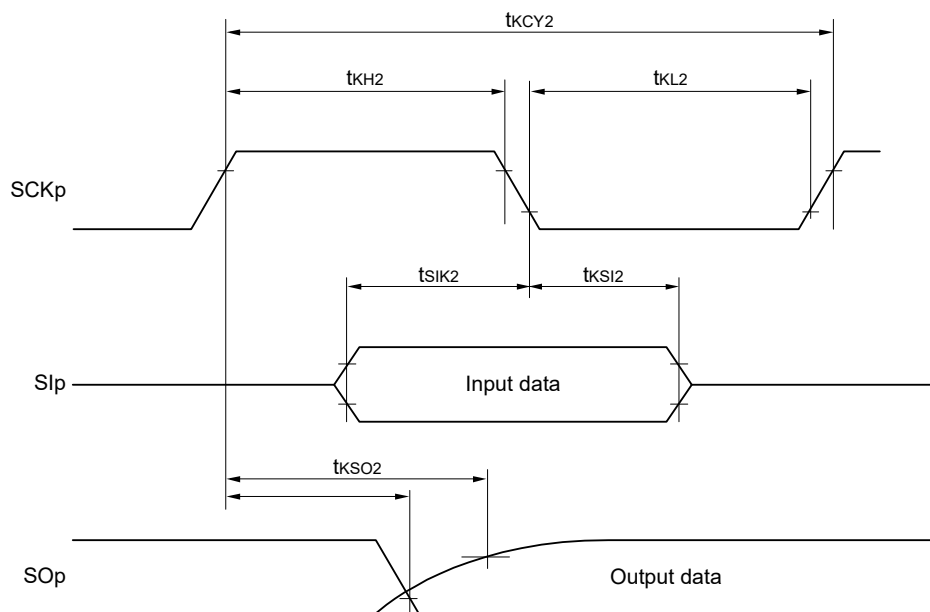
**Remark 2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

**Remark 3.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



**Remark** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)



**(10) Communication at different potential (1.8 V, 2.5 V) (simplified I<sup>2</sup>C mode)****(TA = -40 to 85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

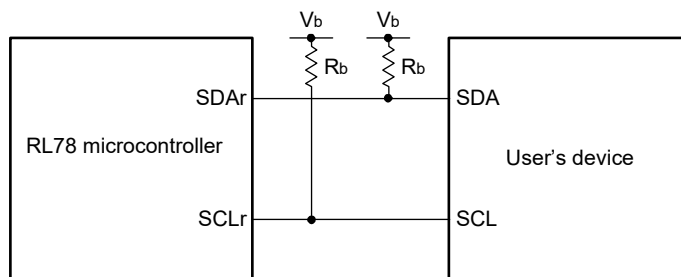
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f <sub>SCL</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ		1000 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ		400 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ		300 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475		1550		1550		1550		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1150		1550		1550		1550		ns
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1550		1550		1550		1550		ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	200		610		610		610		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	600		610		610		610		ns
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	610		610		610		610		ns
Data setup time (reception)	t <sub>SU-DAT</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 Note 3		1/f <sub>MCK</sub> + 190 Note 2		1/f <sub>MCK</sub> + 190 Note 3		1/f <sub>MCK</sub> + 190 Note 3		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 190 Note 3		1/f <sub>MCK</sub> + 190 Note 3		1/f <sub>MCK</sub> + 190 Note 3		1/f <sub>MCK</sub> + 190 Note 3		ns
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1/f <sub>MCK</sub> + 190 Note 3		1/f <sub>MCK</sub> + 190 Note 3		1/f <sub>MCK</sub> + 190 Note 3		1/f <sub>MCK</sub> + 190 Note 3		ns
Data hold time (transmission)	t <sub>HD-DAT</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	0	355	0	355	0	355	0	355	ns
		1.8 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	0	405	0	405	0	405	0	405	ns

**Note 1.** The value must also be equal to or less than f<sub>MCK</sub>/4.**Note 2.** Use it with V<sub>DD</sub> ≥ V<sub>b</sub>.**Note 3.** Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

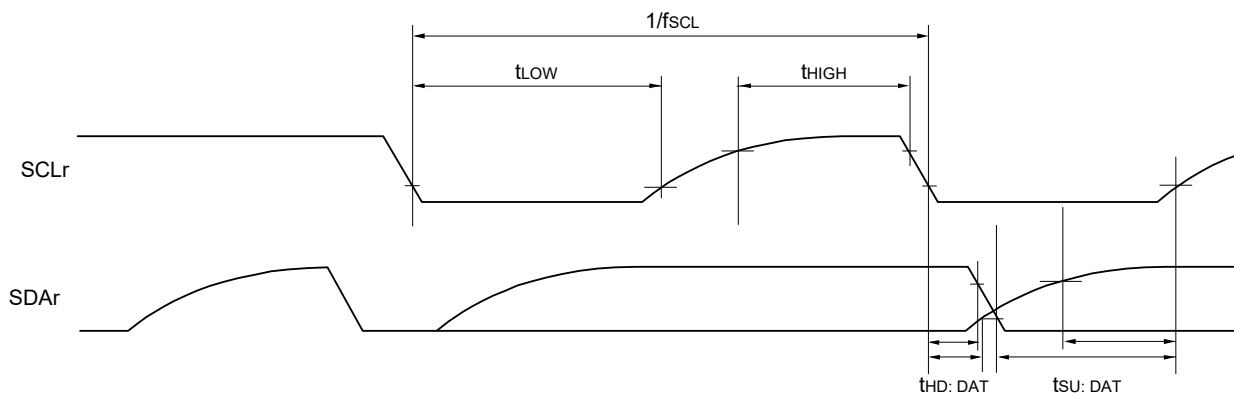
**Caution** Select the TTL input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance) mode for the SDAr pin and the N-ch open drain output (V<sub>DD</sub> tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)**



**Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**



- Remark 1.**  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01), g: PIM, POM number (g = 5)
- Remark 3.**  $f_{mck}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

**(10) Communication at different potential (1.8 V, 2.5 V) (simplified I<sup>2</sup>C mode)****(T<sub>A</sub> = +85 to 105°C, 2.4 V ≤ AV<sub>DD</sub> = V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)**

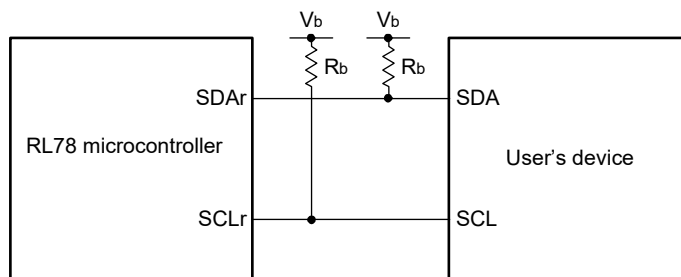
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f <sub>SCL</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1200		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	4600		ns
		2.4 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	500		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	2400		ns
		2.4 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1830		ns
Data setup time (reception)	t <sub>SU-DAT</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 340 Note 3		ns
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 760 Note 3		ns
		2.4 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1/f <sub>MCK</sub> + 570 Note 3		ns
Data hold time (transmission)	t <sub>HD-DAT</sub>	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	770	ns
		2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	0	1420	ns
		2.4 V ≤ V <sub>DD</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V Note 2, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	0	1215	ns

**Note 1.** The value must also be equal to or less than f<sub>MCK</sub>/4.**Note 2.** Use it with V<sub>DD</sub> ≥ V<sub>b</sub>.**Note 3.** Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

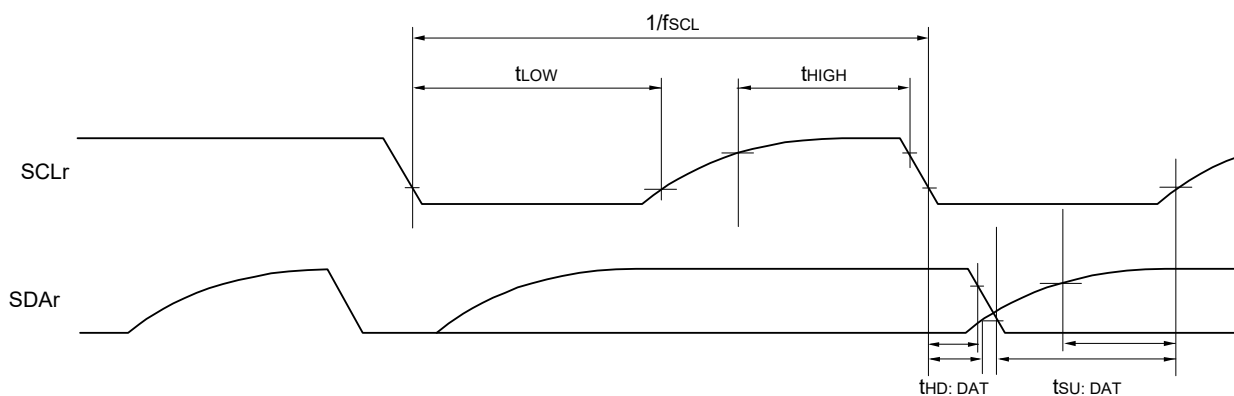
**Caution** Select the TTL input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance) mode for the SDAr pin and the N-ch open drain output (V<sub>DD</sub> tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)**



**Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**



- Remark 1.**  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01), g: PIM and POM numbers (g = 5)
- Remark 3.**  $f_{mck}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

#### Classification of A/D converter characteristics

Reference Voltage Input Channel	Reference voltage (+) = $AV_{REFP}$ Reference voltage (-) = $AV_{REFM}$	Reference voltage (+) = $AV_{DD}$ Reference voltage (-) = $AV_{SS}$	Reference voltage (+) = Internal reference voltage Reference voltage (-) = $AV_{SS}$
High-accuracy channel; ANI0 to ANI13 (input buffer power supply: $AV_{DD}$ )	Refer to 2.6.1 (1). Refer to 2.6.1 (7).	Refer to 2.6.1 (2). Refer to 2.6.1 (7).	Refer to 2.6.1 (5). Refer to 2.6.1 (10).
Standard channel; ANI16 to ANI18 (input buffer power supply: $V_{DD}$ )	Refer to 2.6.1 (3). Refer to 2.6.1 (8).	Refer to 2.6.1 (4). Refer to 2.6.1 (9).	
Internal reference voltage, Temperature sensor output voltage	Refer to 2.6.1 (3). Refer to 2.6.1 (8).	Refer to 2.6.1 (4). Refer to 2.6.1 (9).	—

(1) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), conversion target:  $ANI2$  to  $ANI13$

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $AV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	8		12	bit
		$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	8		10 Note 1	
		$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 6.0$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 5.0$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 2.5$	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	3.375		$\mu\text{s}$
		ADTYP = 0, 10-bit resolution Note 1	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	6.75		
		ADTYP = 0, 8-bit resolution Note 2	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	13.5		
		ADTYP = 1, 8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	2.5625		
			$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	5.125		
Zero-scale error Note 3	Ezs	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 4.5$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 4.5$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 2.0$	
Full-scale error Note 3	EFS	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 4.5$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 4.5$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 2.0$	
Integral linearity error Note 3	ILE	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 2.0$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 1.5$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 1.0$	
Differential linearity error Note 3	DLE	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 1.5$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 1.5$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$		$\pm 1.0$	
Analog input voltage	VAIN		0		$AV_{REFP}$	V

**Note 1.** Cannot be used for lower 2 bit of ADCR register

**Note 2.** Cannot be used for lower 4 bit of ADCR register

**Note 3.** Excludes quantization error ( $\pm 1/2$  LSB).

**Caution** Always use  $AV_{DD}$  pin with the same potential as the  $V_{DD}$  pin.

(2) When reference voltage (+) = AV<sub>DD</sub> (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AV<sub>SS</sub> (ADREFM = 0), conversion target: ANI0 to ANI13

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ AV<sub>DD</sub> = V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = AV<sub>DD</sub>, Reference voltage (-) = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±7.5	LSB
		10-bit resolution	1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±3.0	
Conversion time	t <sub>CONV</sub>	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V	2.5625			
			1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V	5.125			
	1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V	10.25					
Zero-scale error Note 3	E <sub>ZS</sub>	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±2.5	
Full-scale error Note 3	E <sub>FS</sub>	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±1.5	
Analog input voltage	V <sub>AIN</sub>	ANI0 to ANI6		0		AV <sub>DD</sub>	V

**Note 1.** Cannot be used for lower 2 bit of ADCR register

**Note 2.** Cannot be used for lower 4 bit of ADCR register

**Note 3.** Excludes quantization error (±1/2 LSB).

**Caution** Always use AV<sub>DD</sub> pin with the same potential as the V<sub>DD</sub> pin.

- (3) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), conversion target: ANI16 to ANI18, internal reference voltage, temperature sensor output voltage

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ ,  $1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $AV_{SS} = 0\text{ V}$ ,

Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	8		12	bit
			$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	8		10 Note 1	
			$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 7.0$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 5.5$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 3.0$	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	4.125			$\mu\text{s}$
		ADTYP = 0, 10-bit resolution Note 1	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	9.5			
		ADTYP = 0, 8-bit resolution Note 2	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	57.5			
		ADTYP = 1, 8-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	3.3125			
			$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	7.875			
	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	54.25					
Zero-scale error Note 3	Ezs	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 5.0$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 5.0$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 2.5$	
Full-scale error Note 3	Efs	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 5.0$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 5.0$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 2.5$	
Integral linearity error Note 3	ILE	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 3.0$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 2.0$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 1.5$	
Differential linearity error Note 3	DLE	12-bit resolution	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 2.0$	LSB
		10-bit resolution	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 2.0$	
		8-bit resolution	$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 1.5$	
Analog input voltage	VAIN			0		$AV_{REFP}$	V
		Internal reference voltage ( $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ )		$V_{BGR}$ Note 4			
		Temperature sensor output voltage ( $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ )		$V_{TMP25}$ Note 4			

**Note 1.** Cannot be used for lower 2 bits of ADCR register

**Note 2.** Cannot be used for lower 4 bits of ADCR register

**Note 3.** Excludes quantization error ( $\pm 1/2$  LSB).

**Note 4.** Refer to 2.6.2 Temperature sensor, internal reference voltage output characteristics.

**Caution** Always use  $AV_{DD}$  pin with the same potential as the  $V_{DD}$  pin.



(4) When reference voltage (+) = AVDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI16 to ANI18, internal reference voltage, temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVDD, Reference voltage (-) = AVSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVDD ≤ 3.6 V	8		12	bit
			1.8 V ≤ AVDD ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AVDD ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.5	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AVDD ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AVDD ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	3.3125			
			1.8 V ≤ AVDD ≤ 3.6 V	7.875			
	1.6 V ≤ AVDD ≤ 3.6 V	54.25					
Zero-scale error Note 3	Ezs	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.0	
Full-scale error Note 3	EFS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±3.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AVDD ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AVDD ≤ 3.6 V			±2.0	
Analog input voltage	VAIN			0		AVDD	V
		Internal reference voltage (1.8 V ≤ VDD ≤ 3.6 V)		VBGR Note 4			
		Temperature sensor output voltage (1.8 V ≤ VDD ≤ 3.6 V)		VTMP25 Note 4			

**Note 1.** Cannot be used for lower 2 bits of ADCR register

**Note 2.** Cannot be used for lower 4 bits of ADCR register

**Note 3.** Excludes quantization error (±1/2 LSB).

**Note 4.** Refer to 2.6.2 Temperature sensor, internal reference voltage output characteristics.

**Caution** Always use AVDD pin with the same potential as the VDD pin.

- (5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI13, ANI16 to ANI18

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	tCONV	8-bit resolution	16			μs
Zero-scale error <sup>Note</sup>	EZS	8-bit resolution			±4.0	LSB
Integral linearity error <sup>Note</sup>	ILE	8-bit resolution			±2.0	LSB
Differential linearity error <sup>Note</sup>	DLE	8-bit resolution			±2.5	LSB
Analog input voltage	VAIN		0		VBGR	V

**Note** Excludes quantization error (±1/2 LSB).

**Caution** Always use AVDD pin with the same potential as the VDD pin.

- (6) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI13

(TA = +85 to +105°C, 2.4 V ≤ AVREFP ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8		12	bit
Overall error <sup>Note</sup>	AINL	12-bit resolution 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±6.0	LSB
Conversion time	tCONV	ADTYP = 0, 12-bit resolution 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	3.375			μs
Zero-scale error <sup>Note</sup>	EZS	12-bit resolution 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±4.5	LSB
Full-scale error <sup>Note</sup>	EFS	12-bit resolution 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±4.5	LSB
Integral linearity error <sup>Note</sup>	ILE	12-bit resolution 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	LSB
Differential linearity error <sup>Note</sup>	DLE	12-bit resolution 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.5	LSB
Analog input voltage	VAIN		0		AVREFP	V

**Note** Excludes quantization error (±1/2 LSB).

**Caution** Always use AVDD pin with the same potential as the VDD pin.

(7) When reference voltage (+) = AV<sub>DD</sub> (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AV<sub>SS</sub> (ADREFM = 0), conversion target: ANI0 to ANI13

(T<sub>A</sub> = +85 to +105°C, 2.4 V ≤ AV<sub>DD</sub> = V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = AV<sub>DD</sub>, Reference voltage (-) = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V	8		12	bit
Overall error <sup>Note</sup>	AINL	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±7.5	LSB
Conversion time	t <sub>CONV</sub>	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V	3.375			μs
Zero-scale error <sup>Note</sup>	E <sub>ZS</sub>	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±6.0	LSB
Full-scale error <sup>Note</sup>	E <sub>FS</sub>	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±6.0	LSB
Integral linearity error <sup>Note</sup>	ILE	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±3.0	LSB
Differential linearity error <sup>Note</sup>	DLE	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±2.0	LSB
Analog input voltage	V <sub>AIN</sub>			0		AV <sub>DD</sub>	V

**Note** Excludes quantization error (±1/2 LSB).

**Caution** Always use AV<sub>DD</sub> pin with the same potential as the V<sub>DD</sub> pin.

(8) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), conversion target ANI16 to ANI18, internal reference voltage, temperature sensor output voltage

( $T_A = +85$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $AV_{SS} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	8		12	bit
Overall error Note 1	AINL	12-bit resolution $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 7.0$	LSB
Conversion time	tCONV	ADTYP = 0, 12-bit resolution $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$	4.125			$\mu\text{s}$
Zero-scale error Note 1	EzS	12-bit resolution $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 5.0$	LSB
Full-scale error Note 1	EFS	12-bit resolution $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 5.0$	LSB
Integral linearity error Note 1	ILE	12-bit resolution $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 3.0$	LSB
Differential linearity error Note 1	DLE	12-bit resolution $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 3.6\text{ V}$			$\pm 2.0$	LSB
Analog input voltage	VAIN		0		$AV_{REFP}$	V
		Internal reference voltage ( $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ )	$V_{BGR}$ Note 2			
		Temperature sensor output voltage ( $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ )	$V_{TMP25}$ Note 2			

**Note 1.** Excludes quantization error ( $\pm 1/2$  LSB).

**Note 2.** Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

**Caution** Always use  $AV_{DD}$  pin with the same potential as the  $V_{DD}$  pin.

(9) When reference voltage (+) = AV<sub>DD</sub> (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AV<sub>SS</sub> (ADREFM = 0), conversion target: ANI16 to ANI18, internal reference voltage, temperature sensor output voltage

(T<sub>A</sub> = +85 to +105°C, 2.4 V ≤ AV<sub>DD</sub> = V<sub>DD</sub> ≤ 3.6 V, V<sub>SS</sub> = 0 V, AV<sub>SS</sub> = 0 V, Reference voltage (+) = AV<sub>DD</sub>, Reference voltage (-) = AV<sub>SS</sub> = 0)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V	8		12	bit
Overall error <sup>Note 1</sup>	AINL	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±8.5	LSB
Conversion time	t <sub>CONV</sub>	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V	4.125			μs
Zero-scale error <sup>Note 1</sup>	E <sub>ZS</sub>	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±8.0	LSB
Full-scale error <sup>Note 1</sup>	E <sub>FS</sub>	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±8.0	LSB
Integral linearity error <sup>Note 1</sup>	ILE	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±3.5	LSB
Differential linearity error <sup>Note 1</sup>	DLE	12-bit resolution	2.4 V ≤ AV <sub>DD</sub> ≤ 3.6 V			±2.5	LSB
Analog input voltage	V <sub>AIN</sub>			0		AV <sub>DD</sub>	V
		Internal reference voltage (2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V)		V <sub>BGR</sub> <sup>Note 2</sup>			
		Temperature sensor output voltage (2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V)		V <sub>TMP25</sub> <sup>Note 2</sup>			

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

**Caution** Always use AV<sub>DD</sub> pin with the same potential as the V<sub>DD</sub> pin.

(10) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVss (ADREFM = 0), conversion target: ANI0 to ANI13, ANI16 to ANI18

(TA = +85 to +105°C, 2.4 V ≤ VDD, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, Vss = 0 V, AVss = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = AVss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	tCONV	8-bit resolution	16.0			μs
Zero-scale error <sup>Note</sup>	EZS	8-bit resolution			±4.0	LSB
Integral linearity error <sup>Note</sup>	ILE	8-bit resolution			±2.0	LSB
Differential linearity error <sup>Note</sup>	DLE	8-bit resolution			±2.5	LSB
Analog input voltage	VAIN		0		VBGR	V

**Note** Excludes quantization error (±1/2 LSB).

**Caution** Always use AVDD pin with the same potential as the VDD pin.

## 2.6.2 Temperature sensor, internal reference voltage output characteristics

(TA = -40 to 85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, Vss = AVss = 0 V)

(TA = +85 to 105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, Vss = AVss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	FVTMPS	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP	2.4 V ≤ VDD ≤ 3.6 V	5			μs
		1.8 V ≤ VDD < 2.4 V	10			

### 2.6.3 Comparator

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage range	lvref0	IVREF0 pin	0		VDD - 1.4 Note	V	
	lvref1	IVREF1 pin	1.4 Note		VDD	V	
	lvcmp	IVCMP0, IVCMP1 pins	-0.3		VDD + 0.3	V	
Output delay	td	AVDD = 3.0 V Input slew rate > 50 mV/μs	Comparator high-speed mode, standard mode			1.2	μs
			Comparator high-speed mode, window mode			2.0	μs
			Comparator low-speed mode, standard mode		3.0		μs
			Comparator low-speed mode, window mode		4		μs
Operation stabilization wait time	tcMP		100			μs	

**Note** In window mode, make sure that Vref1 - Vref0 ≥ 0.2 V.

## 2.6.4 Operational amplifier characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

( $T_A = +85$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Common mode input range	Vicm1	Low-power consumption mode		0.2		$AV_{DD} - 0.5$	V
	Vicm2	High-speed mode		0.3		$AV_{DD} - 0.6$	V
Output voltage range	Vo1	Low-power consumption mode		0.1		$AV_{DD} - 0.1$	V
	Vo2	High-speed mode		0.1		$AV_{DD} - 0.1$	V
Input offset voltage	Vioff			-10		10	mV
Open gain	Av			60	120		dB
Gain-bandwidth (GB) product	GBW1	Low-power consumption mode			0.04		MHz
	GBW2	High-speed mode			1.7		MHz
Phase margin	PM	CL = 20 pF		50			deg
Gain margin	GM	CL = 20 pF		10			dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power consumption mode		230		nV/ $\sqrt{\text{Hz}}$
	Vnoise2	f = 10 kHz			200		nV/ $\sqrt{\text{Hz}}$
	Vnoise3	f = 1 kHz	High-speed mode		90		nV/ $\sqrt{\text{Hz}}$
	Vnoise4	f = 2 kHz			70		nV/ $\sqrt{\text{Hz}}$
Power supply reduction ratio	PSRR				90		dB
Common mode signal reduction ratio	CMRR				90		dB
Operation stabilization wait time	Tstd1	CL = 20 pF	Low-power consumption mode	Only operational amplifier is activated <sup>Note</sup>	650		$\mu\text{s}$
	Tstd2				High-speed mode	13	
	Tstd3	CL = 20 pF	Low-power consumption mode	Operational amplifier and reference current circuit are activated simultaneously	650		$\mu\text{s}$
	Tstd4				High-speed mode	13	
Settling time	Tset1	CL = 20 pF	Low-power consumption mode			750	$\mu\text{s}$
	Tset2		High-speed mode			13	$\mu\text{s}$
Slew rate	Tslew1	CL = 20 pF	Low-power consumption mode		0.02		V/ $\mu\text{s}$
	Tslew2		High-speed mode		1.1		V/ $\mu\text{s}$
Load current	Iload1	Low-power consumption mode		-100		100	$\mu\text{A}$
	Iload2	High-speed mode		-100		100	$\mu\text{A}$
Load capacitance	CL					20	pF

**Note** When the operational amplifier reference current circuit is activated in advance.



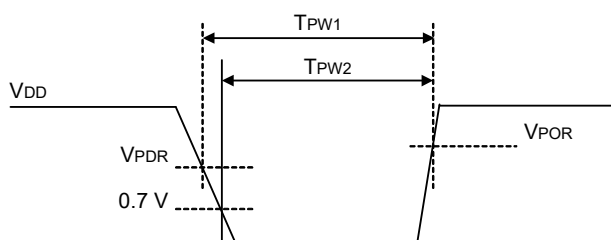
### 2.6.5 POR circuit characteristics

(TA = -40 to +105°C, Vss = AVss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Detection voltage	VPOR	Power supply rise time	TA = -40 to +85°C	1.47	1.51	1.55	V
			TA = +85 to +105°C	1.45	1.51	1.57	V
	VPDR	Power supply fall time <sup>Note 1</sup>	TA = -40 to +85°C	1.46	1.50	1.54	V
			TA = +85 to +105°C	1.44	1.50	1.56	V
Minimum pulse width <sup>Note 2</sup>	TPW1	Other than STOP/SUB HALT/SUB RUN	TA = +40 to +105°C	300			μs
	TPW2	STOP/SUB HALT/SUB RUN	TA = +40 to +105°C	300			μs

**Note 1.** However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 2.4 AC Characteristics.

**Note 2.** Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 2.6.6 LVD circuit characteristics

### (1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(TA = -40 to +85°C, VPDR ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD2	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		VLVD3	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		VLVD4	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		VLVD5	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		VLVD6	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		VLVD7	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		VLVD8	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		VLVD9	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		VLVD10	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		VLVD11	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		VLVD12	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		VLVD13	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

(TA = +85 to +105°C, VPDR ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	VLVD2	Power supply rise time	3.01	3.13	3.25	V		
			Power supply fall time	2.94	3.06	3.18	V		
		VLVD3	Power supply rise time	2.90	3.02	3.14	V		
			Power supply fall time	2.85	2.96	3.07	V		
		VLVD4	Power supply rise time	2.81	2.92	3.03	V		
			Power supply fall time	2.75	2.86	2.97	V		
		VLVD5	Power supply rise time	2.71	2.81	2.92	V		
			Power supply fall time	2.64	2.75	2.86	V		
		VLVD6	Power supply rise time	2.61	2.71	2.81	V		
			Power supply fall time	2.55	2.65	2.75	V		
		VLVD7	Power supply rise time	2.51	2.61	2.71	V		
			Power supply fall time	2.45	2.55	2.65	V		
		Minimum pulse width		tLW		300			μs
		Detection delay time						300	μs

## (2) LVD Detection Voltage of Interrupt &amp; Reset Mode

(TA = -40 to +85°C, VPDR ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	VLVDA0	VPOC0, VPOC1, VPOC2 = 0, 0, 0, falling reset voltage	1.60	1.63	1.66	V	
	VLVDA1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3	LVISO, LVIS1 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDB0	VPOC0, VPOC1, VPOC2 = 0, 0, 1, falling reset voltage	1.80	1.84	1.87	V	
	VLVDB1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	VLVDB3	LVISO, LVIS1 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	VLVDC0	VPOC0, VPOC1, VPOC2 = 0, 1, 0, falling reset voltage	2.40	2.45	2.50	V	
	VLVDC1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	VLVDC2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	VLVDD0	VPOC0, VPOC1, VPOC2 = 0, 1, 1, falling reset voltage	2.70	2.75	2.81	V	
VLVDD1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V	
		Falling interrupt voltage	2.80	2.86	2.91	V	
VLVDD2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V	
		Falling interrupt voltage	2.90	2.96	3.02	V	

(TA = +85 to +105°C, VPDR ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	VLVDD0	VPOC0, VPOC1, VPOC2 = 0, 1, 1, falling reset voltage	2.64	2.75	2.86	V	
	VLVDD1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	VLVDD2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V

## 2.6.7 Power supply voltage rising slope characteristics

(TA = -40 to +105°C, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.

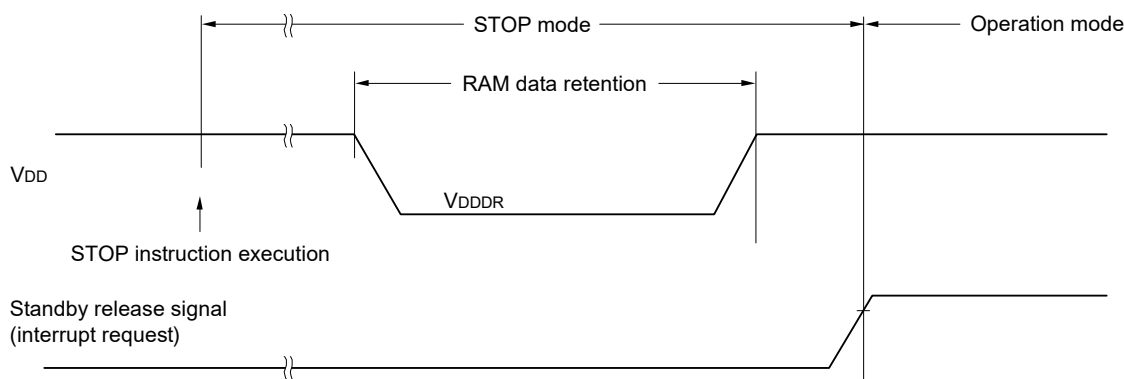
## 2.7 RAM Data Retention Characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

( $T_A = +85$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR	$T_A = -40$ to $+85^\circ\text{C}$	1.46 Note		3.6	V
		$T_A = +85$ to $+105^\circ\text{C}$	1.44 Note		3.6	V

**Note** The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



## 2.8 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

( $T_A = +85$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C <sub>erwr</sub>	Retained for 20 years $T_A = 85^\circ\text{C}$ Note 4	1,000			Times
		Retained for 1 year $T_A = 25^\circ\text{C}$ Note 4		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ Note 4	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ Note 4	10,000			
Number of data flash rewrites Notes 1, 2, 3						

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> **Note 4.** This temperature is the average value at which data are retained.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

## 2.10 Timing of Entry to Flash Memory Programming Modes

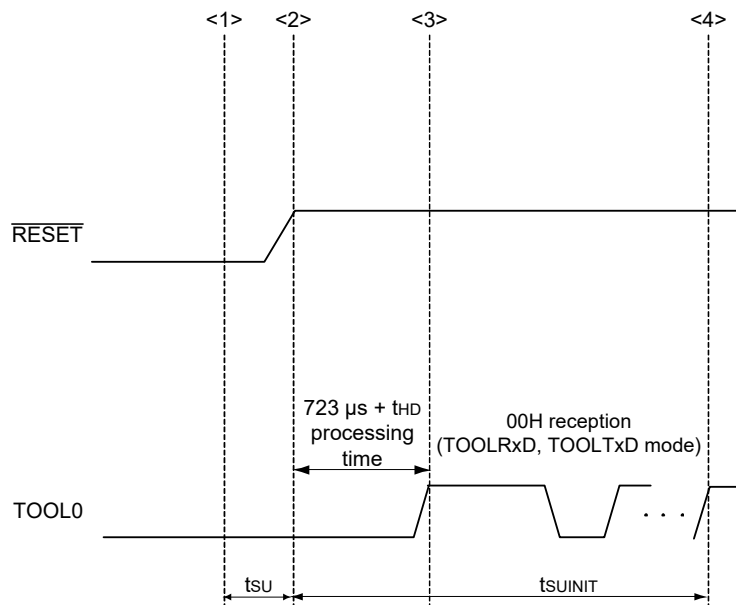
(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified <i>Note 1</i>	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends <i>Note 1</i>	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) <i>Notes 1, 2</i>	tHD	POR and LVD reset must end before the external reset ends.	1			ms

**Note 1.** Deassertion of the POR and LVD reset signals must precede deassertion of the pin reset signal.

**Note 2.** This excludes the flash firmware processing time (723 μs).



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

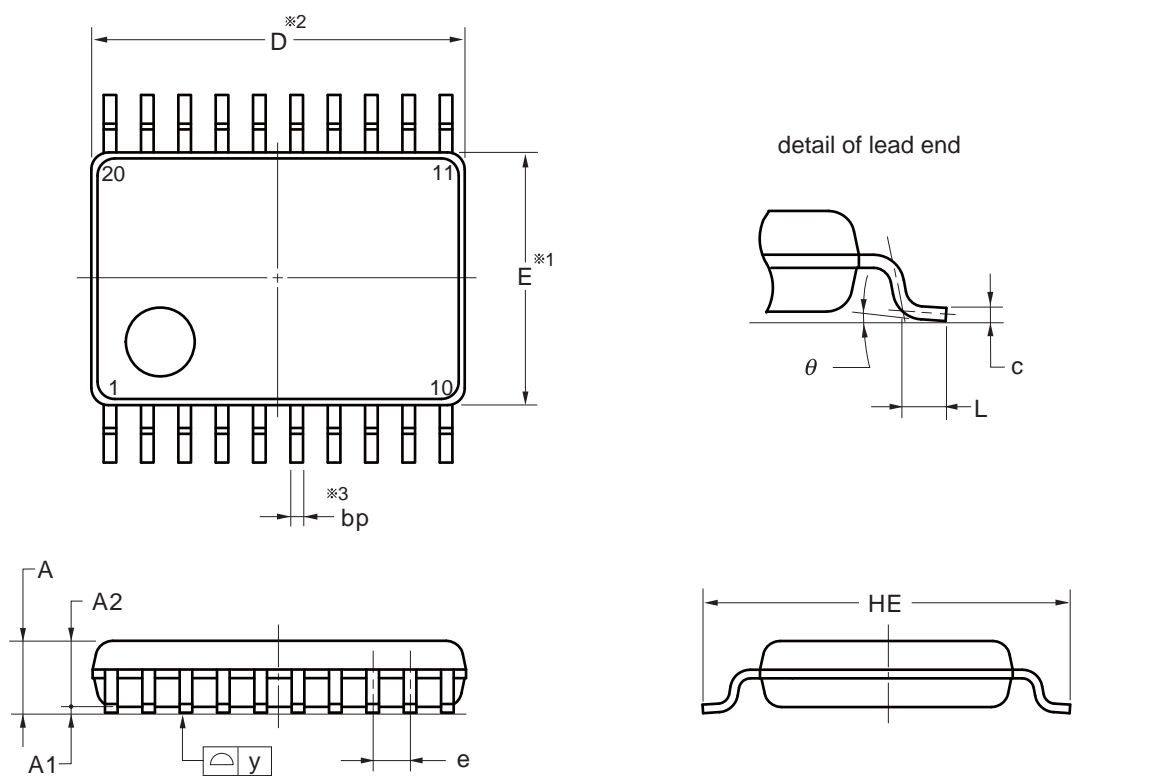
tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

### 3. PACKAGE DRAWINGS

#### 3.1 20-pin products

R5F1176AGSP, R5F11768GSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



**NOTE**

- 1. Dimensions "※1" and "※2" do not include mold flash.
- 2. Dimension "※3" does not include trim offset.

(UNIT:mm)

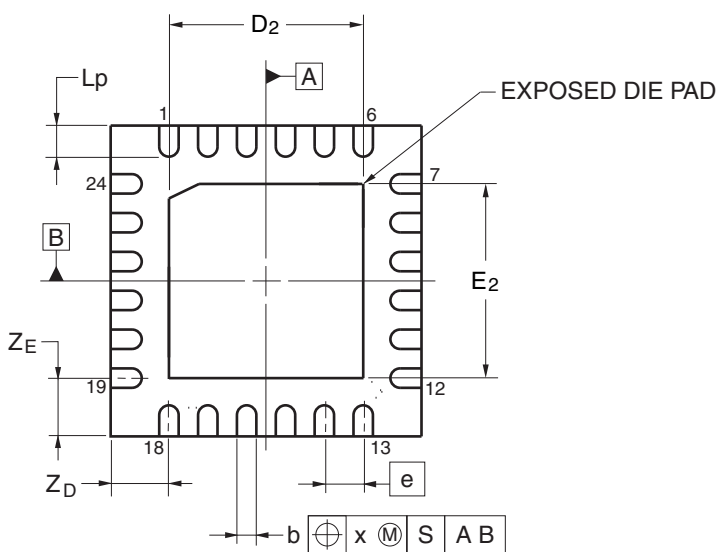
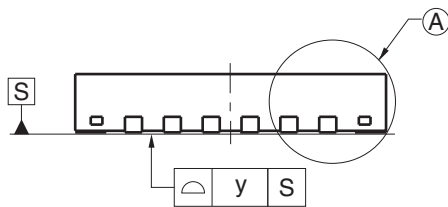
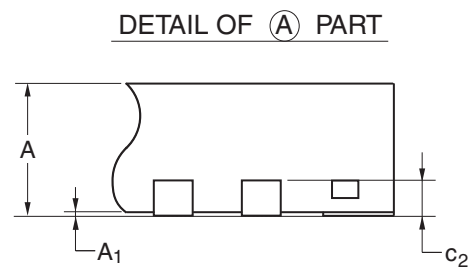
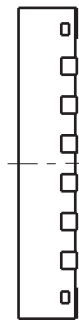
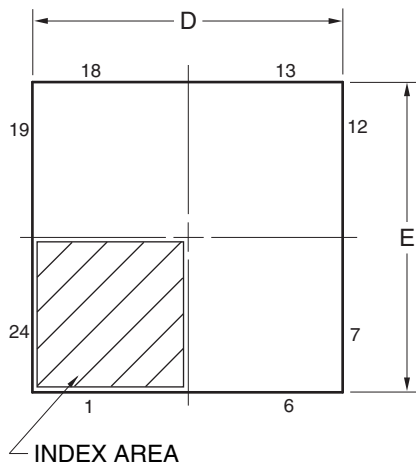
ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	0.22 <sup>+0.10</sup> <sub>-0.05</sub>
c	0.15 <sup>+0.05</sup> <sub>-0.02</sub>
L	0.50±0.20
y	0.10
θ	0° to 10°

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### 3.2 24-pin products

R5F1177AGNA, R5F11778GNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-3	0.04



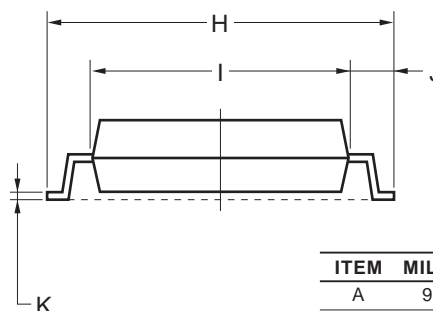
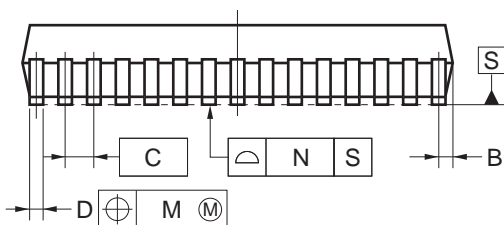
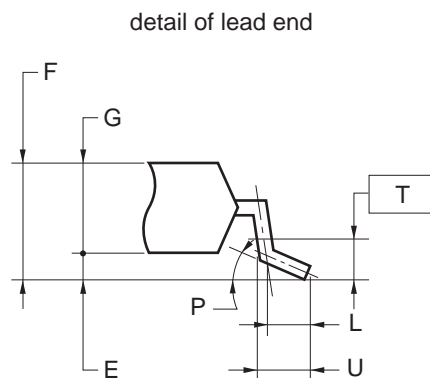
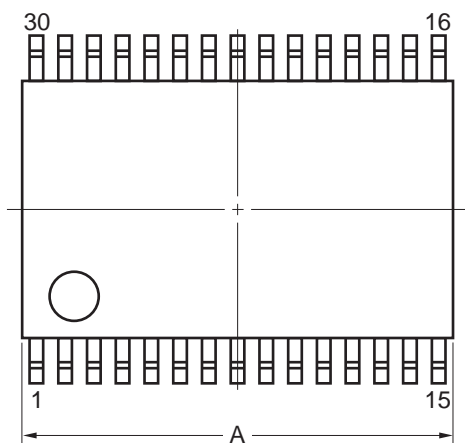
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.95	4.00	4.05
E	3.95	4.00	4.05
A	—	—	0.80
A <sub>1</sub>	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
L <sub>p</sub>	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z <sub>D</sub>	—	0.75	—
Z <sub>E</sub>	—	0.75	—
c <sub>2</sub>	0.15	0.20	0.25
D <sub>2</sub>	—	2.50	—
E <sub>2</sub>	—	2.50	—

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### 3.3 30-pin products

R5F117ACGSP, R5F117AAGSP, R5F117A8GSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

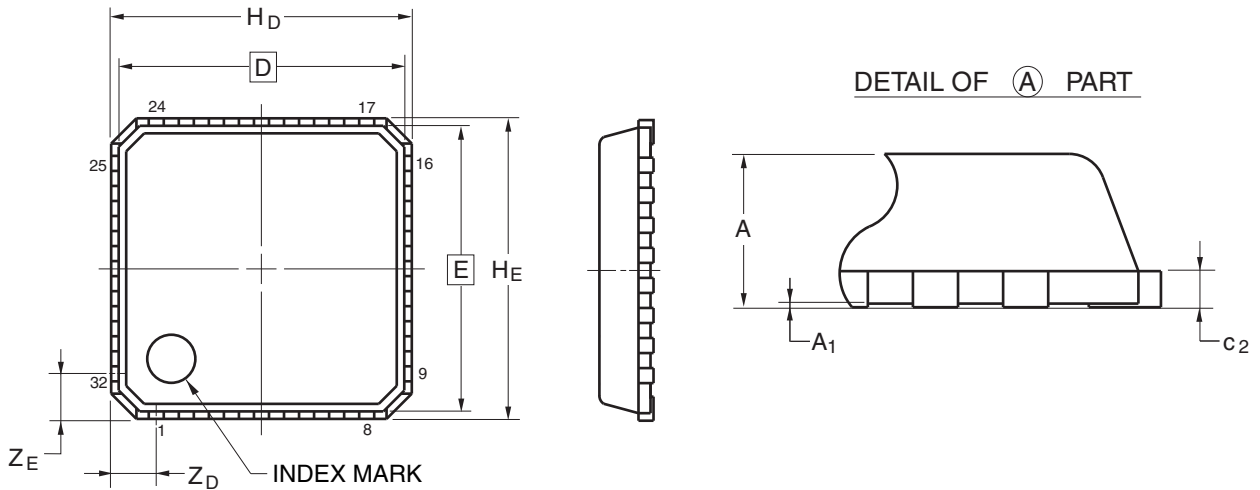
ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° <sup>+5°</sup> <sub>-3°</sub>
T	0.25
U	0.6±0.15



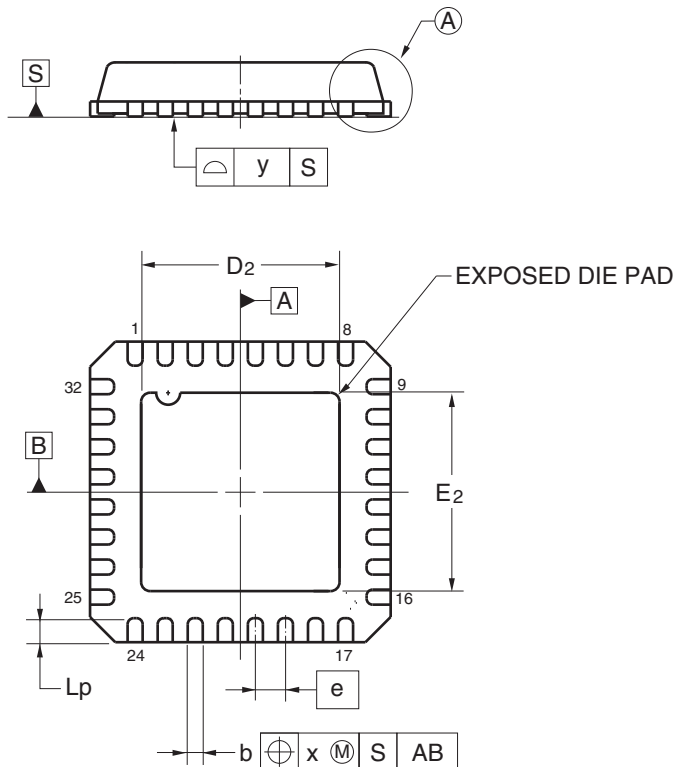
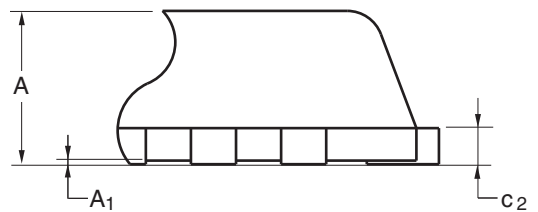
### 3.4 32-pin products

R5F117BCGNA, R5F117BAGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN32-5x5-0.50	PVQN0032KE-A	P32K9-50B-BAH	0.058



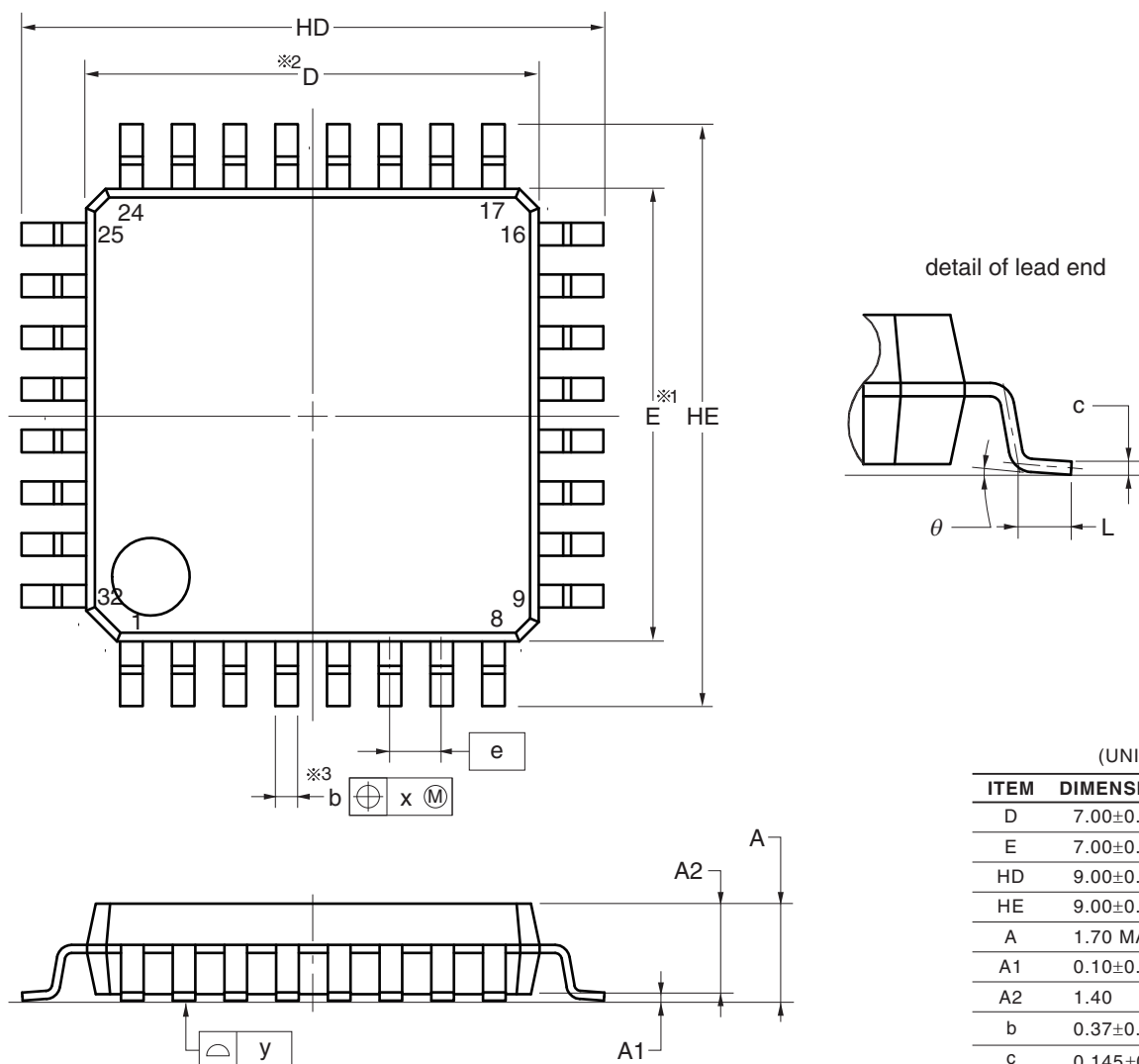
DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.75	—
E	—	4.75	—
A	—	—	0.90
A <sub>1</sub>	0.00	—	—
b	0.20	0.25	0.30
e	—	0.50	—
L <sub>p</sub>	0.30	0.40	0.50
x	—	—	0.10
y	—	—	0.05
H <sub>D</sub>	4.95	5.00	5.05
H <sub>E</sub>	4.95	5.00	5.05
Z <sub>D</sub>	—	0.75	—
Z <sub>E</sub>	—	0.75	—
c <sub>2</sub>	0.19	0.20	0.21
D <sub>2</sub>	—	3.30	—
E <sub>2</sub>	—	3.30	—

R5F117BAGFP, R5F117BCGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

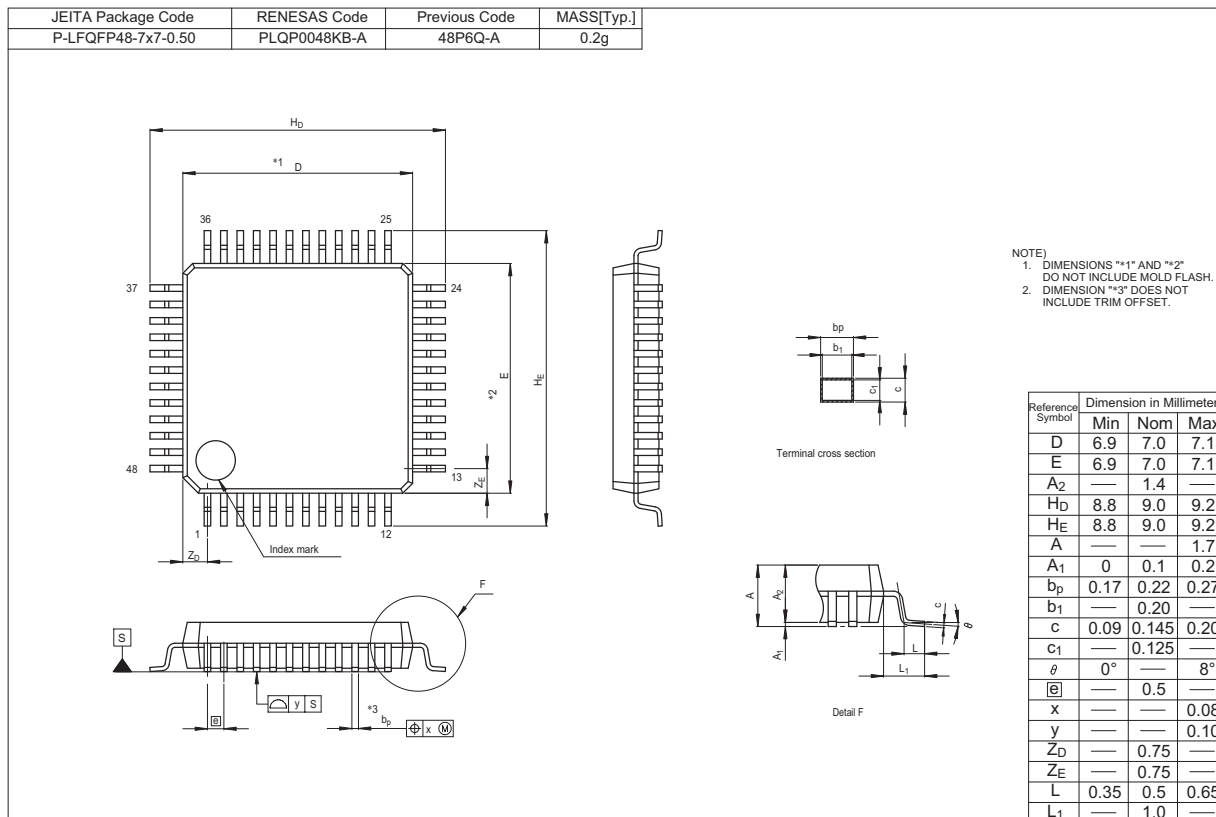
ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

**NOTE**

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

### 3.5 48-pin products

<R> R5F117GCGFB, R5F117GAGFB



## REVISION HISTORY

## RL78/I1D Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Aug 29, 2014	—	First Edition issued
2.00	Jan 16, 2015	24, 25, 27	Addition of note 7 in 2.3.2 Supply current characteristics
		24, 26	Addition of description in 2.3.2 Supply current characteristics
		26, 28	Modification of description in 2.3.2 Supply current characteristics
		28	Correction of error in 2.3.2 Supply current characteristics
		95	Modification of package drawing in 3.2 24-pin products
2.20	Feb 20, 2017	ALL	The function name changed from real-time clock to real-time clock 2
		5	Addition of product name in 1.3.1 20-pin products
		6	Addition of product name in 1.3.2 24-pin products
		7	Addition of product name in 1.3.3 30-pin products
		8	Addition of product name in 1.3.4 32-pin products
		9	Change of description and addition of product name in 1.3.4 32-pin products
		10	Addition of product name in 1.3.5 48-pin products
		13, 14	Change of description in 1.6 Outline of Functions
		16	Change of 2.1 Absolute Maximum Ratings
		22	Change of 2.3.1 Pin characteristics
		24	Change of conditions in 2.3.2 Supply current characteristics
		25, 27, 28	Change of note 1 in 2.3.2 Supply current characteristics
		26	Change of conditions and unit in 2.3.2 Supply current characteristics
		30	Change of note 3 in 2.3.2 Supply current characteristics
		31	Addition of note 5 in 2.3.2 Supply current characteristics
92	Change of table in 2.8 Flash Memory Programming Characteristics		
92	Addition of note 4 in 2.8 Flash Memory Programming Characteristics		
99	Change of package drawing in 3.5 48-pin products		

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## NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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#### Renesas Electronics America Inc.

2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.  
Tel: +1-408-588-6000, Fax: +1-408-588-6130

#### Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

#### Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

#### Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

#### Renesas Electronics (China) Co., Ltd.

Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

#### Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

#### Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852-2886-9022

#### Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

#### Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

#### Renesas Electronics Malaysia Sdn.Bhd.

Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

#### Renesas Electronics India Pvt. Ltd.

No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

#### Renesas Electronics Korea Co., Ltd.

12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141