MPQ4480

6A, 36V, Step-Down Converter for Automotive, AEC-Q100 Qualified

DESCRIPTION

The MPQ4480 is a high-frequency, synchronous rectified, step-down, switch-mode converter. It achieves 6A output current over a wide input-supply range with excellent load and line regulation over a wide input supply range. The MPQ4480 has synchronous mode operation for higher efficiency over the output load range.

Fault condition protection includes hiccup current limiting, OVP, and thermal shutdown (TSD).

The MPQ4480 requires a minimal number of readily available, standard external components. The MPQ4480 is available in a QFN-25 (4mmx5mm) package.

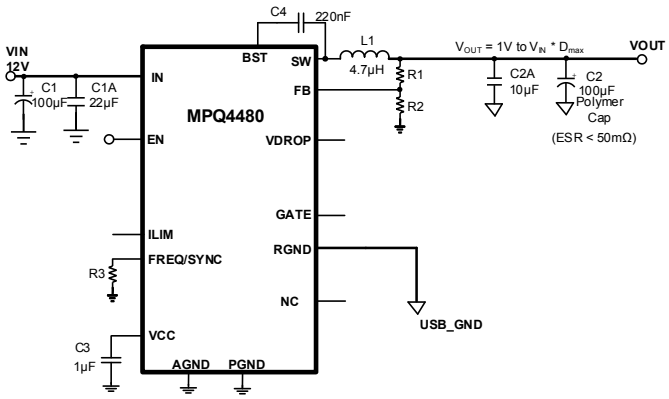
FEATURES

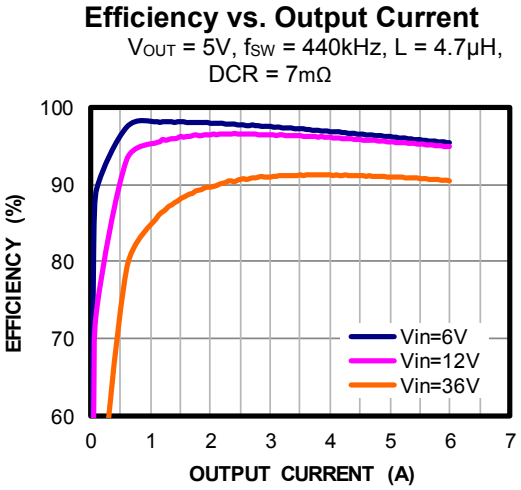
- 4.2V to 36V Operating Input Voltage Range
- 6A Output Current
- Internal Auto EN Pull-Up
- 20mΩ/15mΩ Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- Integrated 4mΩ Ground Sensing Resistor
- Frequency Adjustable (235kHz to 2.2MHz)
- CC Output Current Limit, 3-Level Adjustable, 2.75A/3.75A/7.5A
- Forced PWM Mode
- Frequency SYNC from 300kHz to 2.1MHz
- (Recommend: <25% of SYNC Duty Cycle)
- Spread Spectrum Option with 450kHz f_{SW}
- EN Shutdown Discharge
- Low Dropout Mode
- Battery Short to Ground Protect Driver
- Output Over-Voltage Protection
- Adjustable Line Drop Compensation
- Support 1V to 20V Output Adjustable
- Available in a QFN-25 (4mmx5mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment System
- Automotive USB Hub
- Wireless Charging

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ4480GV-AEC1*	QFN-25 (4mmx5mm)	*See Below*
MPQ4480GV-FD-AEC1**	QFN-25 (4mmx5mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ4480GV-AEC1–Z)

** For Tape & Reel, add suffix –Z (e.g. MPQ4480GV-FD-AEC1-Z)

DEVICE COMPARISON INFORMATION

Part Number	Frequency Spread Spectrum
MPQ4480GV-AEC1	No
MPQ4480GV-FD-AEC1	Yes

TOP MARKING

MPSYWW

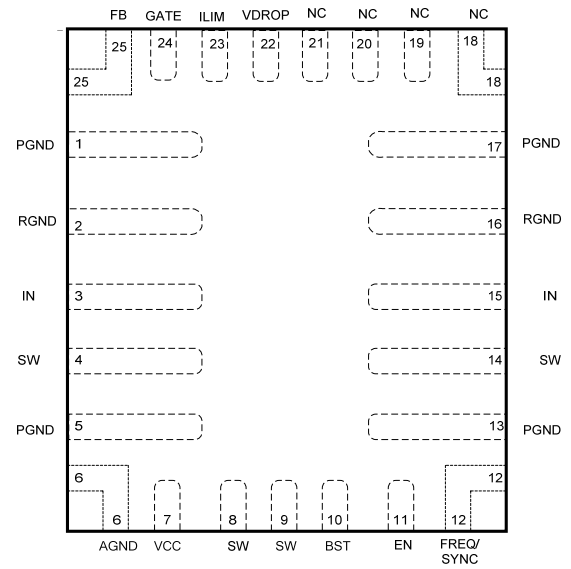
MP4480

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP4480: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-25 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 5, 13, 17	PGND	**Power ground.** Reference ground of the regulated output voltage. PGND requires extra care during PCB layout. Connect to GND with copper traces and vias. All PGND pins must be connected together.
2, 16	RGND	**Remote power ground.** There is an internal 4mΩ current-sensing resistor from RGND to PGND (pin 17 and pin 1).
3,15	IN	**Supply voltage.** The MPQ4480 operates from a 4.2V to 36V input voltage. C_{IN} prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible. IN is the drain of the internal power device, and provides the power supply for the entire chip.
4, 8, 9, 14	SW	**Switch output.** These pins must be connected together by a PCB trace. Use a wide PCB trace to make the connection.
6	AGND	**Analog ground.** Connect AGND to PGND.
7	VCC	**Internal 5.05V LDO regulator output.** Decouple with a 1μF capacitor.
10	BST	**Bootstrap.** A 0.22μF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
11	EN	**On/off control input.** The enable pin is an internal auto pull-up with a 7μA current source. EN has two stage thresholds: when EN is higher than ~1V, the VCC and bias circuitry will be enabled; when EN is higher than 2V, the buck switcher starts to work.
12	FREQ/SYNC	**Switching frequency program input.** Connect a resistor from FREQ to GND to set the switching frequency. This pin also serves as a frequency-synchronous clock input.
18, 19, 20, 21	NC	**No connection.** These pins should be left floating.
22	VDROP	**Line drop amplitude selection.** Three levels can be programmable by pulling VDROP to GND or VCC, or floating.
23	ILIM	**Output CC current limit set pin.** Pull ILIM to VCC, GND, or float to set three different current limit levels.
24	GATE	**Gate drive for external, low-side, N-channel power MOSFET.** Open-drain structure. The GATE pin is pulled low to turn off the power MOSFET when the secondary current RGND-to-PGND limit is triggered.
25	FB	**Feedback.** Connect to the tap of an external resistor divider from the output to GND to set the output voltage.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 40V
V_{SW} ..... -0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN} ..... -0.3V to +10V (2)
All other pins ..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) (5)
QFN-25 (4mmx5mm) 5.4W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Operation input voltage range ..... 4.2V to 36V
Output current 6A
Output voltage range ..... 1V to V_{IN} * D_{MAX}
Operating junction temp…….. ..-40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-25 (4mmx5mm)			
EVQ4480-V-00A (5)	23	4	°C/W
JESD51-7 (6)	44	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS Max rating, see the EN control section on page 14.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EVQ4480-V-00A, 4-layer PCB, 50mmx50mm.
6) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V, T_J = -40°C to +125°C		15	25	μA
Supply current (quiescent)	I_{Q2}	No switching		1	2	mA
EN rising threshold	V_{EN_Rising}		1.96	2.06	2.16	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-up current	I_{EN}	V_{EN} = 3V	3	7	11	μA
Thermal shutdown (7)	T_{STD}			165		°C
Thermal hysteresis (7)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}		4.65	5.05	5.45	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}		3.7	3.95	4.2	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			500		mV
HS switch on resistance	R_{DSON_HS}			20	40	mΩ
LS switch on resistance	R_{DSON_LS}			15	35	mΩ
Feedback voltage	V_{FB}		0.985	1	1.015	V
Low-side current limit (7)	I_{LS_LIMIT}			-2		A
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +125°C			5	
High-side current limit	I_{LIMIT1}	ILIM = GND	8	17	27	A
		ILIM = VCC	12	22	35	
Output CC current limit	I_{LIMIT2}	ILIM = VCC (for 6A continuous), T_J = 25°C	6.6	7.5	8.4	A
		ILIM = float (for 3A continuous), T_J = 25°C	3.3	3.75	4.2	
		ILIM = GND (for 2.4A continuous), T_J = 25°C	2.5	2.75	3	
Oscillator frequency	f_{SW1}	R_{FREQ} = 97.6kΩ	170	235	300	kHz
	f_{SW2}	R_{FREQ} = 9.53kΩ	1800	2200	2600	
	f_{SW3}	R_{FREQ} = 52.3kΩ	350	440	530	
Frequency spread spectrum (7) (MPQ4480GV-FD-AEC1)	f_{SS}	R_{FREQ} = float, based on 450kHz		10		%
Sync frequency range	$FREQ_{SYNC\_IN}$		300		2100	kHz
Maximum on time	t_{ON_MAX}	Dropout mode, max duty cycle $D_{MAX} = t_{ON\_MAX} / (t_{ON\_MAX} + t_{OFF\_MIN})$	6	10		μs
Minimum off time	t_{OFF_MIN}			120		ns
Minimum on time (7)	t_{ON_MIN}			130		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Soft-start time	t_{SS}	10% to 90% V_{OUT}	0.4	1.1	1.8	ms
Line drop compensation gain (from I_{RTN} to I_{FB})	Gain1	VDROP pin = GND, T_J = 25°C	0.1	0.6	1.1	µA/A
	Gain2	VDROP pin = float, T_J = 25°C	1.5	3.25	5	µA/A
	Gain3	VDROP pin = VCC, T_J = 25°C	4	6.75	9.5	µA/A
OVP						
OVP rising threshold	V_{OVP1_RISE}		110%	115%	120%	V_{REF}
OVP falling threshold	V_{OVP_FALL}			105%		V_{REF}
OVP delay (7)	t_{OVPDEL}			2		µs
RGND Current Limit						
RGND to PGND resistor	R_{SENSE}			4	12	mΩ
Second current limit threshold	V_{SENSE_TH}			12		A
GATE pull-low resistance	R_{GATE_L}			85	180	Ω
Second current limit off time	$t_{EXT\_CUR\_RES}$		1	2	3	s

Note:

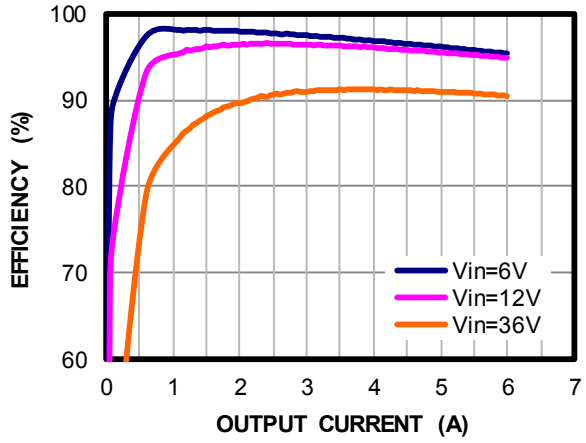
7) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted.

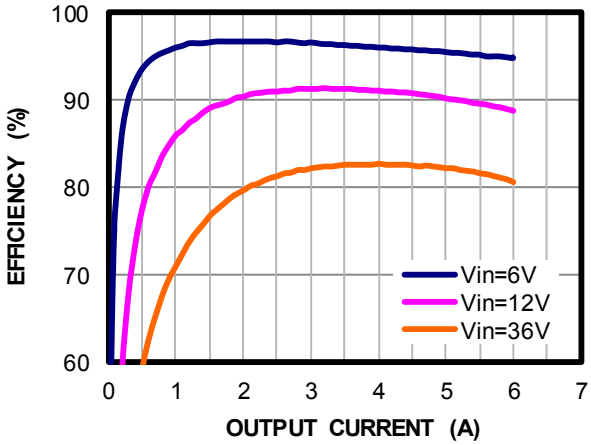
Efficiency vs. Output Current

V_{OUT} = 5V, f_{SW} = 440kHz, L = 4.7µH



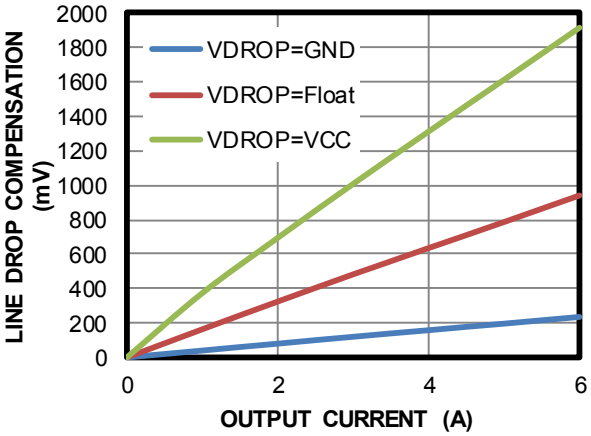
Efficiency vs. Output Current

V_{OUT} = 5V, f_{SW} = 2.2MHz, L = 2.2µH



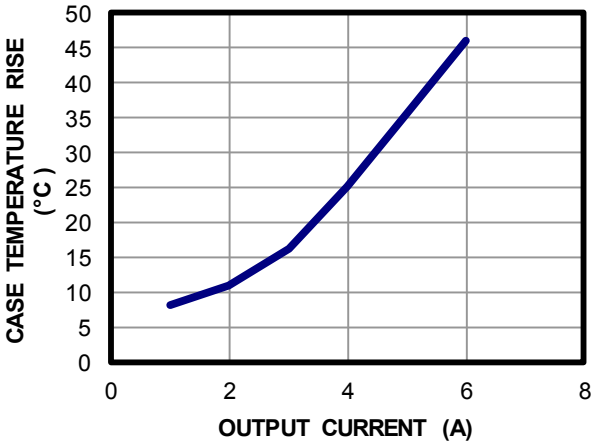
Line Drop Compensation

R1 = 40.2kΩ



Case Temperature Rise vs. IOUT

4-layers, 5cmx5cm

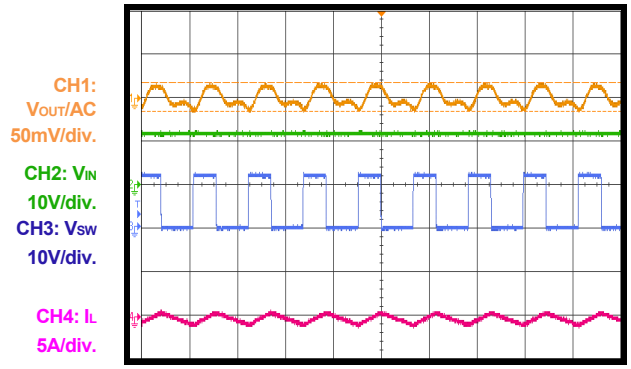


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted. All waveforms are tested based on bypassing the external MOSFET except Short Battery to Ground.

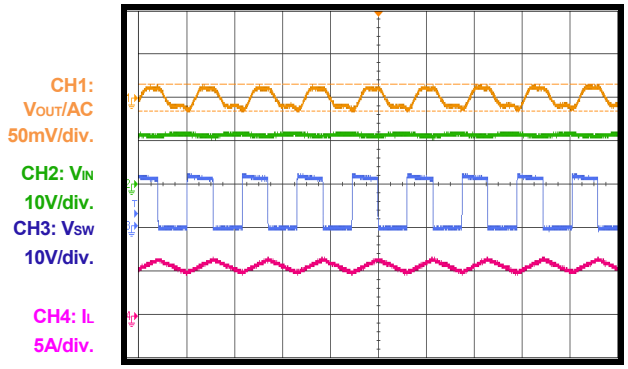
Output Ripple

f_{SW} = 440kHz, L = 4.7µH, I_{OUT} = 0A



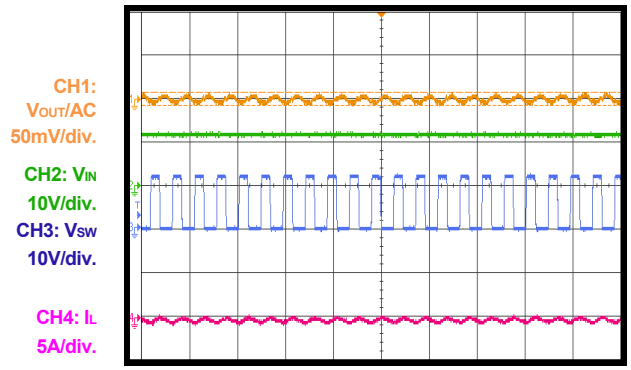
Output Ripple

f_{SW} = 440kHz, L = 4.7µH, I_{OUT} = 6A



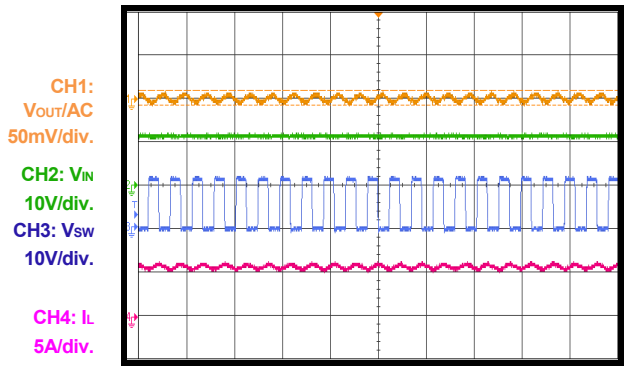
Output Ripple

f_{SW} = 2.2MHz, L = 2.2µH, I_{OUT} = 0A



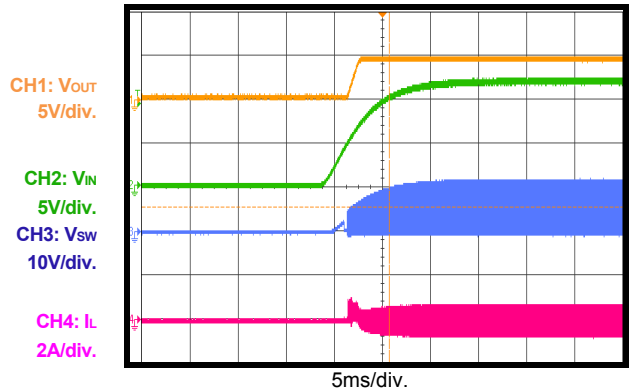
Output Ripple

f_{SW} = 2.2MHz, L = 2.2µH, I_{OUT} = 6A



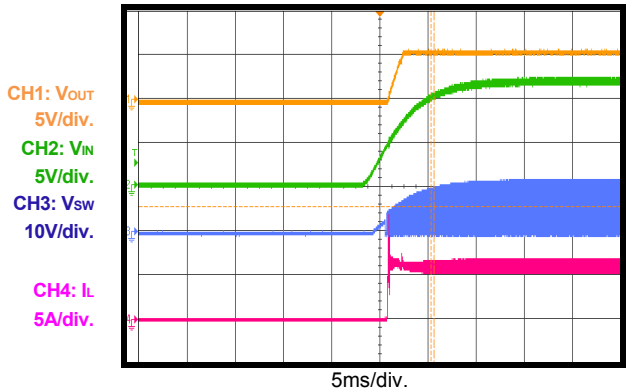
Power Start-Up

I_{OUT} = 0A



Power Start-Up

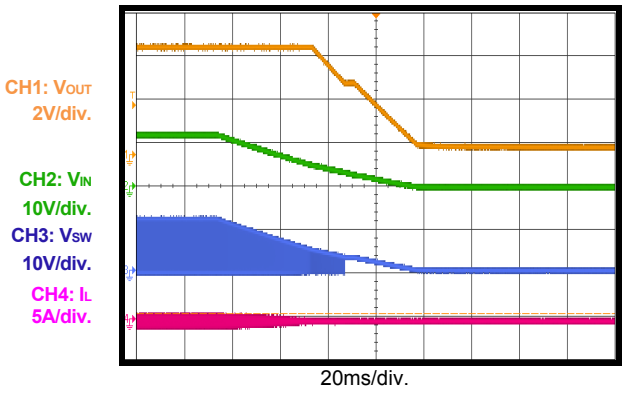
I_{OUT} = 6A



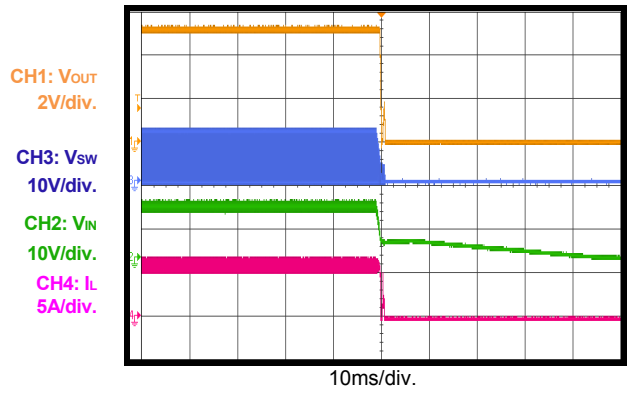
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted. All waveforms are tested based on bypassing the external MOSFET except Short Battery to Ground.

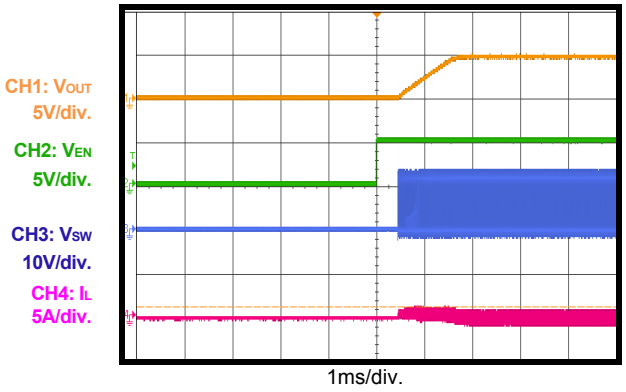
Power Shutdown
I_{OUT} = 0A



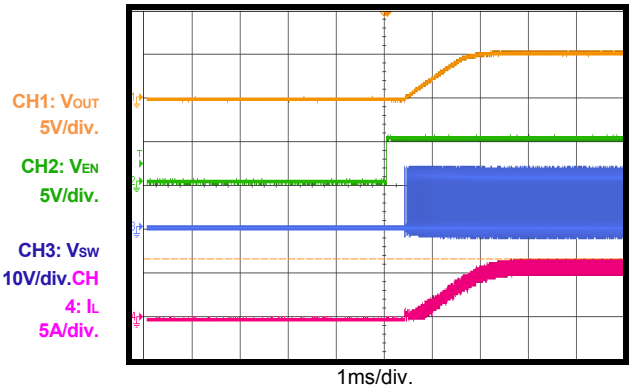
Power Shutdown
I_{OUT} = 6A



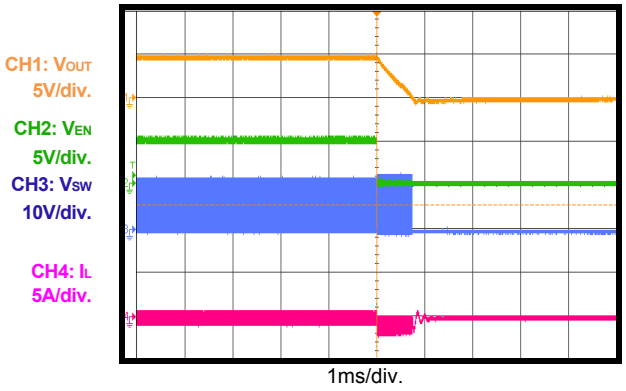
EN Start-Up
I_{OUT} = 0A



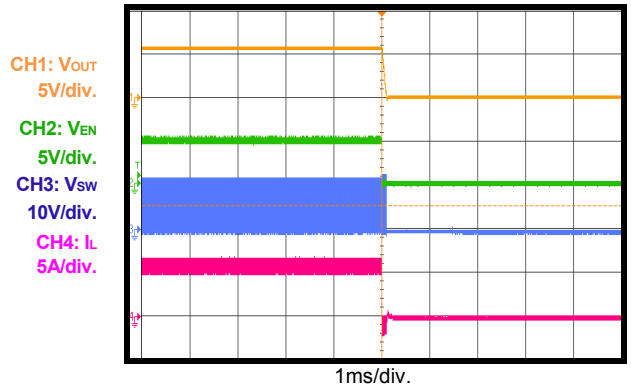
EN Start-Up
I_{OUT} = 6A



EN Shutdown
I_{OUT} = 0A



EN Shutdown
I_{OUT} = 6A

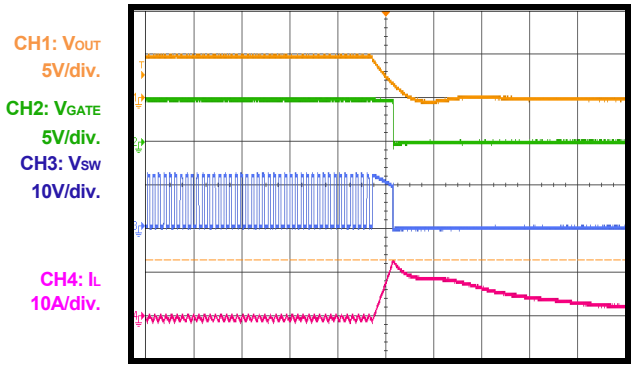


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted. All waveforms are tested based on bypassing the external MOSFET except Short Battery to Ground.

VOUT Short to USB_GND Entry

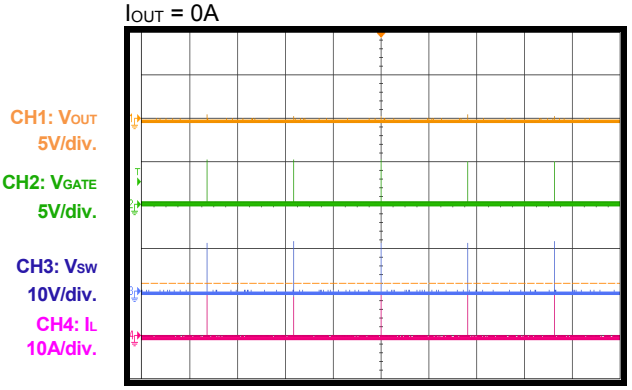
I_{OUT} = 0A



20µs/div.

VOUT Short to USB_GND Steady State

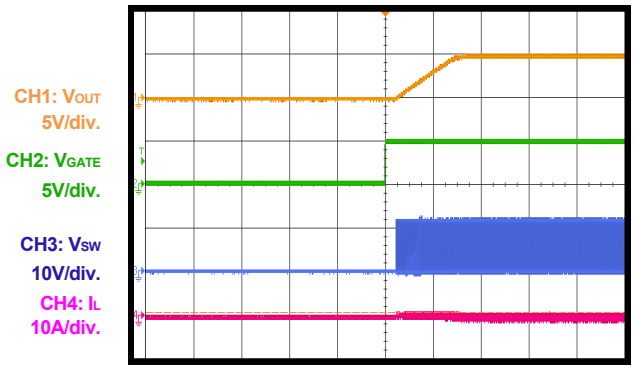
I_{OUT} = 0A



1s/div.

VOUT Short to USB_GND Recovery

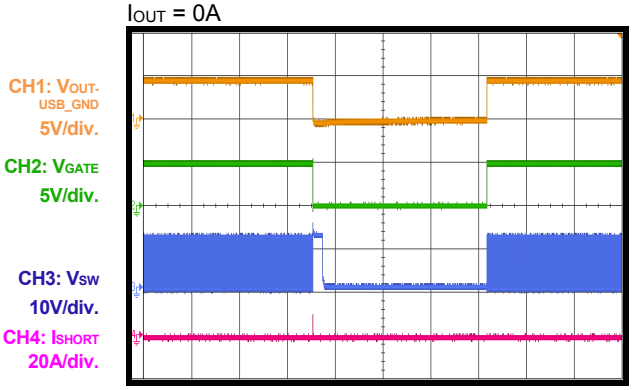
I_{OUT} = 0A



1ms/div.

USB_GND Short to Battery Entry and Recovery

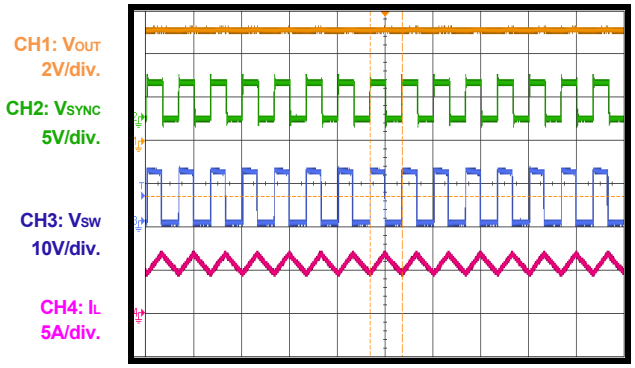
I_{OUT} = 0A



500ms/div.

Sync Function

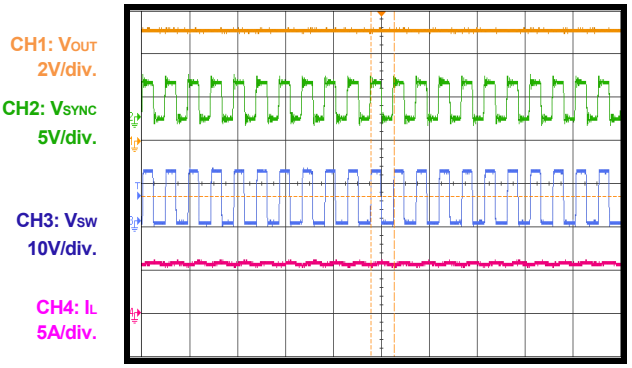
f_{SW} = 300kHz, L = 4.7µH, I_{OUT} = 6A



5µs/div.

Sync Function

f_{SW} = 2.1MHz, L = 2.2µH, I_{OUT} = 6A

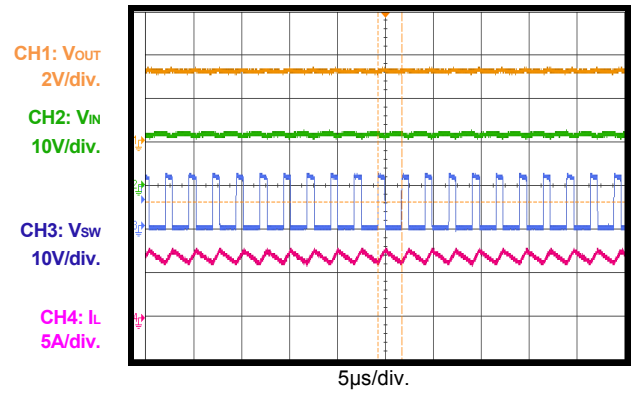


1µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

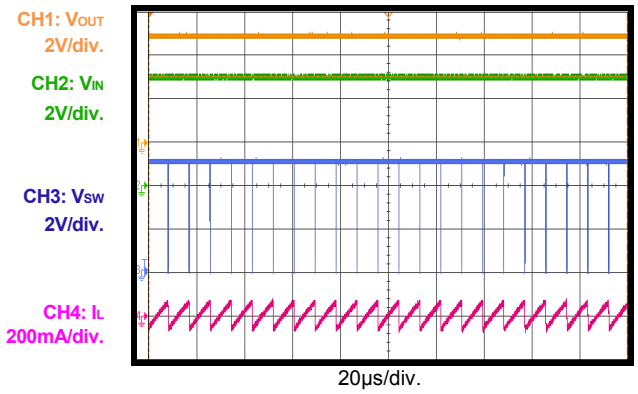
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted. All waveforms are tested based on bypassing the external MOSFET except Short Battery to Ground.

CC Mode Over-Current Protection Steady State



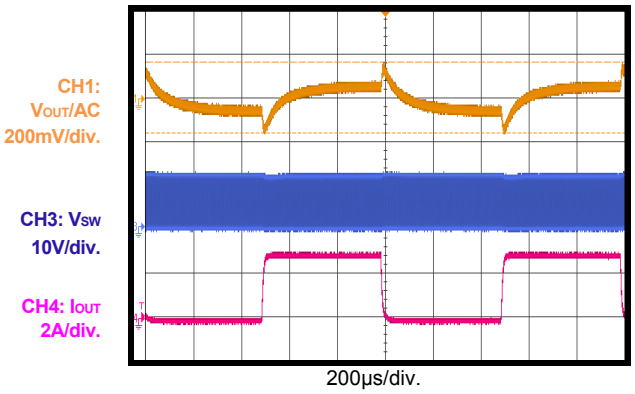
Low Dropout Mode

V_{IN} = 5V, V_{OUT} = 4.93V, I_{OUT} = 0A



Load Transient

I_{OUT} = 0 to 3A, 2.5A/µs, VDROP = GND,
line drop compensation = 73mV @ 3A



FUNCTIONAL BLOCK DIAGRAM

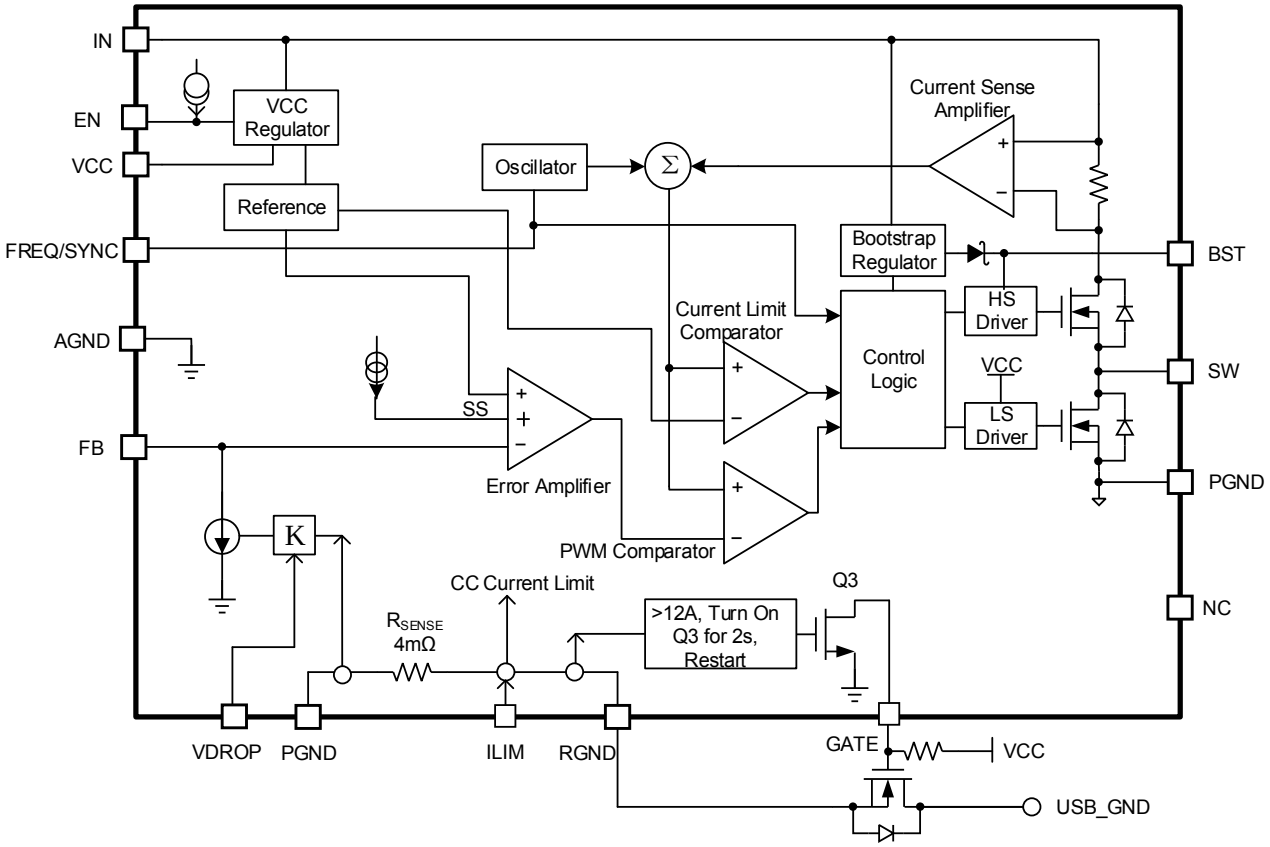


Figure 1: Functional Block Diagram

OPERATION

The MPQ4480 integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a compact solution to achieve 6A of continuous output current over a wide input supply range with excellent load and line regulation.

The MPQ4480 operates in a fixed-frequency, peak current mode control to regulate the output voltage. The internal clock initiates the PWM cycle, which turns on the integrated high-side MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle begins.

Low-Dropout Operation

The operation frequency auto-decreases when the input voltage is close to the output voltage, helping the part achieve a low dropout voltage.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal 1V reference (REF), and outputs a COMP voltage. This COMP voltage controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Internal VCC Regulator

The 5.05V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.05V, the output of the regulator is in full regulation. If V_{IN} is less than 5.05V, the output decreases with V_{IN}. VCC requires an external 1µF ceramic decoupling capacitor.

Enable Control (EN)

The MPQ4480 has an enable control (EN). There is an internal 7µA pull-up current, which allows auto start-up if EN is floated. Pull EN high or float to enable the IC; pull EN low to disable the IC. EN is clamped internally using a 7.6V series Zener diode and a 10V breakdown voltage ESD cell (see Figure 2).

It is recommended to connect EN to VIN and GND through divider resistors. When selecting a pull-up resistor, ensure that it is large enough to limit the current flow into EN to below 100µA.

For example, if the EN pull-up resistor is 100kΩ and the pull-down resistor is 110kΩ, the IC will power up when VIN exceeds the UVLO rising threshold.

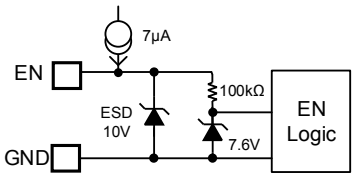


Figure 2: Zener Diode Between EN and GND

Setting the Frequency

Connect a resistor from FREQ to ground to set the switching frequency. The value of the frequency can be estimated with Equation (1):

$$FREQ(kHz) = \frac{1000}{0.04 \times R_{FREQ}(k\Omega) + 0.1} \quad (1)$$

Figure 3 shows the frequency vs. R_{FREQ}.

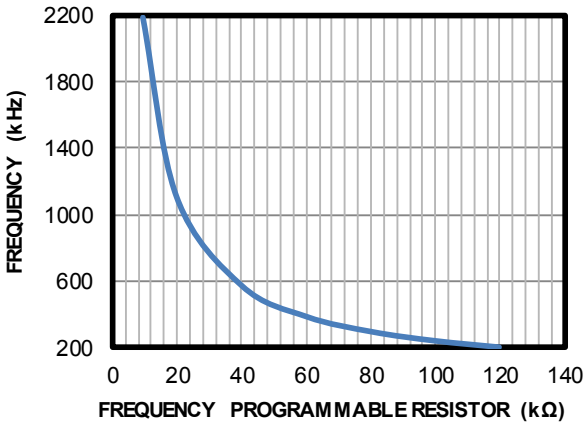


Figure 3: Switching Frequency vs R_{FREQ}

For the MPQ4480, the FREQ pin cannot be left floating or tied to VCC or GND. FREQ should be connected to GND through a resistor.

To avoid tripping the minimum on time limitation in high-frequency and high input voltage conditions, the MPQ4480 employs frequency foldback. When f_{SW} exceeds 1.2MHz and V_{IN} is above 15V, the device decreases the switching frequency gradually until the frequency falls to half of the setting value.

Frequency Spread Spectrum

The MPQ4480-FD is the switching frequency spread spectrum version of the MPQ4480. The purpose of spread spectrum is to minimize the peak emissions at a specific frequency.

The MPQ4480-FD uses a 4kHz triangle wave (rising 125μs, falling 125μs) to modulate the internal oscillator (see Figure 4). The frequency span of spread spectrum operation is ±10%.

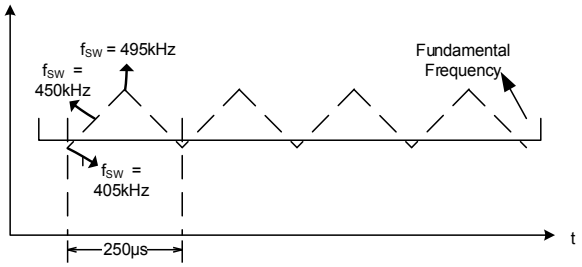


Figure 4: Frequency Spread Spectrum

The MPQ4480-FD frequency is only determined by internal trimming. It has no relationship with the FREQ pin's status.

Frequency Synchronizing

The MPQ4480 can be synchronized to an external clock with a range from 300kHz to 2.1MHz through the SYNC pin, in series with a 10pF capacitor. The internal clock rising edge is synchronized to the external clock rising edge. A typical SYNC input signal should have a <25% duty cycle.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 3.95V; its falling threshold is 3.45V.

Internal Soft Start (SS)

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 5.05V. When V_{SS} is lower than V_{REF}, the error amplifier uses V_{SS} as the reference. When V_{SS} is higher than V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is internally set to 1.1ms.

If the output of the MPQ4480 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

EN Shutdown Discharge

When EN is pulled low, the MPQ4480 enters output discharge mode. Meanwhile, the internal soft-start capacitor starts to discharge. The part remains in discharge mode until the soft-start capacitor discharges to very low.

In this mode, the low-side switch remains on until the low-side current reaches -2A, then turns on again after a clock cycle.

CC Mode Over-Current Protection

The MPQ4480 senses the ground current and uses this information to limit output current below a certain threshold. If I_{OUT} exceeds the set current-limit threshold, the MPQ4480 enters constant current limit mode (CC mode). In this mode, the current amplitude is limited. As the load resistance reduces, the output voltage drops until the feedback voltage falls below the under-voltage (UV) threshold (typically 30% below the reference).

Once UV triggers, the MPQ4480 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4480 exits hiccup mode once the over-current condition is removed.

In addition to the ground current limit, the MPQ4480 also has a high-side peak current limit.

Pulling the ILIM pin to GND, to VCC, or floating it can set three different CC current-limit thresholds.

Over-Voltage Protection (OVP)

The MPQ4480 monitors a resistor-divided feedback voltage to detect over-voltage. When the feedback voltage (V_{FB}) exceeds 115% of the target voltage, the controller enters a dynamic regulation period. During this period, the LS-FET remains on until its current goes to -2A. This discharges the output and tries to keep it within the normal range. If the OV still exists, the LS-FET turns on again after an 800ns delay. The part exits this regulation period when V_{FB}

falls below 105% of V_{REF}. During OV protection, if the input voltage reaches 40V, the MPQ4480 stops the OVP discharge function until V_{IN} drops to 38V.

RGND Short to Battery Protection

The MPQ4480 supports USB_GND short to battery protection. The USB_GND should be connected to the RGND through an N-MOSFET. The MPQ4480 senses the current from RGND to PGND, and the GATE pin is pulled low to turn off the N-MOSFET when the RGND-to-PGND current is above 12A. If RGND shorts to battery, the buck stops switching. When the battery short to ground is removed, the MPQ4480 resumes normal operation.

Output Line Drop Compensation

The MPQ4480 is capable of compensating an output voltage drop, such as high impedance caused by a long trace, to keep a fairly constant load-side voltage.

The MPQ4480 uses the sensed load current through the internal ground current sensing MOSFET to sink a current (I_{FB}) at the FB pin (see Figure 5).

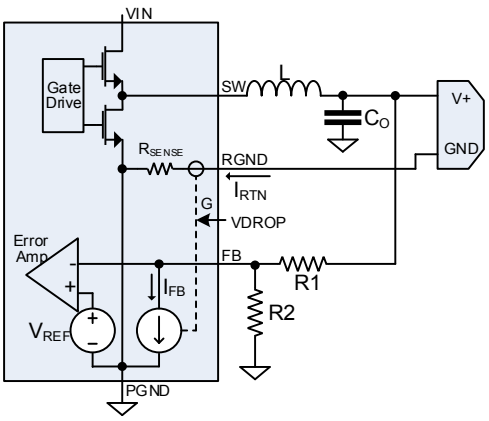


Figure 5: Output Line Drop Compensation Circuit

Calculate the feedback current with Equation (2):

$$I_{FB} = G \cdot I_{RTN} \quad (2)$$

V_O can be calculated with Equation (3):

$$V_{OUT} = \left(\frac{R_1}{R_2} + 1\right) v_{REF} + R_1 G \cdot I_{RTN} \quad (3)$$

The line drop compensation amplitude at certain output current condition is equal to R1 * G * I_{OUT}. The VDROP pin can program three gain levels, as the specification table shows.

The R1 value can also be used to adjust the line drop compensation amplitude. For example, at 3A output current, pull VDROP = 0 and select 40.2kΩ for R1 for the line drop compensation to be ~73mV (typically).

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V, with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} and VCC through D1, D2, M1, C4, L1, and C2 (see Figure 6). The BST capacitor (C4) voltage is charged quickly by turning on M1 when the low-side switch is turned on. The 2.5μA input to the BST current source also charges the BST capacitor when the low-side switch does not turn on.

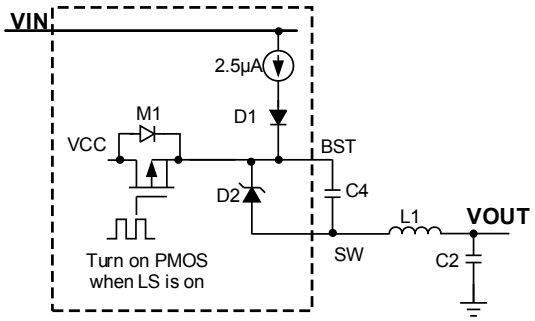


Figure 6: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, VIN low, and thermal shutdown. In shutdown, the signaling path is blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures.

When the silicon die temperature exceeds 165°C, it shuts down the entire chip. When the temperature falls below its lower threshold (typically 145°C), the chip is enabled.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 2). The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation capacitor. R2 is determined with Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{1V} - 1} \quad (4)$$

Figure 7 shows the external resistor divider.

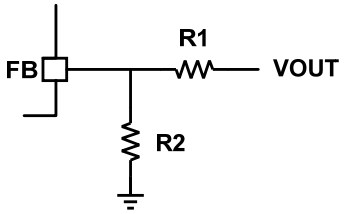


Figure 7: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
3.3	40.2	17.4
5	40.2	10
9	40.2	4.99

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. The inductor value for most designs can be calculated with Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be determined with Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Selecting the Buck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimal performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For CLA application, a 100µF electrolytic capacitor and two 10µF ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, which can be calculated with Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Selecting the Buck Output Capacitor

The MPQ4480 requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (10)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

For polymer capacitor designs, the ESR of output capacitor should be less than 50mΩ.

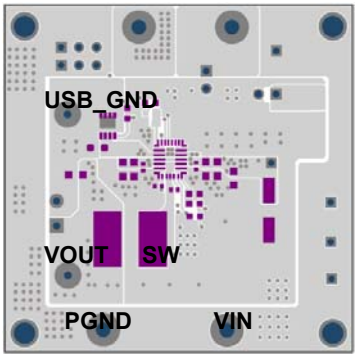
PCB Layout Guidelines [8]

Proper PCB layout is critical for efficient operation and thermal dissipation. For best results, refer to Figure 8 and follow the guidelines below:

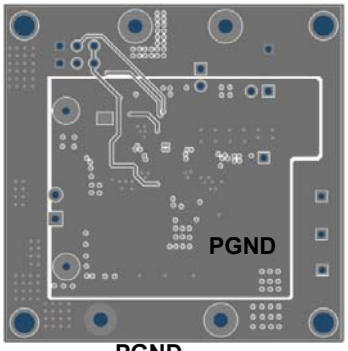
1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Use a large copper plane for PGND. Add multiple vias to improve thermal dissipation.
3. Connect AGND to PGND.
4. Ensure that FB is far from SW to avoid noise.
5. To improve EMI performance, place two ceramic input decoupling capacitors as close as possible to IN and PGND.
6. Place the VCC decoupling capacitor as close as possible to VCC.

Note:

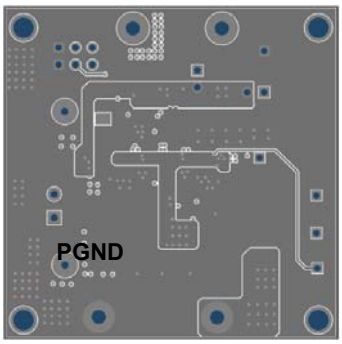
8) The recommended layout is based on the Typical Application Circuits on page 19.



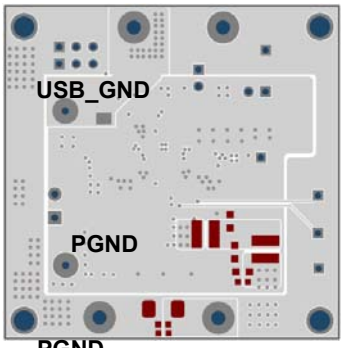
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 8: Recommend Layout

TYPICAL APPLICATION CIRCUITS

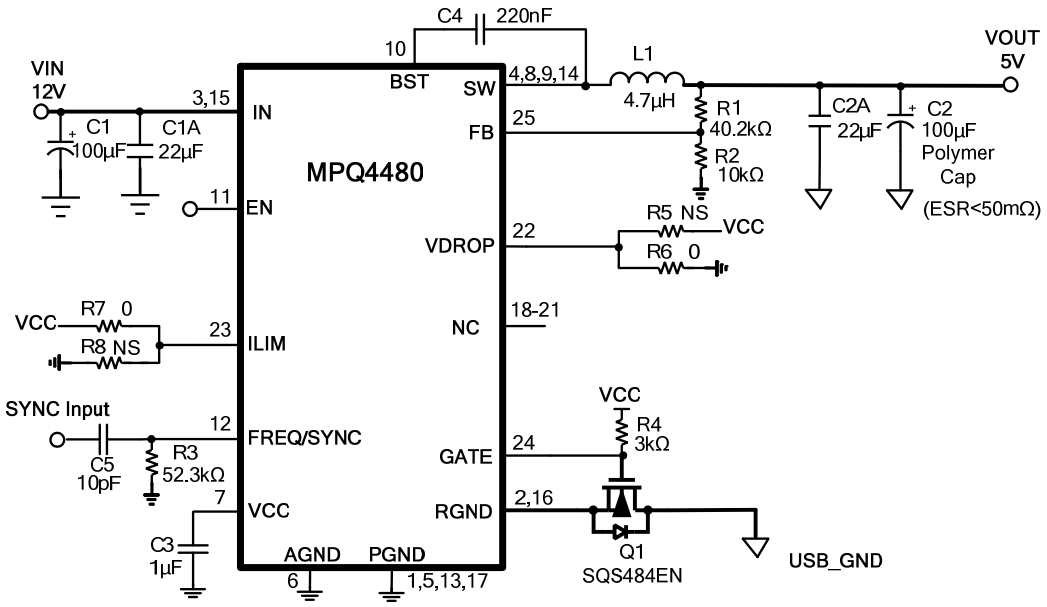


Figure 9: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, f_{SW} = 440kHz, with GND short to battery protection

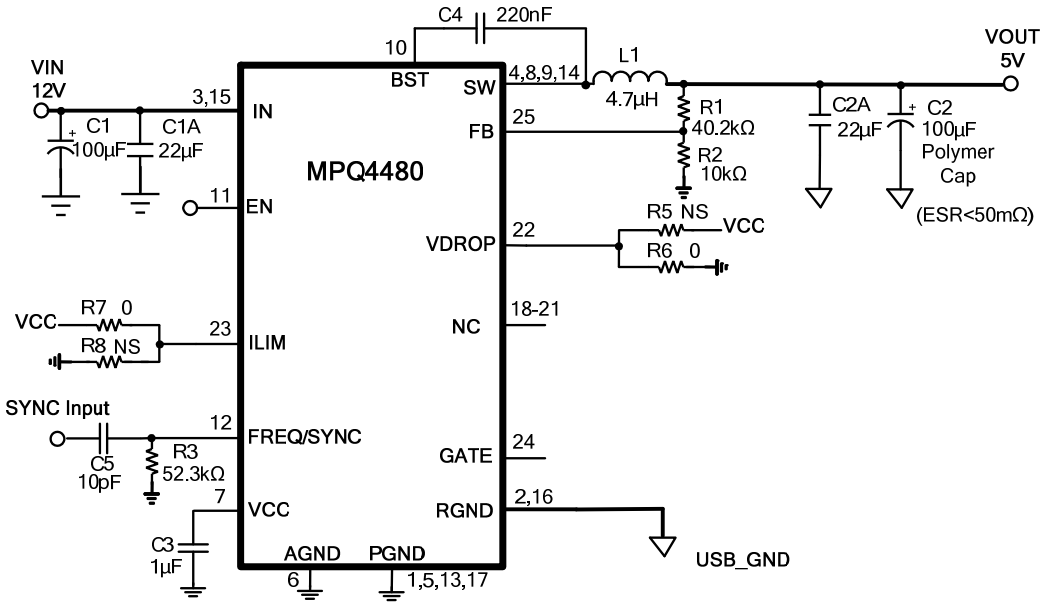


Figure 10: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, f_{SW} = 440kHz, without GND short to battery protection

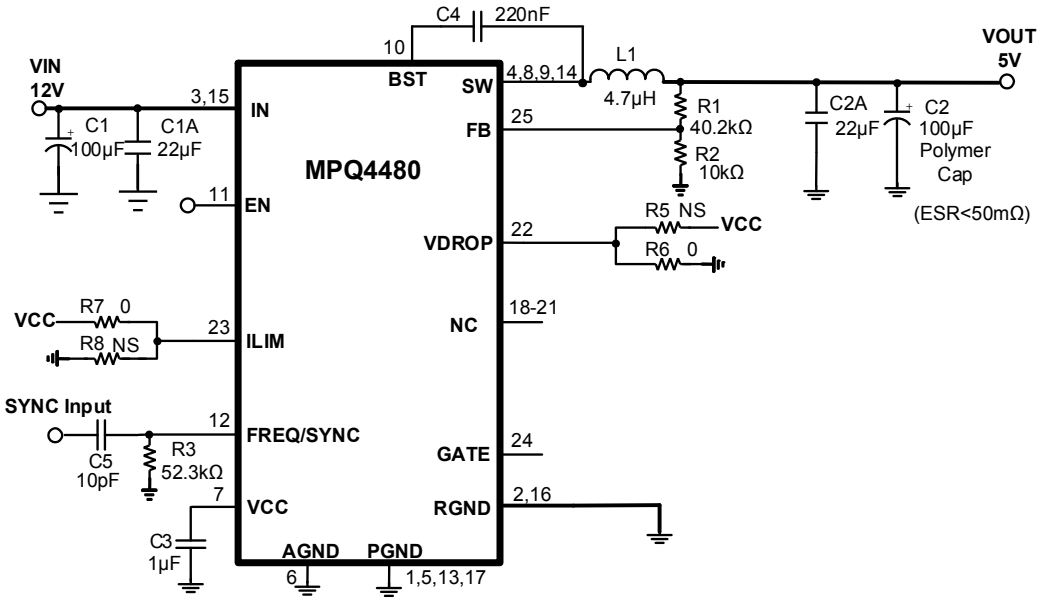


Figure 11: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, f_{SW} = 440kHz, without CC protection, only buck peak OCP

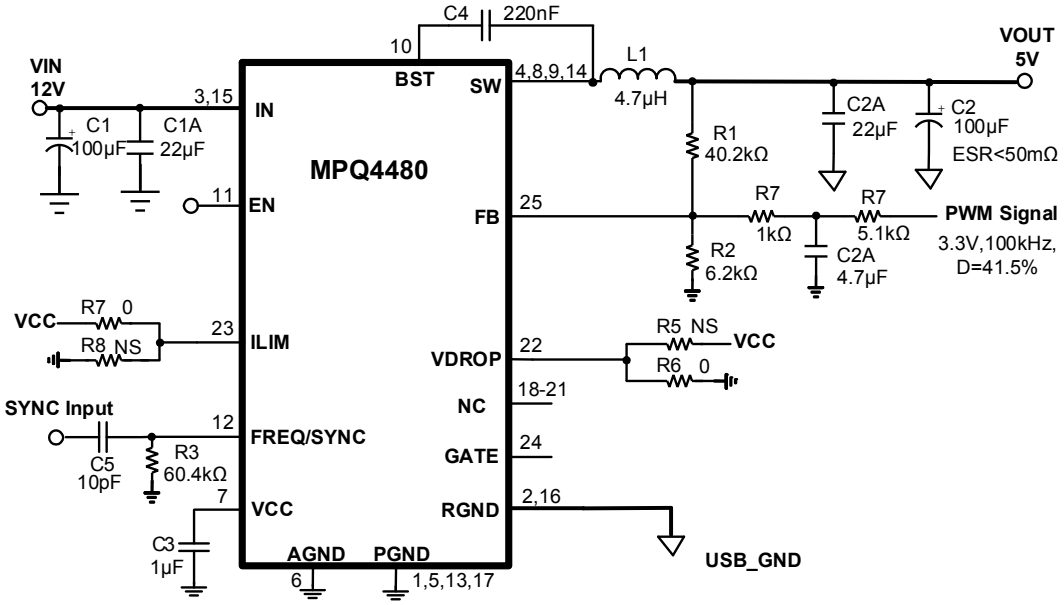
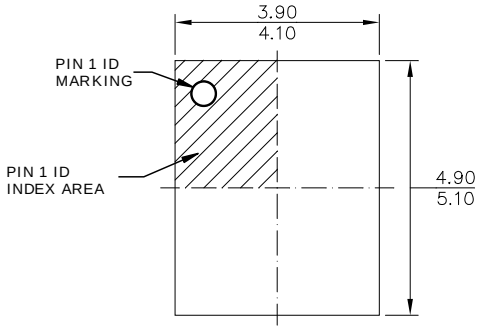


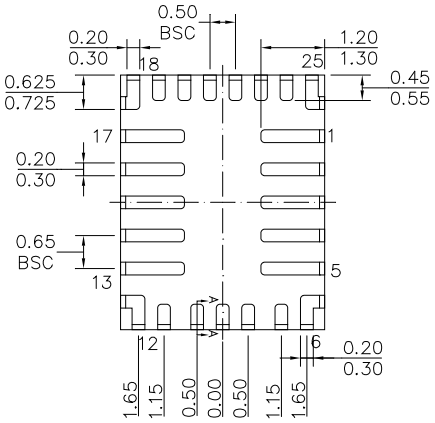
Figure 12: V_{IN} = 12V, V_{OUT} = 1V to 11V (5V default), I_{OUT} = 6A, f_{SW} = 380kHz, wireless charging application

PACKAGE INFORMATION

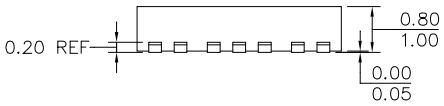
QFN-25 (4mm x 5mm)



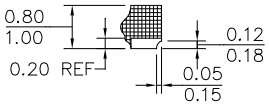
TOP VIEW



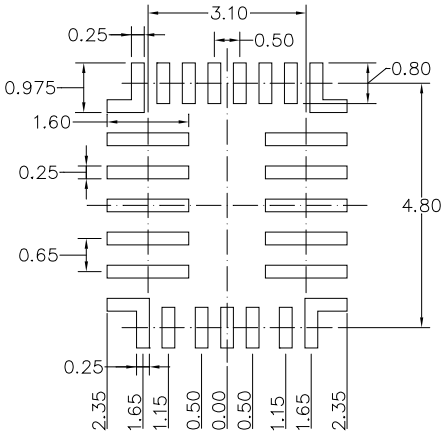
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:
1) THE LEAD SIDE IS WETTABLE.
2) LAND PATTERNS OF PIN1~5 AND 13~17 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.