8A3xxxx 72QFN

Evaluation Kit

The 8A3xxxx 72QFN EVK allows customers to evaluate Renesas' ClockMatrix devices (for example, 8A34005, 72QFN). This document discusses the following:

- The board's design, its power supply, and jumper settings
- The input and output connectors for normal operation
- How to bring up the board using the Timing Commander software GUI
- How to configure and program the board to generate standard-compliant frequencies

PC Requirements

- Renesas Timing Commander Software installed
- ClockMatrix GUI
- USB 2.0 or USB 3.0 interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available disk space: Minimum 600MB (1.5GB 64-bit); recommended 1GB (2GB 64-bit)
- Network access during installation if the .NET framework is not currently installed on the system

Kit Contents

- 8A34xxx 72QFN Evaluation Board
- USB Type A cable

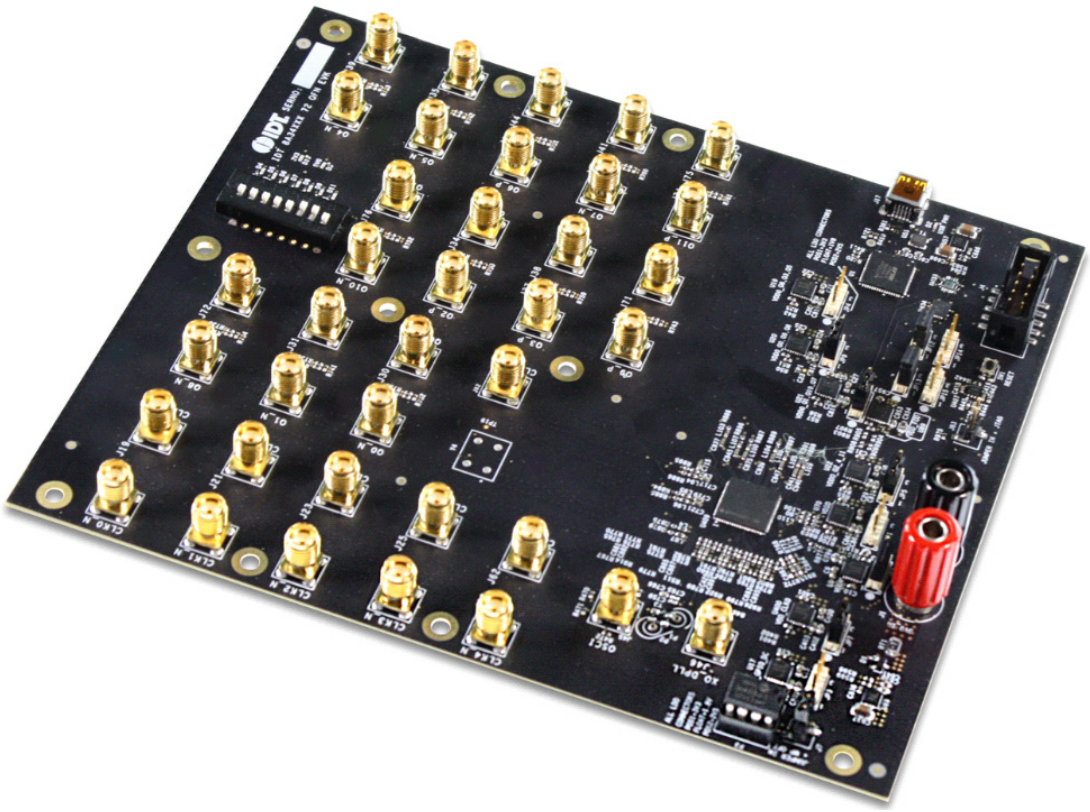


Figure 1. 8A3xxxx Evaluation Board

Contents

Figures

1. Board Design

The following diagram identifies the various components of the evaluation board: input and output SMA connectors, power supply jacks, and some jumper settings necessary for the board operations. Detailed descriptions are included below.

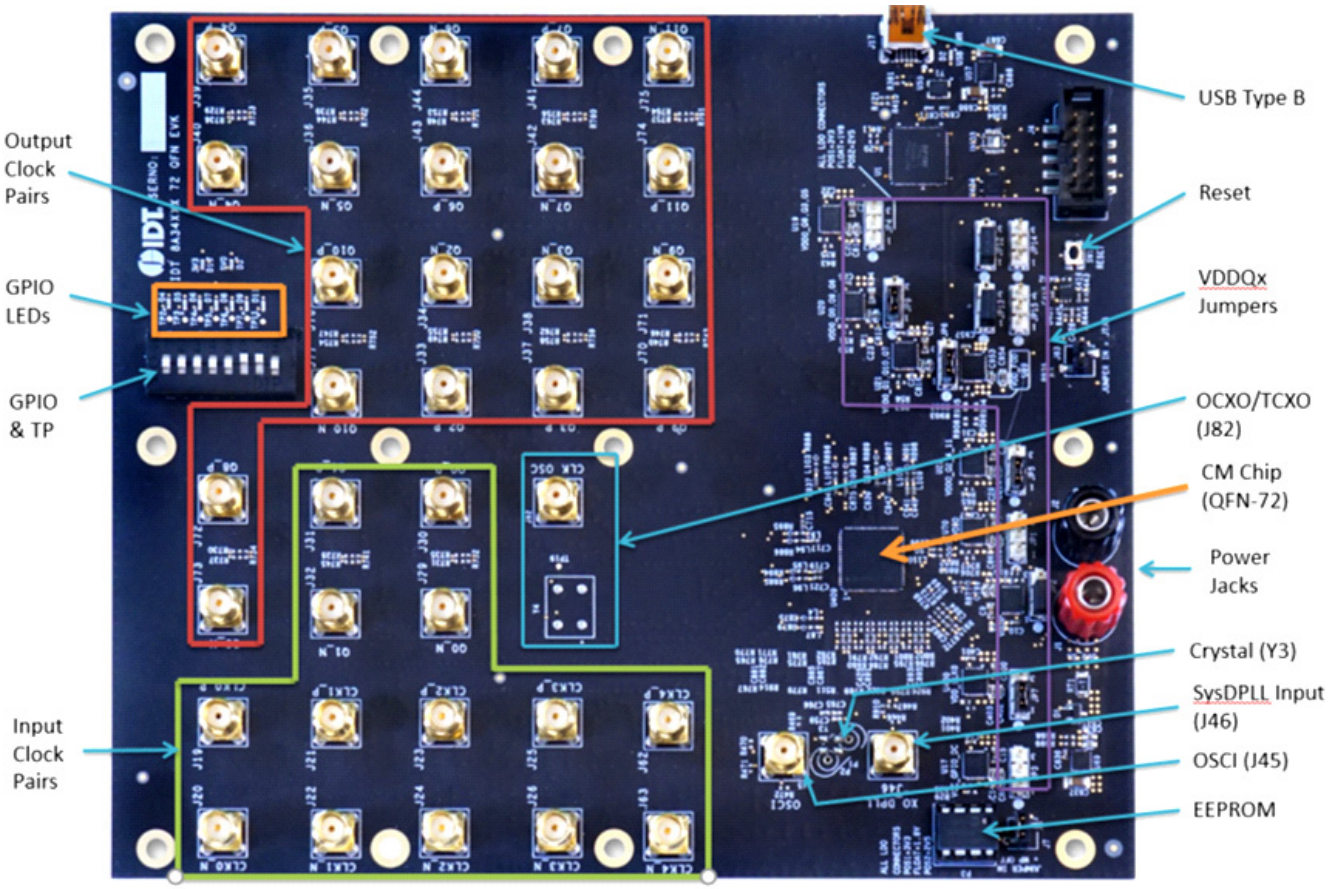


Figure 2. 8A3xxxx 72QFN Evaluation Board – Detailed

- **Input SMA connectors** – There are five differential inputs labeled CLK0/nCLK0 - CLK4/nCLK4. Each input clock can be configured differentially (LVDS, PECL 2.5V, and PECL 3.3V) or in single-ended format (CMOS).
- **Output SMA connectors** – There are 12 outputs labeled as Q0/nQ0 - Q11/nQ11. Each output clock can be configured differentially (LVDS, LVPECL, or user-defined amplitude) or in single-ended format (LVCMOS . in-phase or out-of-phase).
- **GPIO switch, LEDs, and Test points** – There are seven GPIOs available. Each GPIO can be set a “low” or “high” level (if input) or displayed with an LED (if output). Some GPIOs are used to set the chip in a certain working condition on power-up. For more information, see “Table 18. GPIO Pin Usage at Start-Up” in the 8A34005 datasheet.
- **USB connector** – A USB mini connector connects the evaluation board to a PC for GUI communications. No power is consumed from the USB connector other than to power the FTDI USB device.
- **VDDQx voltage selection jumpers** – Each output voltage can be individually supplied with 1.8V, 2.5V, or 3.3V. These jumpers are used to select the voltage for the output voltages.
- **Reset button**: A small button is used to reset the board.
- **OSCI Input connector** – An SMA connector, J45, is provided to optionally supply a clock signal to overdrive the crystal.
- **OCXO/TCXO Reference (Optional)** – An OCXO/TCXO footprint, output at J82. It can be connected to J46 (below) as the reference for System DPLL.

- **SysDPLL Input (Optional)** – An SMA connector, J46, is provided to supply a local OCXO/TCXO reference as an optional reference for System DPLL.
- **Crystal**: A crystal of various frequencies must be present for board operations. A 3225 footprint is provided for SMT crystals. For easy plug-in of a canned crystal, two through-holes are also available.
- **EEPROM** – An SO-8 socket is provided to hold an EEPROM device of compatible package. EEROM is used to store firmware and customer configuration data, if needed.

1.1 Board Power Supply

The board uses a single +5V supply for its power supplies. When running the board, please set the bench power supply at 5V/2A. The red jack (J1) is positive; the black jack (J2) is the ground.

Multiple LDOs are used to generate 3.3V, 2.5V, and 1.8V from the +5V supply.

1.2 Voltage Selection Jumpers

There are eight headers/jumpers to select different voltages for different functional blocks of the chip. Each header has pin 1 and 3 labeled in silkscreen – jumping pin 1 and pin 2 will select 3.3V; jumping pin 2 and pin 3 will select 2.5V; no jumper will have 1.8V. See the following example for JP4 and JP9 – JP4 will select 2.5V, JP9 will select 3.3V.

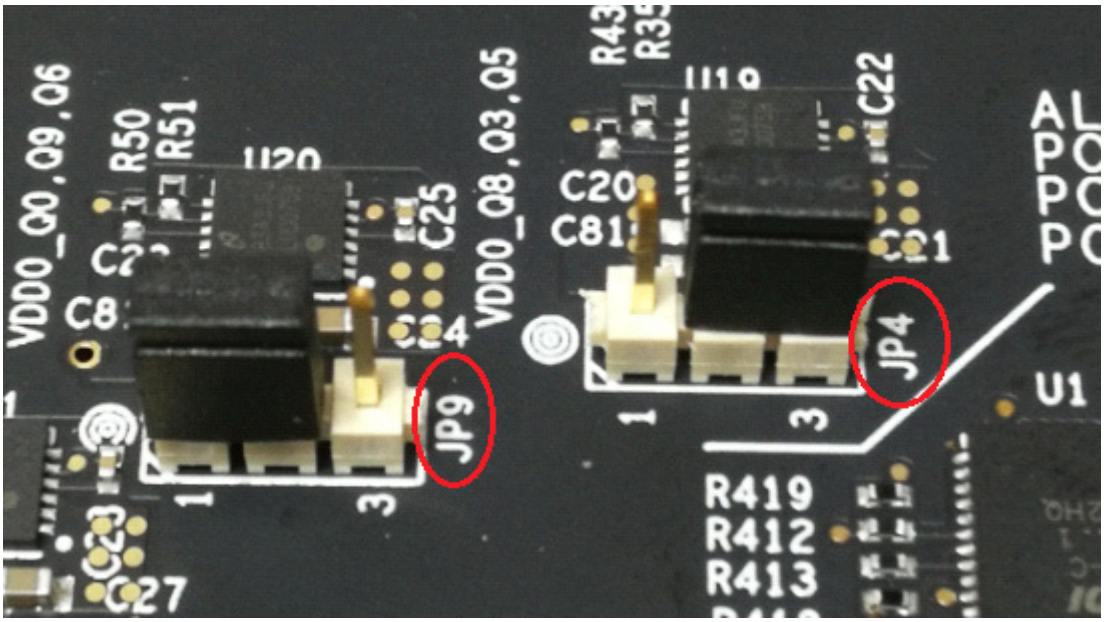


Figure 3. Example of Voltage Jumpers

The following list shows which head/jumper is used to select what voltage:

- JP1 - VDDD
- JP2 - VDDA
- JP3 - VCC_GPIO_DC
- JP4 - VDDO_Q8_3_5
- JP5 - VDDO_Q2_4_11
- JP6 - VDDO_1_10_7
- JP7 - VDD_CLK0
- JP9 - VDDO_Q0_9_6

Note: VDD_FOD voltage is selected by resistor R908 and R909. In order to prevent damage to the device, both R908 and R909 should not be stuffed, in which case VDD_FOD = 1.8V.

1.3 GPIO Switches, LEDs, and Test Points

An 8-bit dip switch sets the logic levels for seven GPIOs (GPIO0-5 and GPIO9). The GPIO levels for each setting and the corresponding LED state are listed in the following table (see picture and labels in Figure 4).

Table 1. GPIO Settings

Dip Switch Position	GPIO Logic Level	LED
Left	Low	On
Center	High if GPIO is configured as Input High or Low according to the GPIO output setting	High if GPIO is configured as Input High or Low according to the GPIO output setting
Right	High	Off

When the GPIOs are configured as outputs (such as User-Controlled or LOL indicator), the dip switch for the corresponding GPIO should be placed in the center position. The LED will indicate the state of the GPIO.

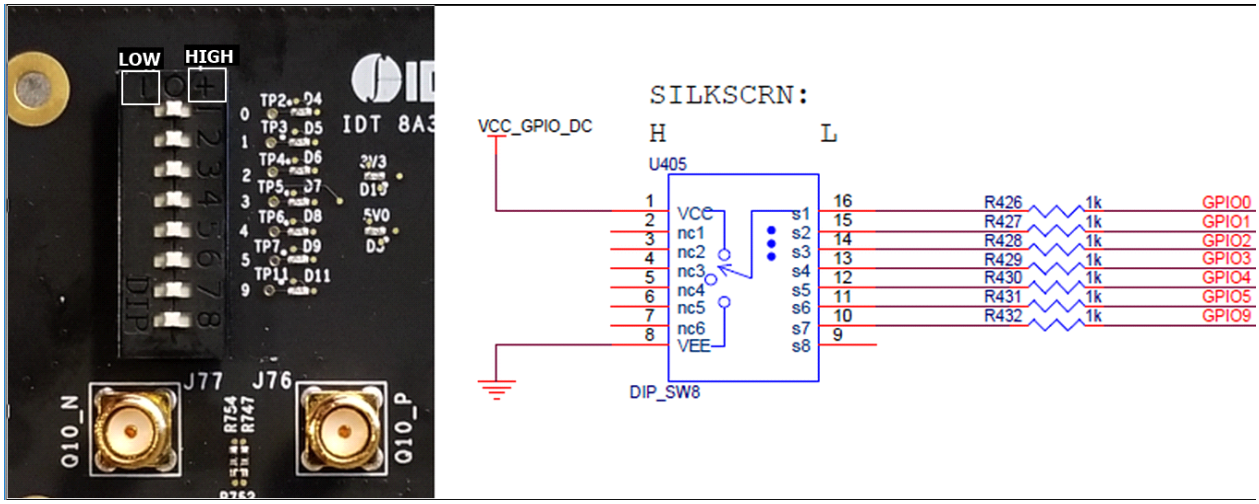


Figure 4. GPIO Setting and Status Display Area

1.4 USB Jack

The board has a USB mini-connector. The other end of the USB cable is a USB Type A connector going to a PC.

1.5 I2C between FTDI, CM Device, and On-board EEPROM

One of the major differences between the 72QFN and 144BGA144 chips is that there is only one serial bus on the 72QFN chip. The I2C bus between the FTDI chip and CM chip is the same bus between the CM chip and the on-board EEPROM. The on-board EEPROM is used to store device firmware and/or customer's configuration data. JP12 and JP13 must be jumped between pin 1 and 2 to enable the I2C connections.

Table 2. EEPROM I2C Connections

	JP12/JP13	JP12/JP13
Jumper Position	Pin 1 and 2	Pin 2 and 3
EEPROM I^2C Path	FDTI and CM Chip; CM Chip and EEPROM	N/A

2. Working with Timing Commander™ for Programing / Configuration

The following sections are best cross-referenced with the *ClockMatrix GUI Step-by-Step User Guide* that is available on the ClockMatrix Timing Solutions page and various ClockMatrix device product pages.

2.1 Default Operation

The board can operate off an EEPROM that has stored all information including firmware and a default configuration data. A default operation provides a sanity check on the board before running the board through the Timing Commander tool. Set the board in the following default conditions (for jumper and switch positions, see Figure 5):

- Set all the GPIOs to the center position. This will ensure that GPIO9 is high and that the serial port is configured for I2C 1 byte addressing.
- VDDA = 3.3V, VDD_ FOD = 1.8V, and VDDO_Qx = 3.3V
- Crystal frequency = 50MHz
- CLK0 = 25MHz
- FTDI, CM device, and EEPROM share the same I2C bus by jumping Pin 1 and 2 of JP12 and JP13

With the above default conditions ready, connect the board to the PC using a USB cable (type A on the PC side and mini-type on the board side), and power up the board using a single +5V supply. On power-up, the ClockMatrix device will read its firmware and configuration data from EEPROM and update all registers. When this process is completed, the following frequencies are available:

- Q0 = 122.88MHz
- Q1 = 122.88MHz

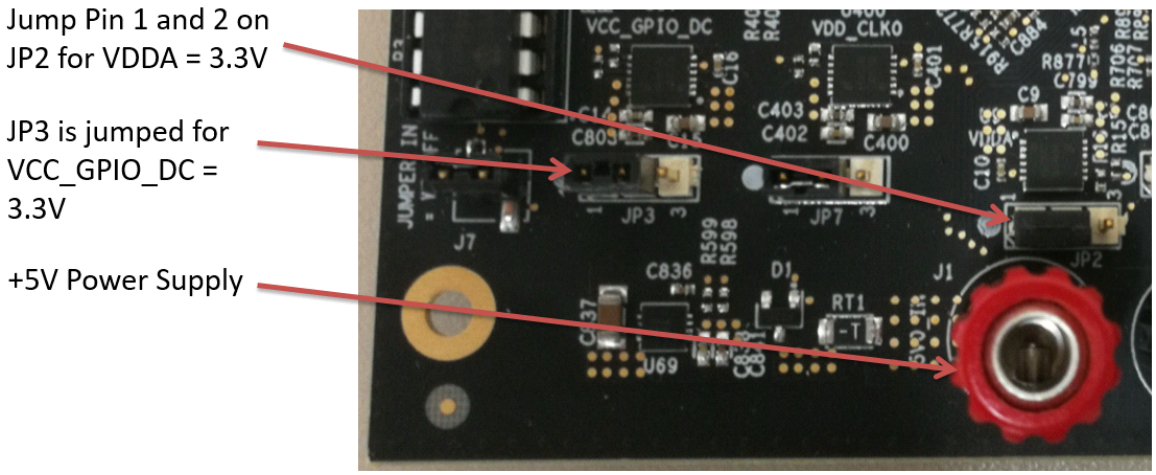


Figure 5. Board Setting for Default Operation

Note: In order to set GPIO9 to “High”, the switch for GPIO9 must be set either to the “+” (high) position or the center position (see Figure 4).

2.2 Using Timing Commander to Control the Board

Once the default operation is successful, complete the following steps to configure and program the ClockMatrix device per your specific application requirements using Timing Commander GUI tools:

1. Power up the board and set the main serial port in I2C mode by GPIO9 = “high”. Connect the board to the PC.
2. Start the Timing Commander software.

   You will see options of “New Setting File” and “Open Setting file”. For a new configuration, select “New Setting File”.

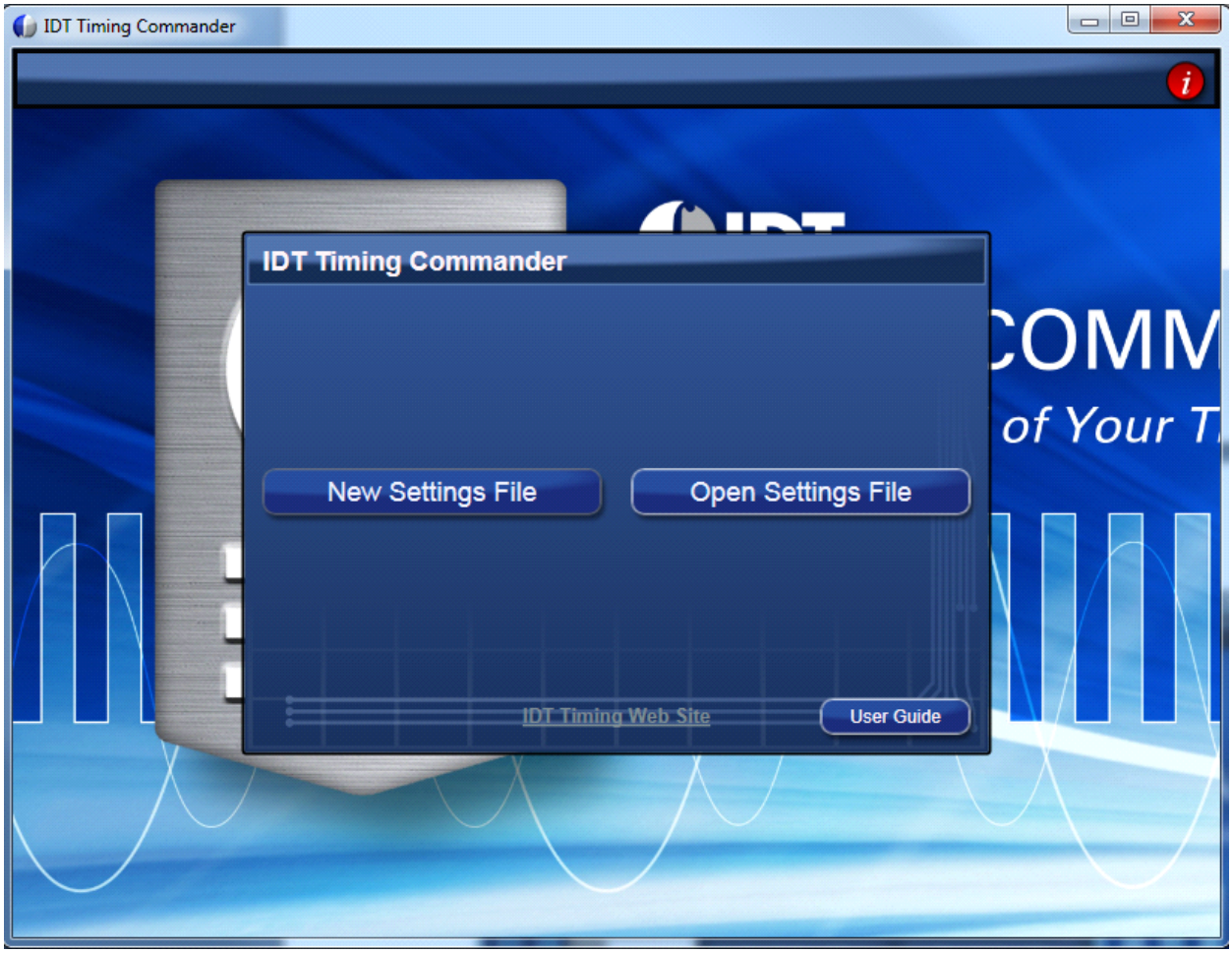


Figure 6. Starting Up Timing Commander GUI

3. After selecting “New Settings File”, a device selection window will pop up (see Figure 7). In the window, choose the intended device in the list (in this example, 8A34001 is selected).

   Click the button at the lower right corner of the window (red circle) to browse and select the correct personality file (in this example, personality Version 4.6 is selected), then click OK.

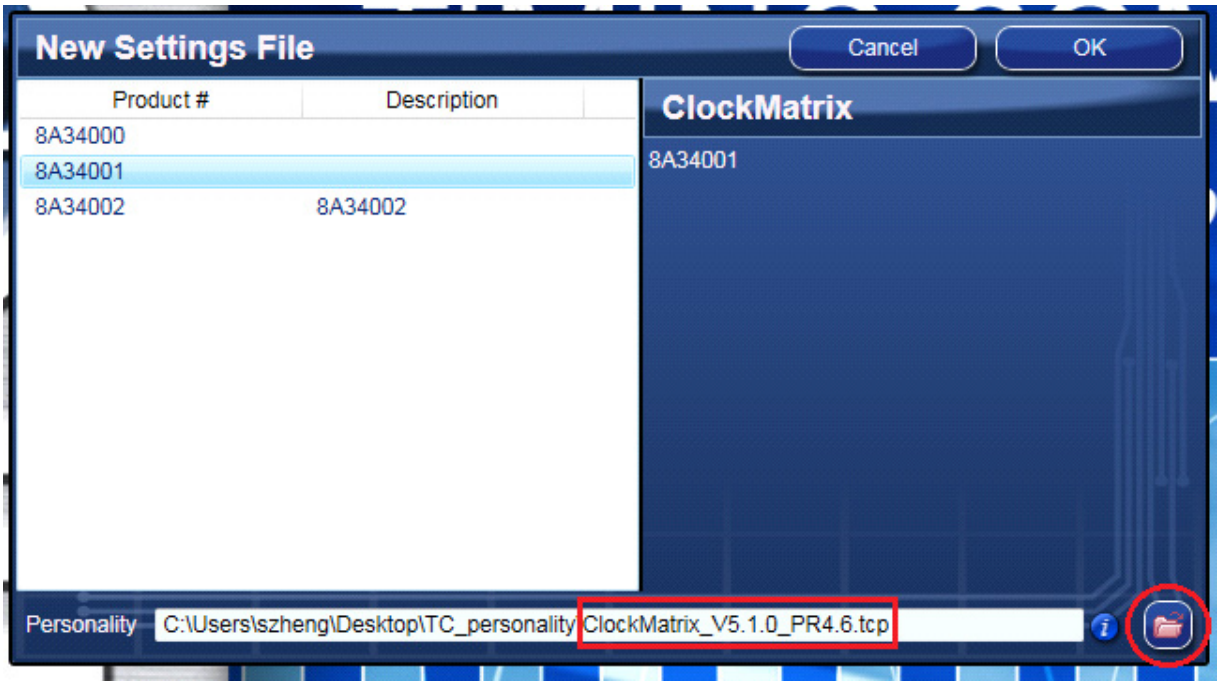


Figure 7. Selecting 8A34001 using Personality File v4.6

4. The GUI window with the 8A34001 block diagram will open for configurations; or if “Open Settings File” is selected in Step 3 above, you will be prompted to browse and select an existing .tcs file and the personality file. When the configuration file is open, all configured values will be displayed as in Figure 8.

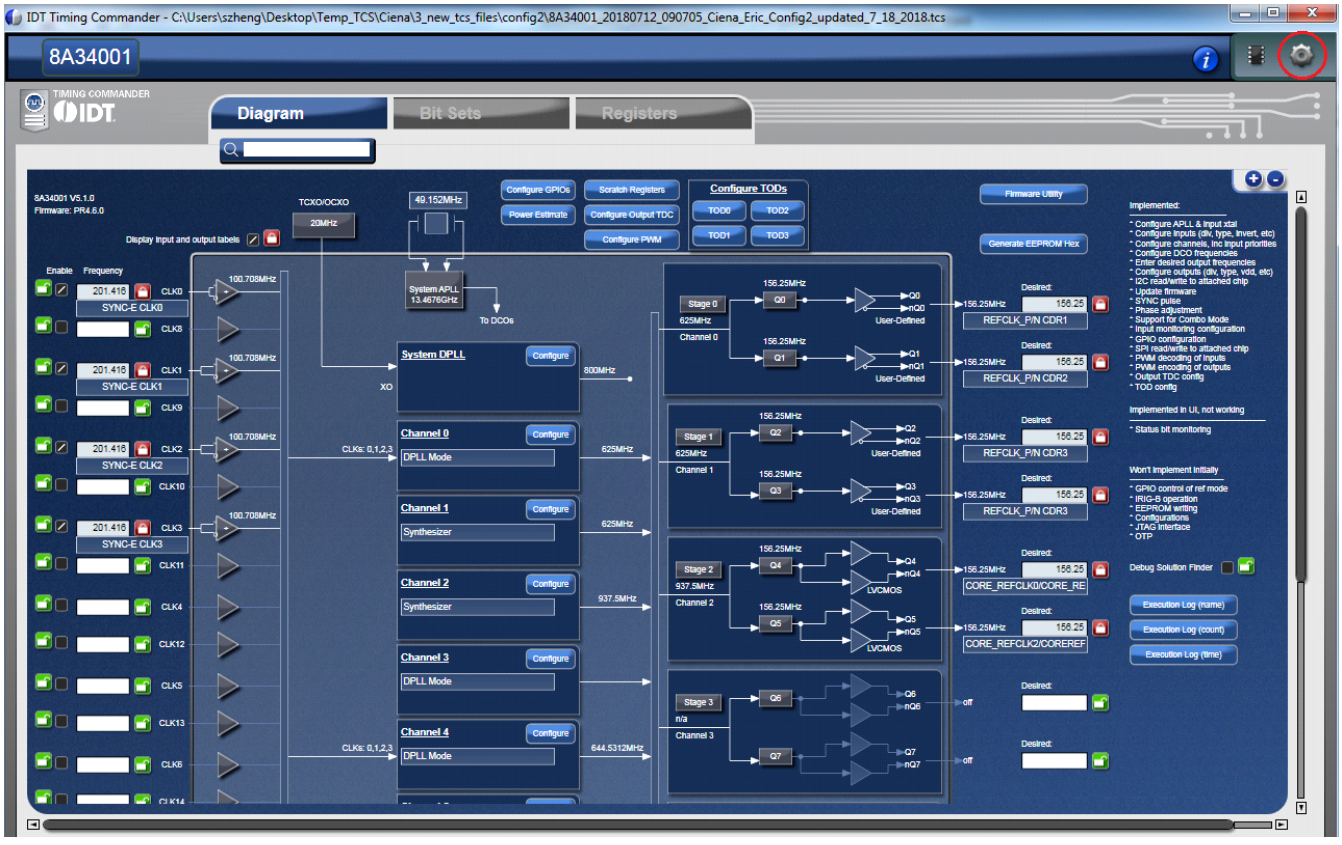


Figure 8. Timing Commander GUI with a Settings File Opened

5. In order to connect the board with Timing Commander (PC), click the button (red circle) at the up-right corner of the GUI to set up the communication protocols (see Figure 8). After I2C and one-byte addressing are selected, click OK to close the window (seeFigure 9).

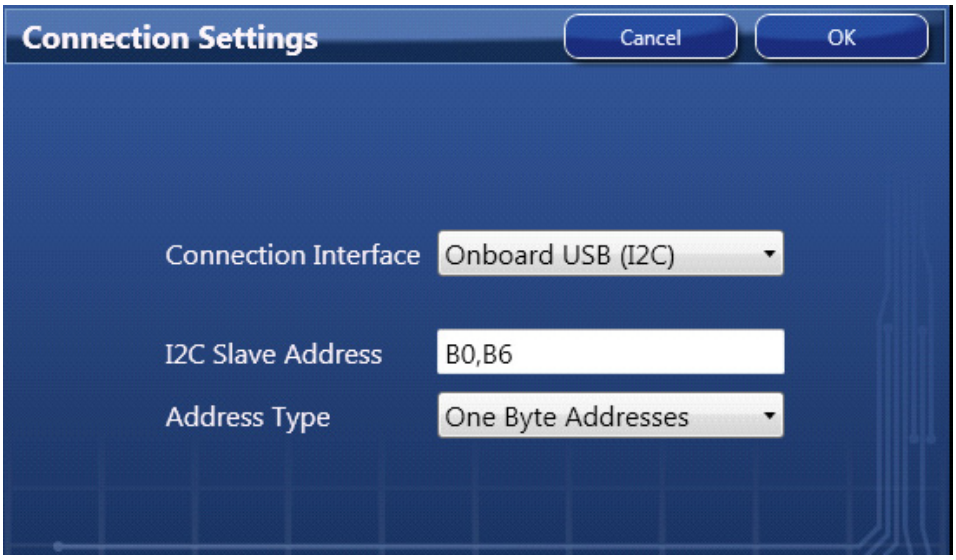


Figure 9. Setting I2C for Connecting the Board with GUI

6. Click on the chip symbol at the upper-right corner of the GUI window to initiate the connection. The connection is valid when a green band appears at the upper-right corner of the window, as shown in Figure 10.

Figure 10. A Green Band Appears when a Valid Connection is Made

7. If ClockMatrix device's firmware, or firmware loaded from EEPROM, has a different version from that in the Personality file, a firmware version mismatch warning message will appear (see Figure 11). Click "Close" button to close the message window and a connection is made.

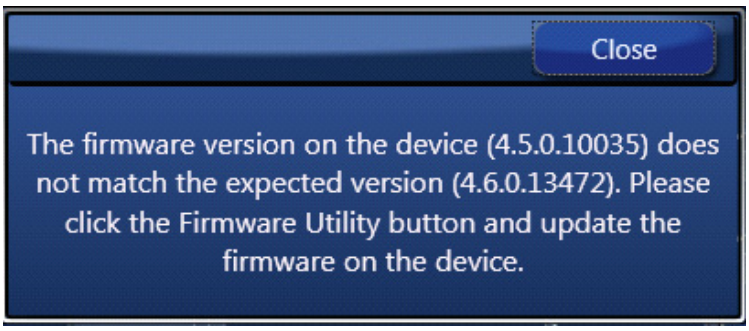


Figure 11. Firmware Version Mismatch Warning Message

8. Once the connection is made, the firmware version can be read within the GUI. Click the “Firmware Utility” button to bring up the Firmware Utility window, as shown in Figure 12.

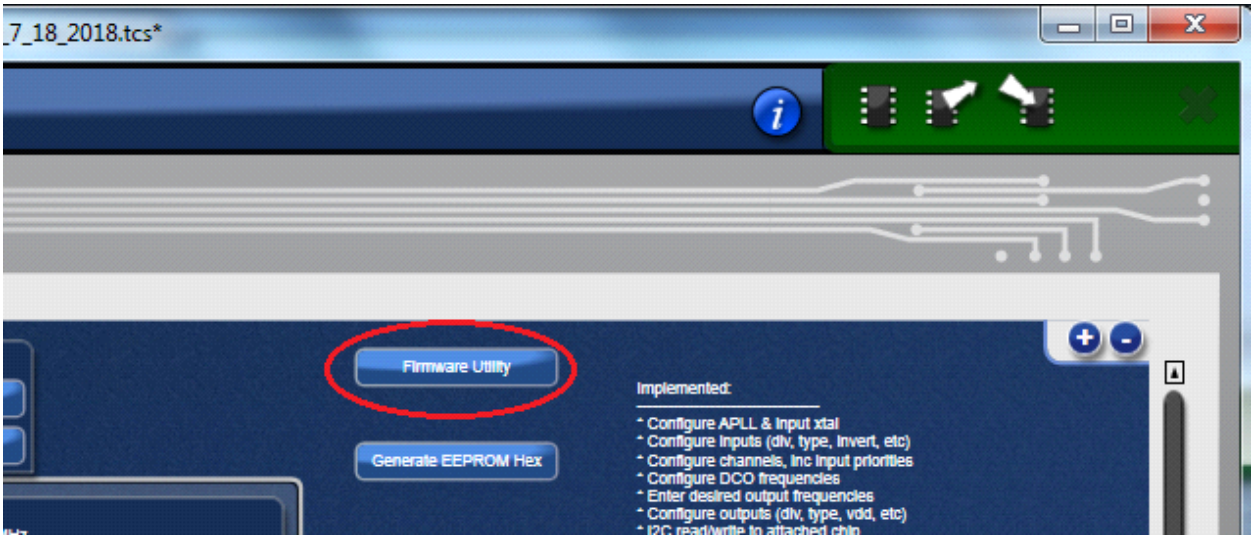


Figure 12. Reading Firmware Version

9. Within the Firmware Utility window, click the “Get Firmware Version” button to read the firmware version.

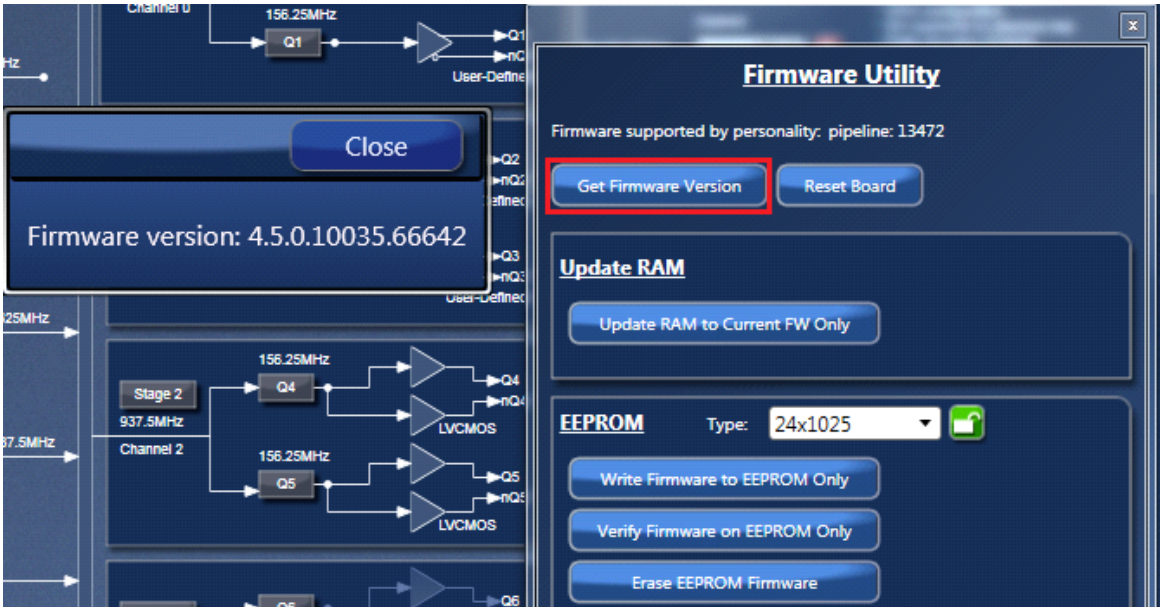


Figure 13. Read Firmware Version of ClockMatrix Chip

10. In the case where the firmware version mismatches each other, a firmware upgrade is necessary to update the device's firmware. To update the device's firmware, complete the Firmware Version Update steps in Appendix A: How to Upgrade the Firmware.

2.3 Output Terminations and Rework to Take 1PPS Input

All outputs are terminated with a 100Ω resistor across the output pair. This is the recommended termination regardless of the Voffset and Vswing settings. Since the outputs are DC-coupled, they will support a 1PPS output without any need for rework.

Note: When connecting the outputs to measurement equipment, use a DC-block to ensure that the output operates at its intended Voffset; otherwise, the equipment may load the output down and cause degraded performance.

The following rework must be implemented in order to support a 1PPS input clock. All input clocks for the evaluation board are AC-coupled and terminated as in

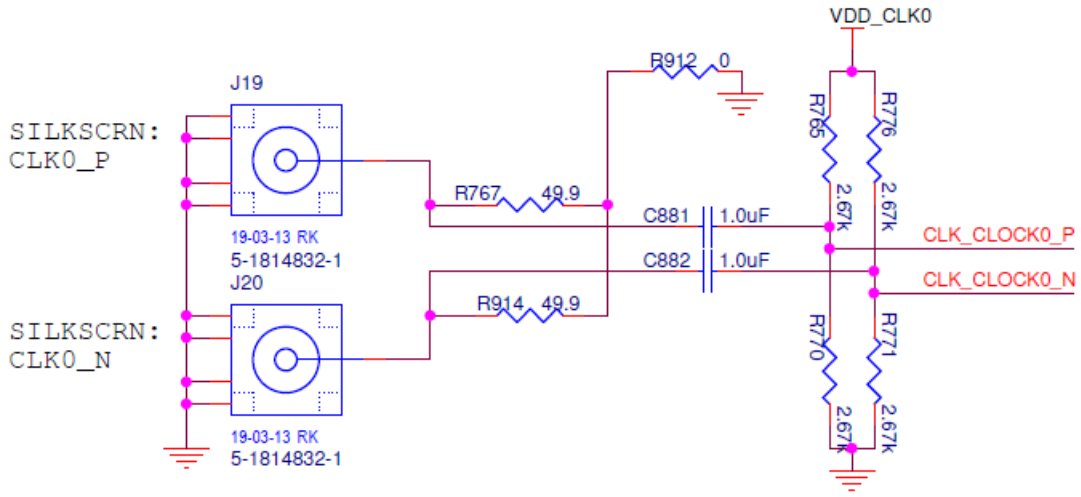


Figure 14. Input Clock's AC-Coupling and Terminations

For a 1PPS input, a single-ended input with DC-coupling is recommended. As such, the populated AC-coupling capacitor must be removed and the input must be configured as LVCMOS, not differential. In Figure 14, to make CLK0 supportive of 1PPS input, first configure CLK0 as LVCMOS in Timing Commander (see Figure 15)

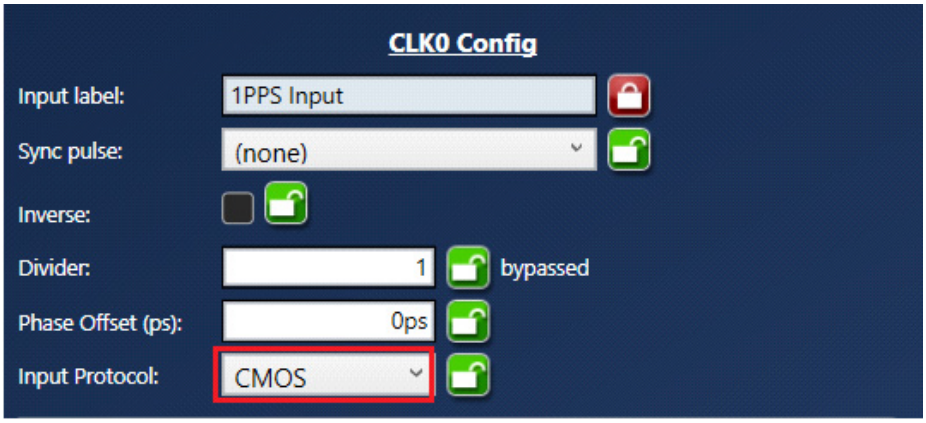


Figure 15. Configuring CLK0 as CMOS to Receive a 1PPS Input

Once in LVCMOS mode, CLK0_P and CLK0_N will be two separate LVCMOS inputs instead of a differential pair. To make CLK0_P receive a 1PPS input, replace C881 with a 0Ω resistor, while at the same time, remove R765 and R770.

3. Schematics

Schematic diagrams are located at the rear of the document.

4. Ordering Information

Part Number	Description
8A34044-EVK	8A3xxxx 72QFN Evaluation Kit

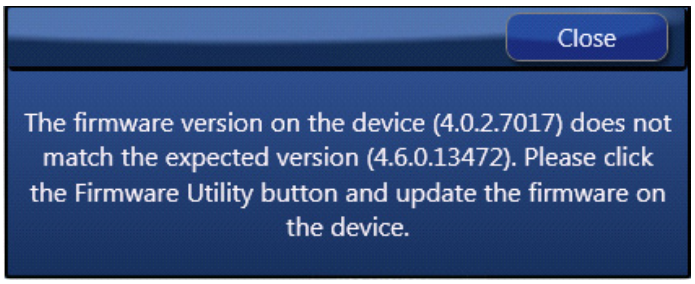
5. Revision History

Revision	Date	Description
1.01	Apr 26, 2022	▪ Added updated Schematics. ▪ Reformatted to the latest template.
1.00	Feb 14, 2019	Initial release

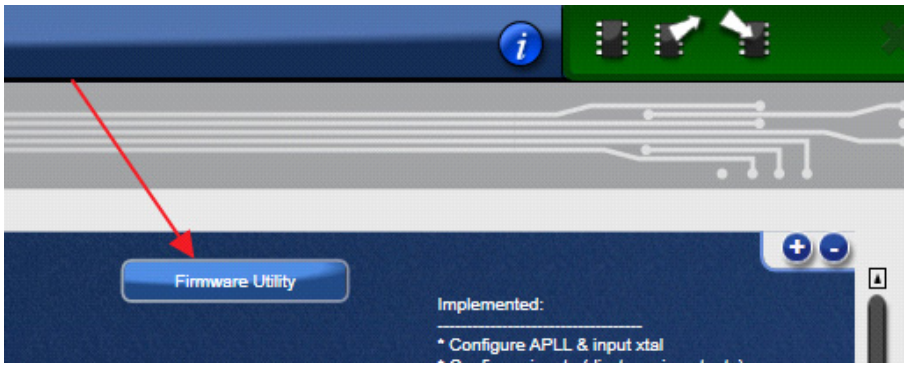
Appendix A: How to Upgrade the Firmware

Upload Firmware to the RAM

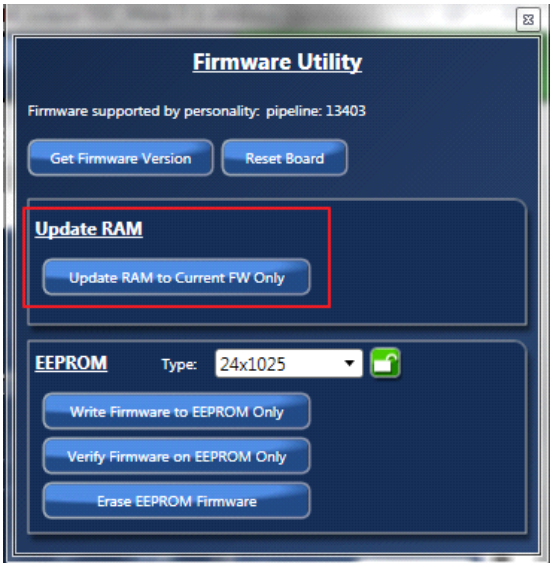
1. Connect to the EVB.
2. Power up the EVB with no EEPROM present. This ensures the firmware is 4.0.2.7017.
3. The GUI will indicate that the firmware on the chip does not match the GUI firmware. Press “Close”.



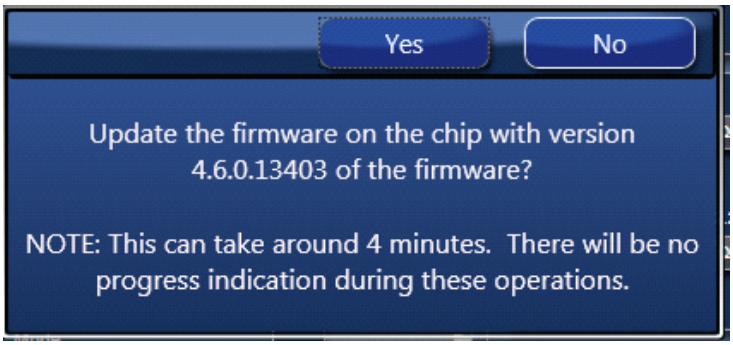
4. Open the “Firmware Utility” window.



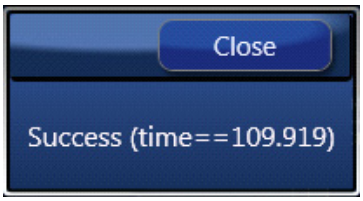
5. Update the Firmware first. Press “Update RAM to Current FW Only”.



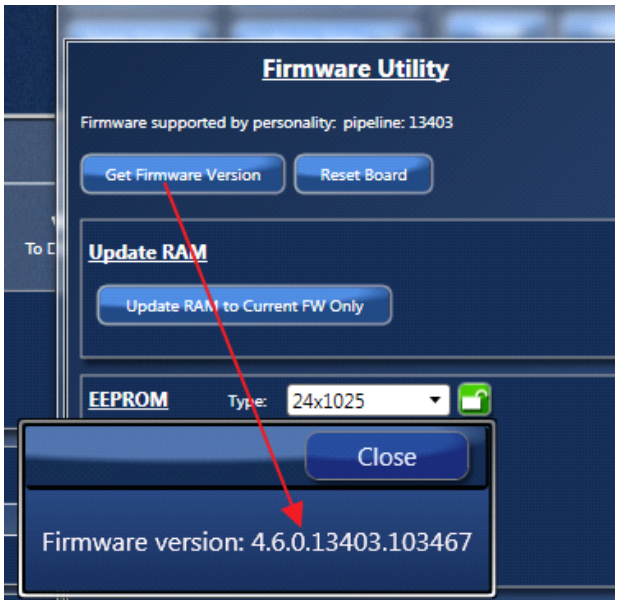
6. In the next dialog window, press “Yes” and wait approximately 3–4 minutes.

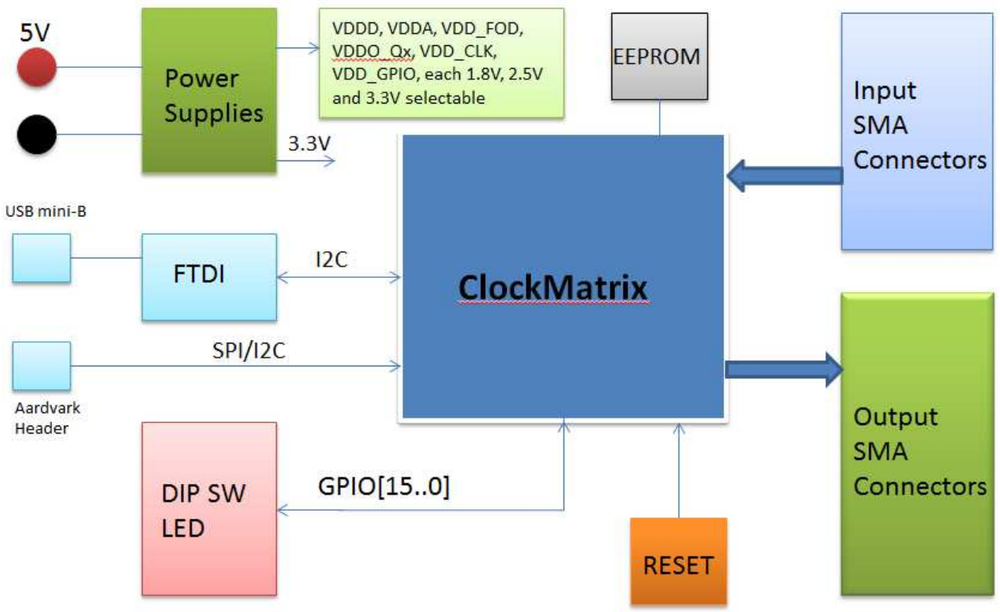


7. Once the FW updates, a dialog window will indicate a successful update. Click “Close”.



8. Press “Get Firmware Version” to verify that the RAM was updated correctly. When verified, click “Close”.





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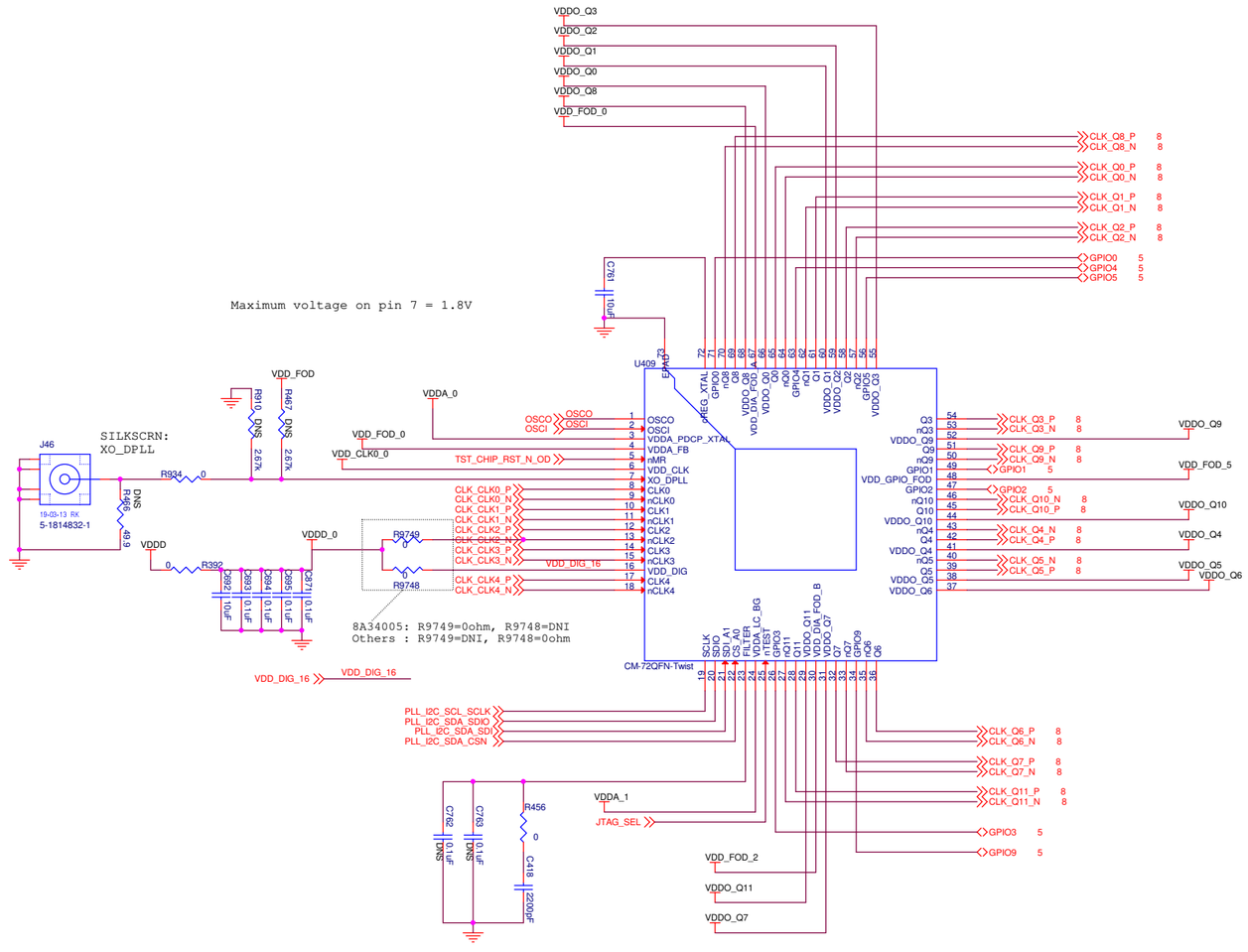

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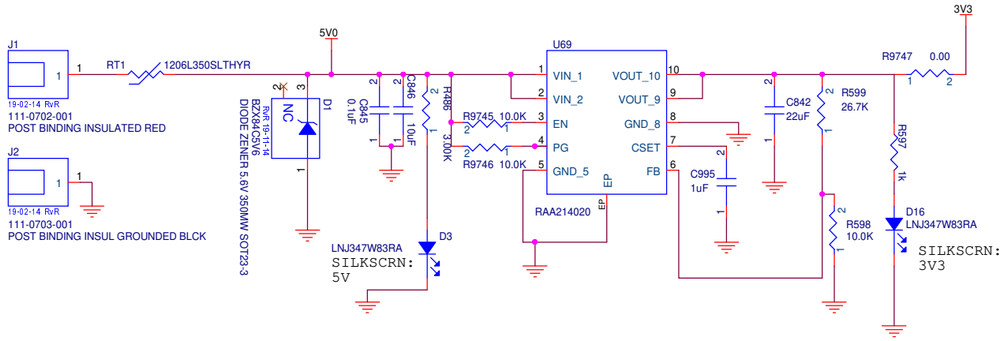
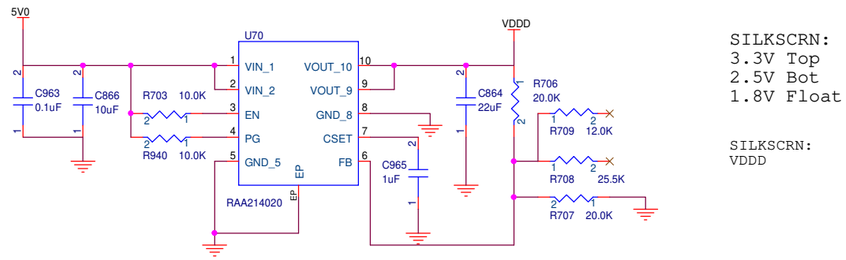
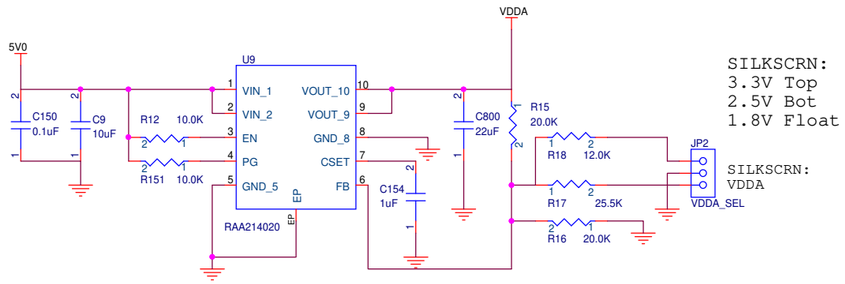
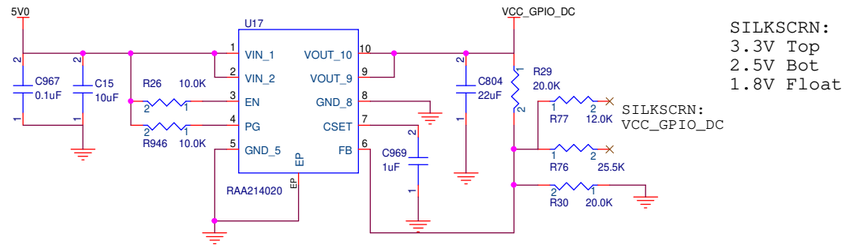
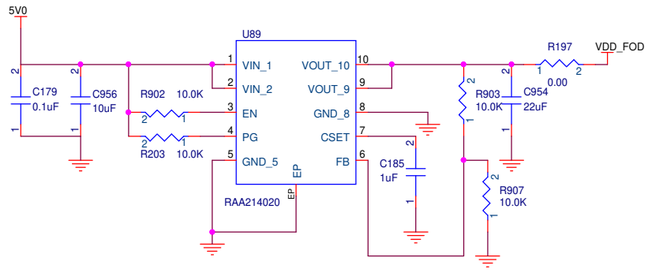
Board 3V3











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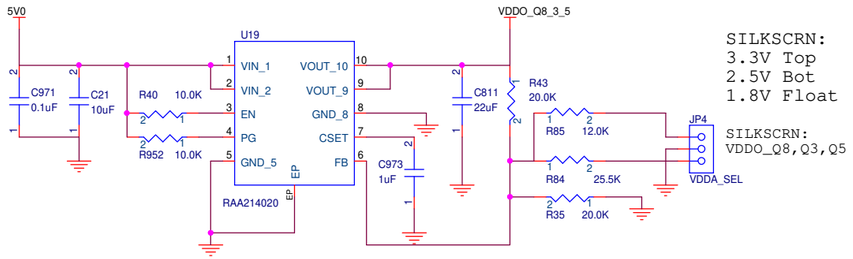

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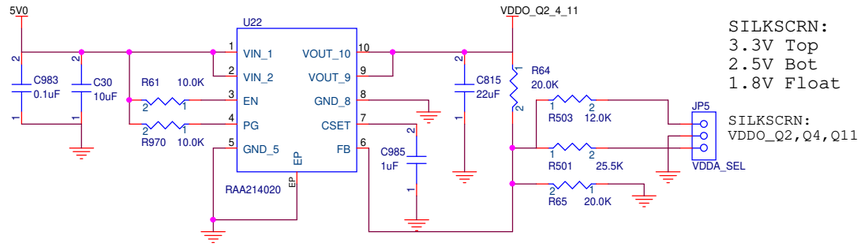
2.5V Bot
1.8V Float

SILKSCRN:
VDDO_Q8,Q3,Q5



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1.8V Float

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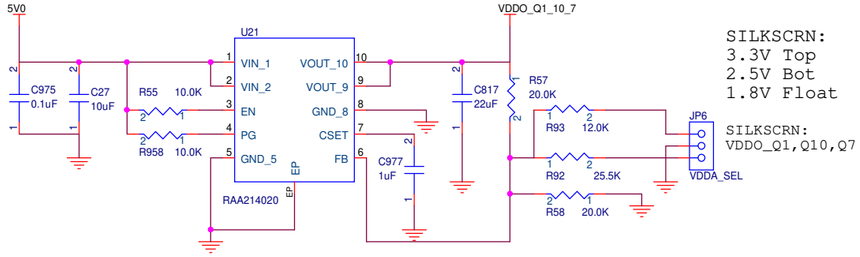

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1.8V Float

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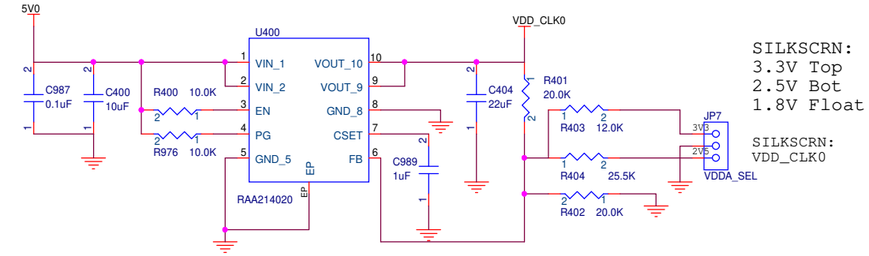

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1.8V Float

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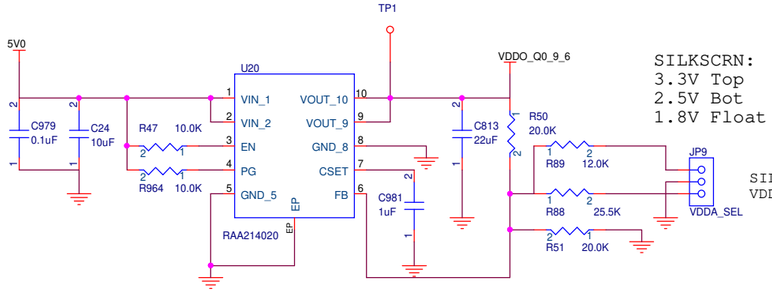

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2.5V Bot
1.8V Float

SILKSCRN:
VDDO_Q0,Q9,Q6

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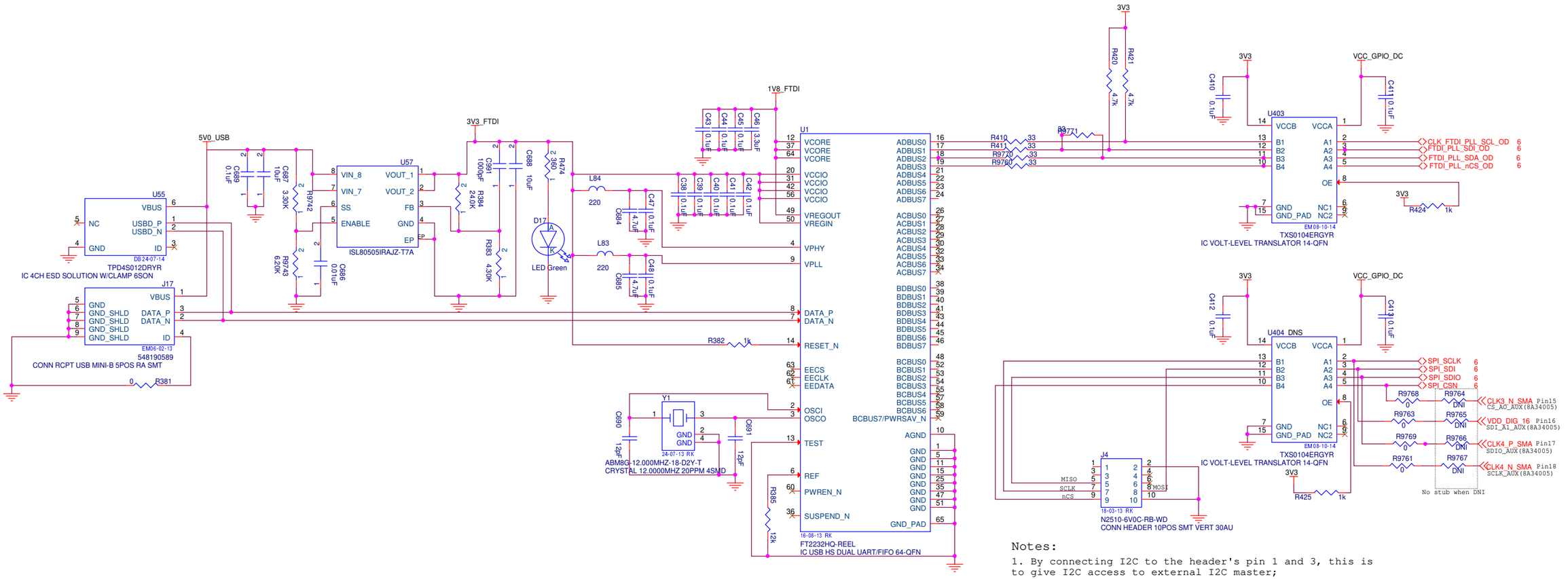
CHECK: DB	DRAWING NUMBER: SK-10280-01	REVISION: 1.2
	RELEASE DATE:	SHEET: 4 OF 10

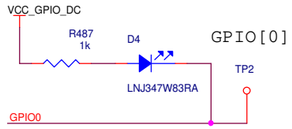


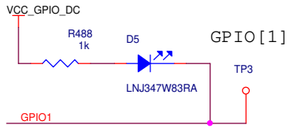
Notes:

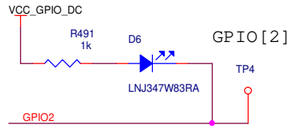
1. By connecting I2C to the header's pin 1 and 3, this is to give I2C access to external I2C master;
2. By installing R926 and R927, FTDI can also access Aux I2C port (also removing R87 and R88). This feature is not expected to be used.
3. Normal use: FTDI controls I2C port; Header is connected to Aux port in SPI configuration.

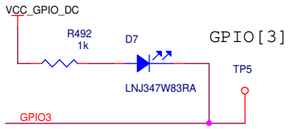
PROJECT NAME: Indira3	Fidus Systems, 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN: DB	TITLE:	
DRAWN: DB	SUBTITLE: FTDI USB Interface	
CHECK: DB	DRAWING NUMBER: SK-10280-01	REVISION: 1.2
	RELEASE DATE:	SHEET: 5 OF 10

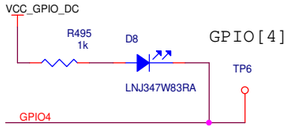
Note for Silkcreen:
Place GPIO[x] lable close to each
corresponding LED and Test point.

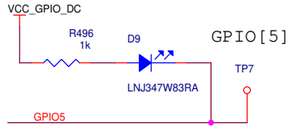


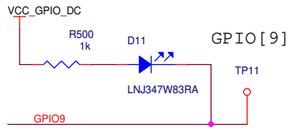


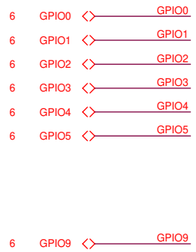




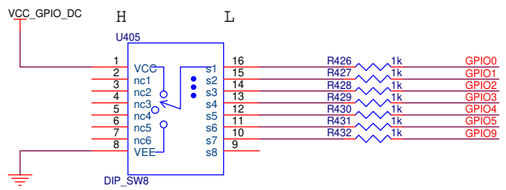








SILKSCRN:



PROJECT NAME: Indira3	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN: RK	TITLE:	
DRAWN: RK	SUBTITLE: GPIO LEDs	
CHECK: DB	DRAWING NUMBER: SK-10280-01	REVISION: 1.2
	RELEASE DATE:	SHEET: 6 OF 10

SILKSCRN:
OSCI

Place close to
crystal Y3

J45
DNS R469 0
DNS R470 0
DNS R471 0
DNS R472 0
19-03-13 RK
5-1814832-1
R468 39
R473DNS 10
C759 1.0uF DNS
OSCI
R9750 0
OSCO
Y3
C765 12pF
C766 12pF
NC1
NC2
25-11-15 DM
CX3225GB50000P0HPQCC
CRYSTAL 50.000MHZ 20PPM 18PF SMD
R9751 DNI
C996 0.1uF

I2 Bus

JP12~JP15 Default Jump Up

4 CLK_FTDI_PLL_SCL_OD
4 FTDI_PLL_SDA_OD
4 FTDI_PLL_SDI_OD
4 FTDI_PLL_nCS_OD
R117 33
R118 33
R9758 33
R9759 33
JP12
EEPROM_SEL
PLL_I2C_SCL_SCLK
JP13
EEPROM_SEL
PLL_I2C_SDA_SDIO
0552-2-15-01-11-27-10-0
P1 DNS
Y2 DNS
P2 DNS
A-50.000-12-EXT
CRYSTAL 50MHZ 12PF 30PPM HC49/U
15-01-16 RvR
15-01-18 RvR

SPI Bus

4 SPI_SCLK
4 SPI_SDIO
4 SPI_SDI
4 SPI_CSN
R119 33
R120 33
R121 33
R122 33
JP14
EEPROM_SEL
PLL_I2C_SDA_SDI
JP15
EEPROM_SEL
PLL_I2C_SDA_CSN

Place sockets to
match spacing of
through-hole crystal

VCC_GPIO_DC
R935 4.7k
JTAG_SEL
J83
18-03-13 RK
TSM-102-01-T-SV
CONN HEADER 2POS 0.1IN PITCH SMD

SILKSCRN:
JUMPER IN = JTAG

VCC_GPIO_DC
C417 0.1uF
R452 4.7k DNS
R451 4.7k DNS
R450 0
R455 4.7k
R454 4.7k
R453 4.7k
P3
11-11-14 RvR
A08-LC-TT
IC SOCKET STRAIGHT 8POS TIN
R449 1k
U408DNS
VCC A0
WP A1
A2
SCL
SDA VSS
28-01-14 RvR
24LC64-I/P
IC EEPROM 64KBIT 400KHZ 8DIP

VCC_GPIO_DC
R448 4.7k
R447 4.7k
R446 4.7k
PLL_I2C_SCL_SCLK
PLL_I2C_SDA_SDIO
J7
18-03-13 RK
TSM-102-01-T-SV
CONN HEADER 2POS 0.1IN PITCH SMD

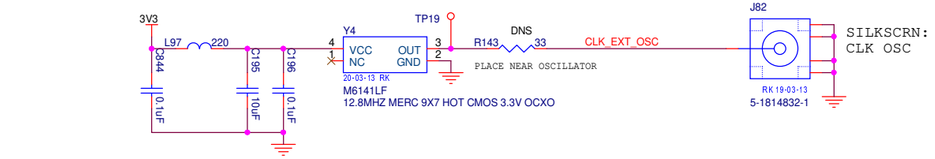
SILKSCRN:
JUMPER IN = WP OFF

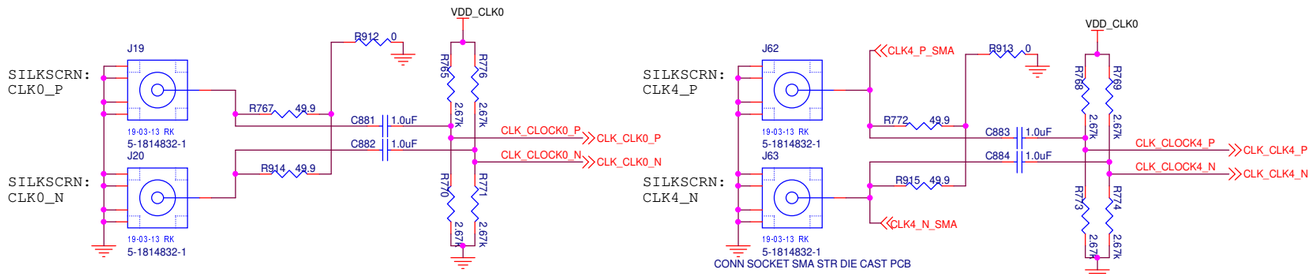
3V3
5V0
C415 0.1uF
R444 10k
R442 10k
R443 10k DNS
U407
VDD RESET_N
CT
MR_N
GND
SENSE GND_PAD
08-04-14 EM
TPS3808G01DRVR
ADJ SUPPLY MONITOR PRG DLY 6QFN
TST_CHIP_RST_N_OD
C416 0.1uF DNS
C428 0.01uF
R445 1k

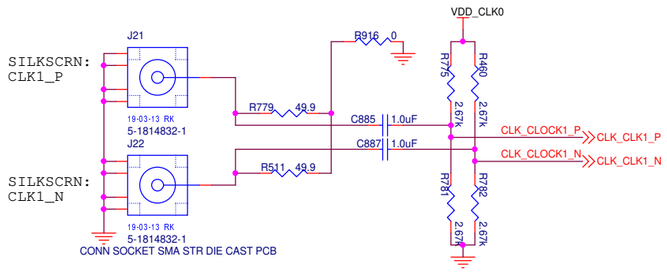
SILKSCRN:
RESET

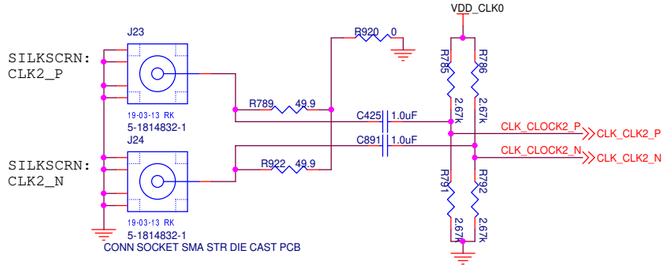
SW1
RvR 04-06-14
KMR211GLFS
SWITCH TACTILE SPST-NO 0.05A 32V

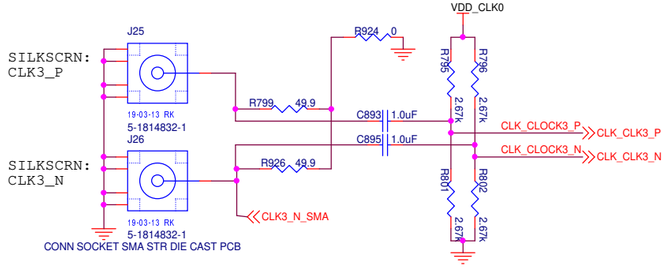
PROJECT NAME: Indira3	Fidus Systems, 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN: DB	TITLE:	
DRAWN: DB	SUBTITLE: PLL Core	
CHECK: DB	DRAWING NUMBER: SK-10280-01	REVISION: 1.2
	RELEASE DATE:	SHEET: 7 OF 10

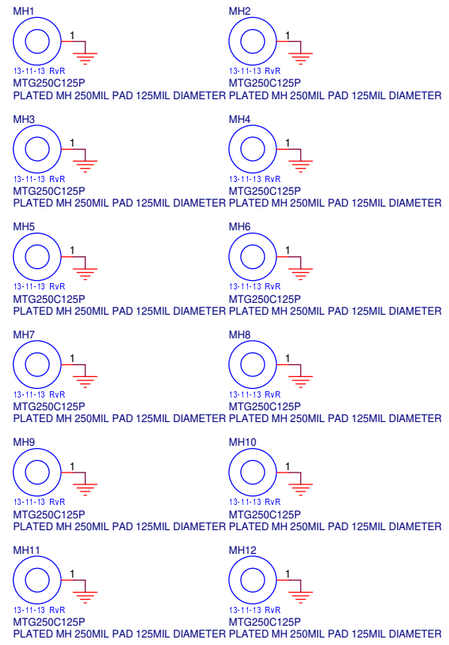






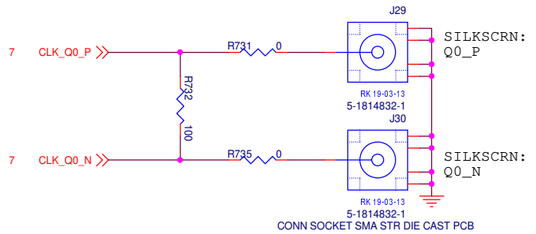


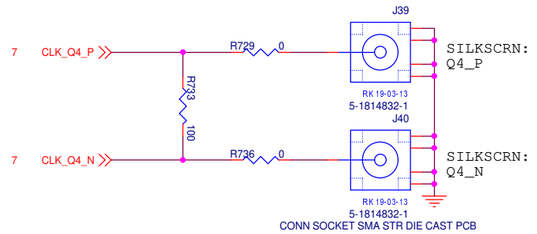


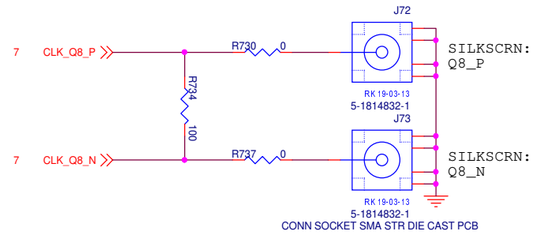


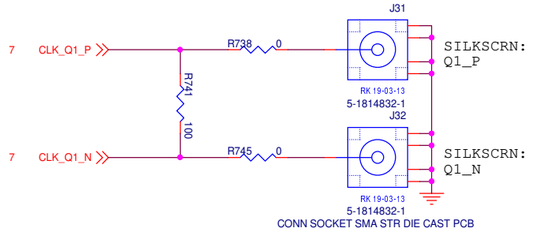
PROJECT NAME: Indira3	Fidus Systems, 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN: RK	TITLE:	
DRAWN: RK	SUBTITLE: PLL Input Clocks	
CHECK: DB	DRAWING NUMBER: SK-10280-01	REVISION: 1.2
	RELEASE DATE:	SHEET: 8 OF 10

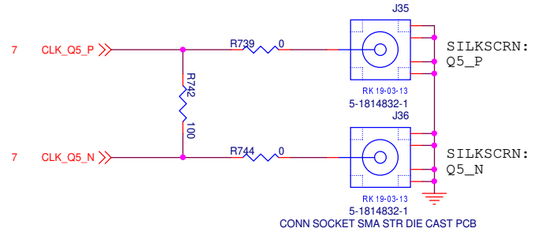
PLACE PARALLEL
TERMINATIONS
CLOSE TO U58

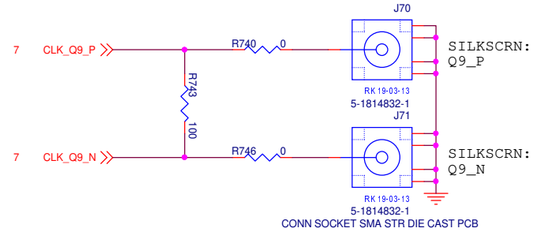


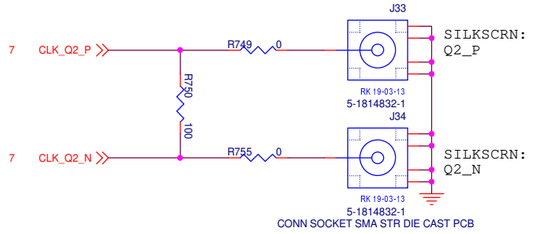


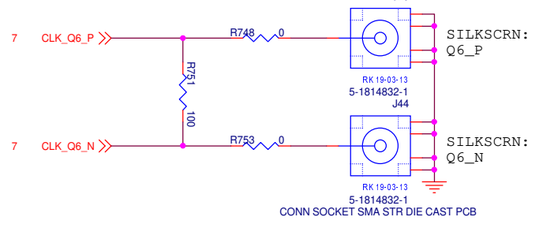


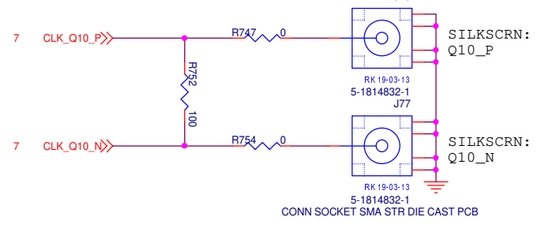


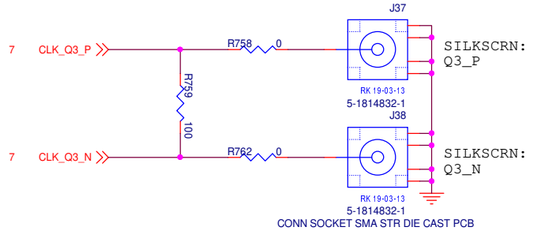


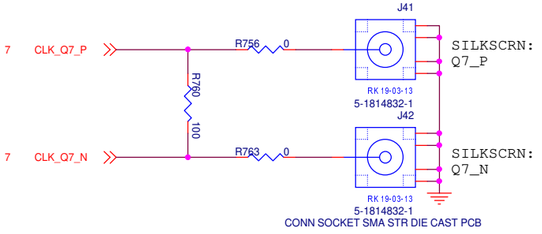


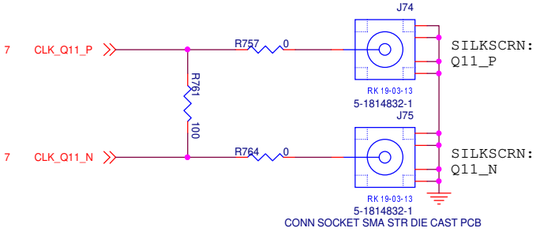




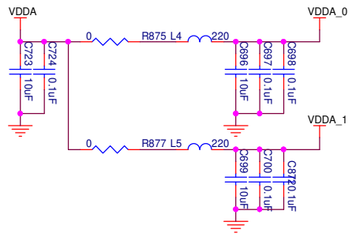


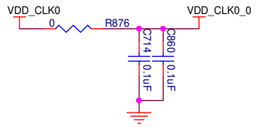


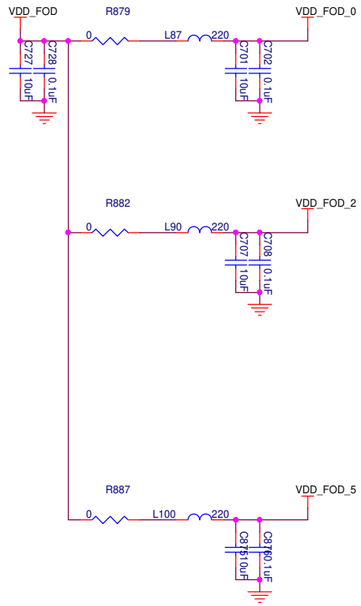


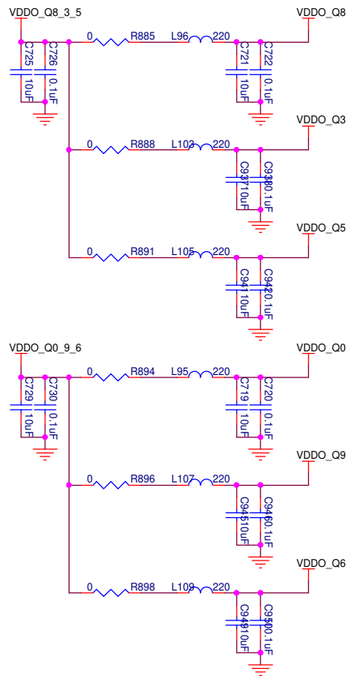


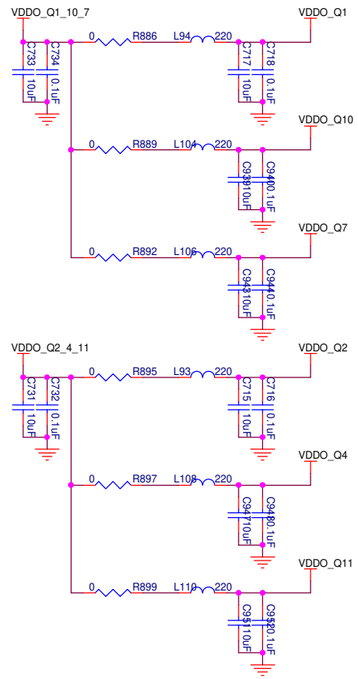
PROJECT NAME: Indira3	Fidus Systems, 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN: DB	TITLE:	
DRAWN: DB	SUBTITLE: PLL Output Clocks	
CHECK: DB	DRAWING NUMBER: SK-10280-01	REVISION: 1.2
	RELEASE DATE:	SHEET: 9 OF 10











PROJECT NAME: Indira3	Fidus Systems 375 Terry Fox Drive, Ottawa, ON K2K 0J8	
DESIGN: RK	TITLE:	
DRAWN: RK	SUBTITLE: PLL Power	
CHECK: DB	DRAWING NUMBER: SK-10280-01	REVISION: 1.2
	RELEASE DATE:	SHEET: 10 OF 10

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(Rev.1.0 Mar 2020)

Corporate Headquarters

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www.renesas.com

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