ISL55210

Wideband, Low-Power, Ultra-High Dynamic Range Differential Amplifier

FN7811
Rev 2.00
Jun 6, 2013

The ISL55210 is a very wide band, Fully Differential Amplifier (FDA) intended for high dynamic range ADC input interface applications. This voltage feedback FDA design includes an independent output common mode voltage control.

Intended for very high dynamic range ADC interface applications, at the lowest quiescent power (115mW), the ISL55210 offers a 4.0GHz Gain Bandwidth Product with a very low input noise of 0.85nV/√(Hz). In a balanced differential I/O configuration, with $2V_{P-P}$ output into a 200Ω load configured for a gain of 15dB, the IM3 terms are <-100dBc through 110MHz. With a minimum operating gain of 2V/V (6dB), the ISL55210 supports a wide range of higher gains with minimal BW or SFDR degradation. Its ultra high differential slew rate of 5,600V/µs ensures clean large signal SFDR performance or a fast settling step response.

The ISL55210 requires only a single 3.3V (max 4.2V) power supply with 35mA typical quiescent current. This industry leading low current solution can be further reduced when needed using the optional power shutdown to <0.4mA supply current. External feedback and gain setting resistors give maximum flexibility and accuracy. A companion device, the ISL55211, includes on-chip feedback and 3 possible gain setting connections where an internally fixed gain solution is preferred. The ISL55210 is available in a leadless, 16 Ld TQFN package and is specified for operation over the -40°C to +85°C ambient temperature range.

Features

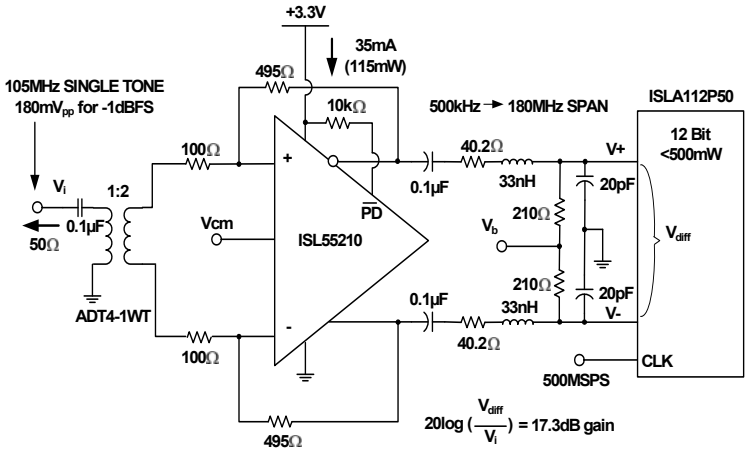
- Gain Bandwidth Product 4.0GHz
- Input Voltage Noise . . . . . 0.85nV/√(Hz)
- Differential Slew Rate 5,600V/µs
- $2V_{P-P}$, 2-tone IM3 (200Ω) 100MHz . . . . . -109dBc
- Supply Voltage Range . . . . . 3.0V to 4.2V
- Quiescent Power (3.3V Supply) 115mW

Applications

- Low Power, High Dynamic Range ADC Interface
- Differential Mixer Output Amplifier
- SAW Filter Pre/Post Driver
- Differential Comms-DAC Output Driver

Related Products and Literature

- ISL55211 - Fixed Gain Version of the ISL55210
- ISLA112P50 - 12-bit, 500MSPS ADC (<500mW)
- ISLA214P50 - 14-bit, 500MSPS ADC (<850mW)
- AN1649 - Designer's Guide to the ISL55210 and ISL55211 Evaluation Boards
- AN1725 - Ultra Low Power Broadband 8 to 14-Bit Data Acquisition Platform
- AN1837 - Ultra High Performance Broadband 12 to 16-Bit Data Acquisition Platform
- AN1831 - Designer's Guide to the ISL55210-ABEVAL1Z Active Balun Evaluation Board



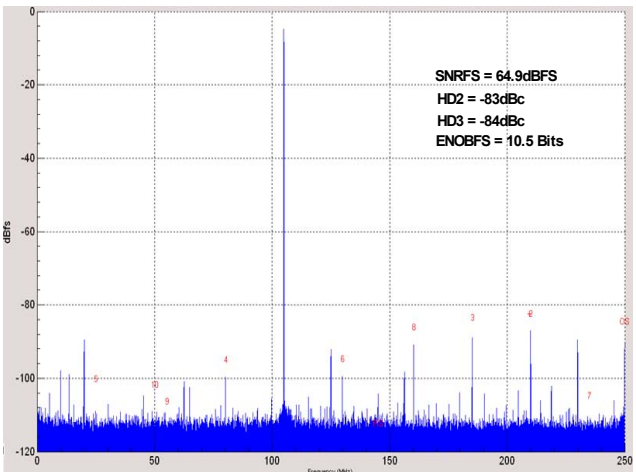
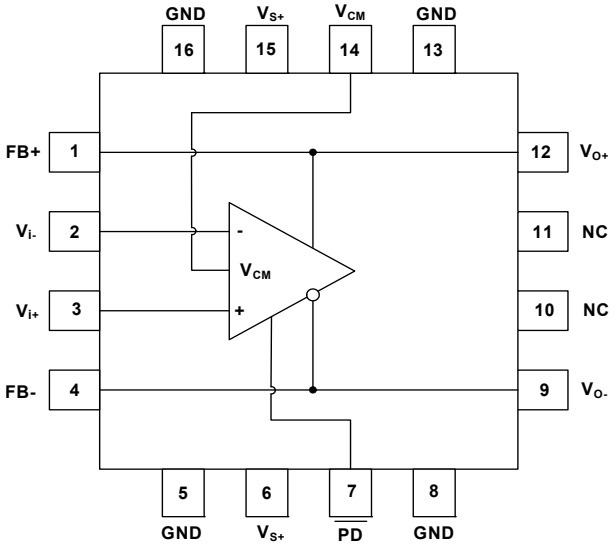


FIGURE 1. TYPICAL APPLICATION CIRCUIT

Pin Configuration

ISL55210
(3x3 16 LD TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	FB+	Positive Output Feedback resistor connection
2	V_{i-}	Inverting Amplifier Input
3	V_{i+}	Noninverting Amplifier Input
4	FB-	Negative Output Feedback resistor connection
5, 8, 13, 16	GND	Supply Ground (Thermal Pad Electrically Connected)
6, 15	V_{S+}	Positive power supply (3.0V~4.5V)
7	$\overline{PD}$	Power-down: $\overline{PD}$ = logic low puts part into low power mode, $\overline{PD}$ = logic high or 1kΩ to V_{S+} for normal operation
9	V_{O-}	Inverting Amplifier Output
10, 11	NC	No Internal Connection
12	V_{O+}	Noninverting Amplifier Output
14	V_{CM}	Common-mode Voltage Input

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	TRANSPORT MEDIA, QUANTITY	PKG. DWG. #
ISL55210IRTZ	5210	-40 to +85	16 Ld 3x3 TQFN		L16.3x3D
ISL55210IRTZ-T7	5210	-40 to +85	16 Ld 3x3 TQFN	Tape and Reel, 1000	L16.3x3D
ISL55210IRTZ-T7A	5210	-40 to +85	16 Ld 3x3 TQFN	Tape and Reel, 250	L16.3x3D
ISL55210IRTZ-EVALZ	Evaluation Board (Contact local sales)				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL55210. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage from V_{S+} to GND 4.5V
Input Voltage . . . . . V_{S+} +0.3V to GND-0.3V
Power Dissipation (See "Power Supply, Shutdown, and Thermal Considerations" on page 13)
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3500V
Machine Model (Per EIAJ ED-4701 Method C-111) 250V
Charged Device Model 1500V
Latch up (Per JESD-78; Class II; Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TQFN Package (Notes 4, 5)	63	16.5

Storage Temperature . . . . . -65°C to +125°C
Maximum Continuous Operating Junction Temperature . . . . . +135°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Operating Temperature . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{S+} = +3.3V Test Conditions: G = 12dB, V_{CM} = open, V_O = $2V_{P-P}$, R_F = 200Ω, R_L = 200Ω differential, T_A = +25°C, differential input, differential output, input and output referenced to internal default V_{CM} (1.2V nominal) unless otherwise specified.

PARAMETER	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT	TESTED (Note 7)
AC PERFORMANCE						
Small-Signal Bandwidth (4-port S parameter, Test Circuit #2)	G = 12dB, V_O = $100mV_{P-P}$		2,200		MHz	
	G = 18dB, V_O = $100mV_{P-P}$		700		MHz	
	G = 24dB, V_O = $100mV_{P-P}$		300		MHz	
Gain-Bandwidth Product	G = 18dB		4.0		GHz	
Bandwidth for 0.1-dB Flatness	G = 12dB, V_O = $100mV_{P-P}$		200		MHz	
Large-Signal Bandwidth	G = 12dB, V_O = $2V_{P-P}$		1.2		GHz	
Slew Rate (Differential)	2-V step		5,600		V/µs	
Differential Rise/Fall Time			0.17		ns	
2nd-order Harmonic Distortion	f = 20MHz, V_O = $2V_{P-P}$		-105		dBc	
	f = 50MHz, V_O = $2V_{P-P}$		-88		dBc	
	f = 100MHz, V_O = $2V_{P-P}$		-72		dBc	
3rd-order Harmonic Distortion	f = 20MHz, V_O = $2V_{P-P}$		-120		dBc	
	f = 50MHz, V_O = $2V_{P-P}$		-107		dBc	
	f = 100MHz, V_O = $2V_{P-P}$		-95		dBc	
2nd-order Intermodulation Distortion	f_C = 70MHz, 200kHz spacing ($2V_{P-P}$ envelope)		-80		dBc	
	f_C = 140MHz, 200kHz spacing ($2V_{P-P}$ envelope)		-68		dBc	
3rd-order Intermodulation Distortion	f_C = 70MHz, 200kHz spacing ($2V_{P-P}$ envelope)		-102		dBc	
	f_C = 140MHz, 200kHz spacing ($2V_{P-P}$ envelope)		-94		dBc	
Input Voltage Noise	f > 1MHz, Differential		0.85		$nV/\sqrt{HZ}$	
Input Current Noise	f > 1MHz, Each Input		5.0		$pA/\sqrt{HZ}$	

Electrical Specifications V_{S+} = +3.3V Test Conditions: G = 12dB, V_{CM} = open, V_O = $2V_{P-P}$, R_F = 200Ω, R_L = 200Ω differential, T_A = +25°C, differential input, differential output, input and output referenced to internal default V_{CM} (1.2V nominal) unless otherwise specified. **(Continued)**

PARAMETER	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT	TESTED (Note 7)
DC PERFORMANCE						
Open-loop Voltage Gain (A_{OL})	Differential	86	100		dB	*
Input Offset Voltage	T_A = +25°C	-1.4	±0.1	+1.4	mV	*
	T_A = -40°C to +85°C	-1.6	±0.1	+1.6	mV	
Average Offset Voltage Drift	T_A = -40°C to +85°C		±3		µV/°C	
Input Bias Current	T_A = +25°C, positive current into the pin		+50	+120	µA	*
	T_A = -40°C to +85°C		+50	+140	µA	
Average Bias Current Drift	T_A = -40°C to +85°C		+200		nA/°C	
Input Offset Current	T_A = +25°C	-5	±1	+5	µA	*
	T_A = -40°C to +85°C	-6	±1	+6	µA	
Average Offset Current Drift	T_A = -40°C to +85°C		±8		nA/°C	
INPUT						
Common-mode Input Range High				1.7	V	*
Common-mode Input Range Low		1.1			V	*
Common-mode Rejection Ratio	f < 10MHz, common mode to differential output	56	75		dB	*
Differential Input Impedance			1 ‖ 2		kΩ ‖ pF	
OUTPUT						
Maximum Output Voltage	Each output (with 200Ω differential load) Linear Operation	2.15	2.35		V	*
Minimum Output Voltage			0.45	0.63	V	*
Differential Output Voltage Swing	T_A = +25°C	3.04	3.8		V_{P-P}	*
	T_A = -40°C to +85°C	2.95			V	
Differential Output Current Drive	R_L = 10Ω [sourcing or sinking]	40	45		mA	*
Closed-loop Output Impedance	f < 10MHz, differential		0.6		Ω	
OUTPUT COMMON-MODE VOLTAGE CONTROL						
Small-signal Bandwidth	From V_{CM} pin to Output V_{CM}		30		MHz	
Slew Rate	Rising/Falling		150		V/µs	
Gain	V_{CM} input pin 1.0V to 1.4V	0.995	0.999		V/V	*
Output Common-Mode Offset from CM Input		-8	±1	+8	mV	*
CM Default Voltage	Output V_{CM} with V_{CM} pin floating	1.18	1.2	1.22	V	*
CM Input Bias Current	At control pin		2		µA	
CM Input Voltage Range	At control pin	0.9		1.9	V	*
CM Input Impedance	At control pin		15 ‖ 50		kΩ ‖ pF	
POWER SUPPLY						
Specified Operation Voltage		3	3.3	4.2	V	
Quiescent Current	T_A = +25°, V_{S+} = 3.3V, V_{S-} = 0V	33	35	37	mA	*
	T_A = -40°C to +85°C	30.5	36	39.5	mA	
Power-supply Rejection (PSRR) V_{S+}	3.0V - 4.5V range	56	90		dB	*

Electrical Specifications V_{S+} = +3.3V Test Conditions: G = 12dB, V_{CM} = open, V_O = $2V_{P-P}$, R_F = 200Ω, R_L = 200Ω differential, T_A = +25°C, differential input, differential output, input and output referenced to internal default V_{CM} (1.2V nominal) unless otherwise specified. **(Continued)**

PARAMETER	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT	TESTED (Note 7)
POWER-DOWN	Referenced to GND					
Enable Voltage Threshold	Assured on above 1.55V		1.3	1.55	V	*
Disable Voltage Threshold	Assured off below 0.54V	0.54	0.7		V	*
Power-down Quiescent Current	T_A = +25°C	0.2	0.3	0.4	mA	*
	T_A = -40°C to +85°C	0.15	0.3	0.45	mA	
Input Bias Current	$\overline{PD}$ = 0V, current positive into pin		-2		µA	
Input Impedance			2 || 5		MΩ || pF	
Turn-on Time Delay	Measured to output on		200		ns	
Turn-off Time Delay	Measured to output off		400		ns	

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
7. Parameters denoted by an "*" are ATE tested.

Typical Performance Curves

V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted.

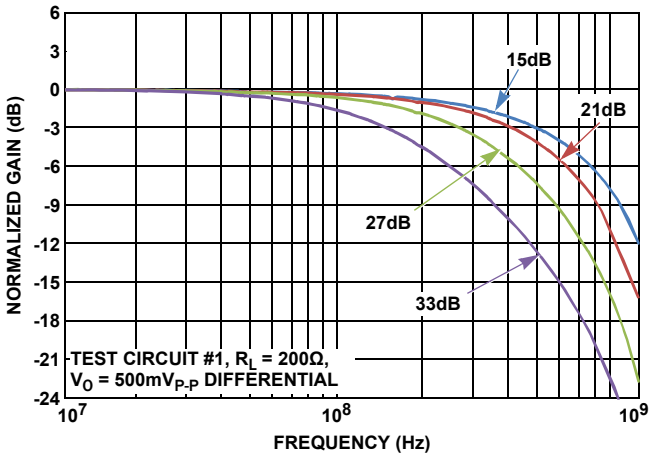


FIGURE 2. FREQUENCY RESPONSE vs GAIN SETTING

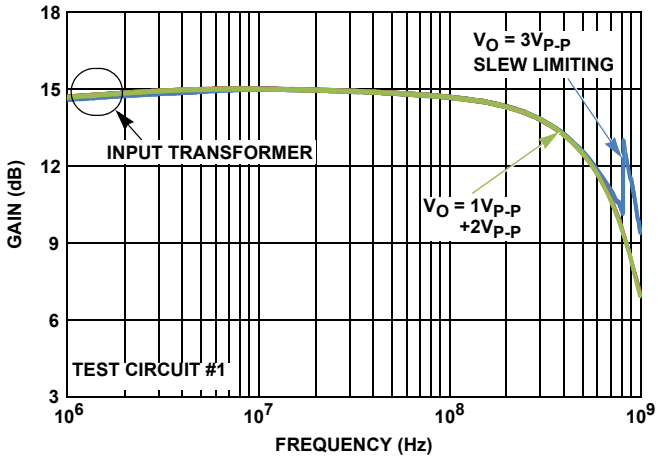


FIGURE 3. FREQUENCY RESPONSE vs OUTPUT SWING

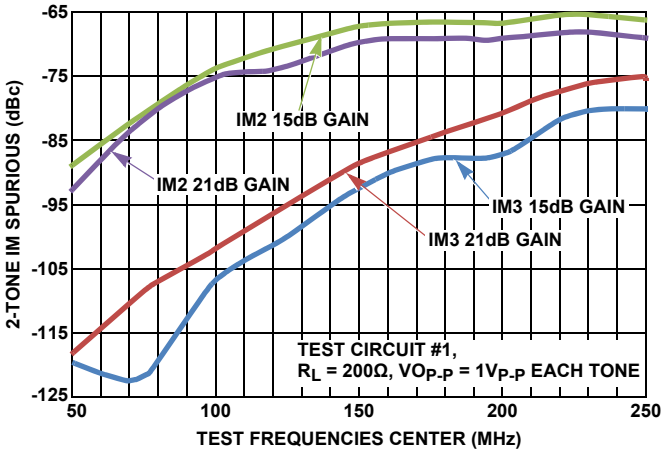


FIGURE 4. IM2 AND IM3 vs GAIN

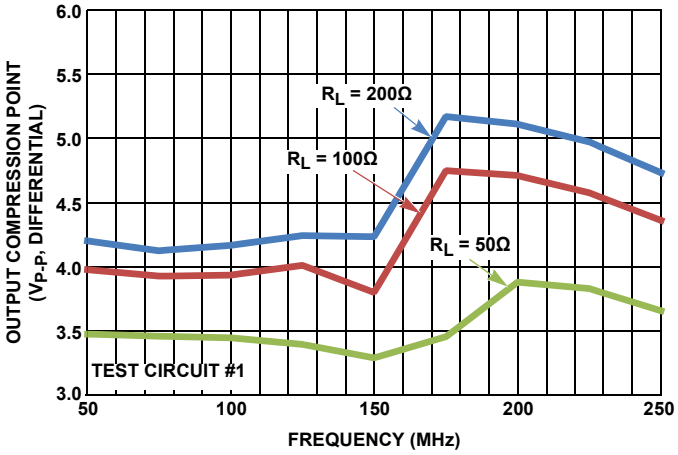


FIGURE 5. OUTPUT V_{P-P} FOR -1dB GAIN COMPRESSION

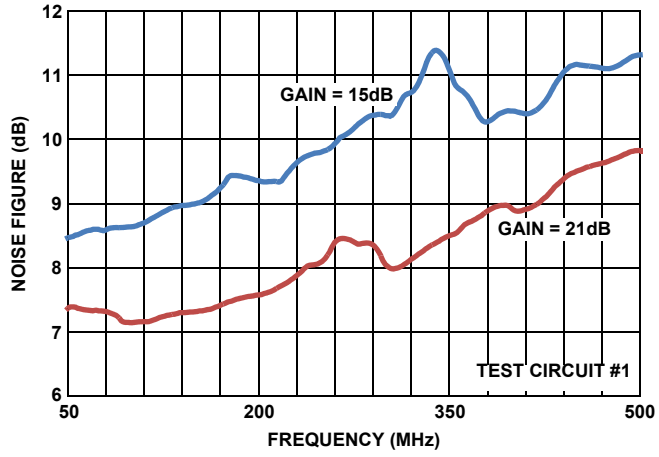


FIGURE 6. NOISE FIGURE

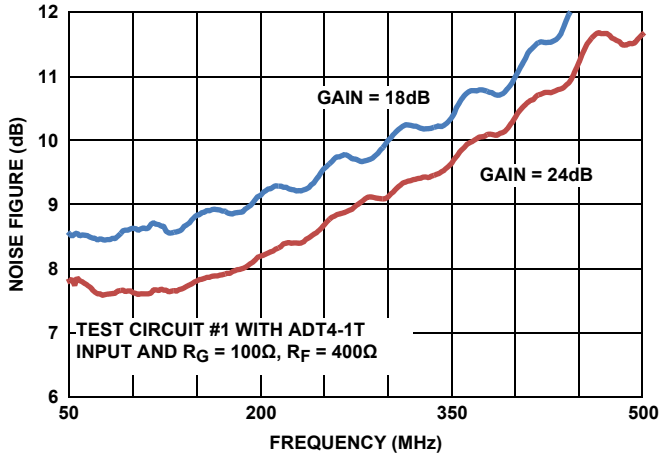


FIGURE 7. NOISE FIGURE AT HIGHER GAINS

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted. **(Continued)**

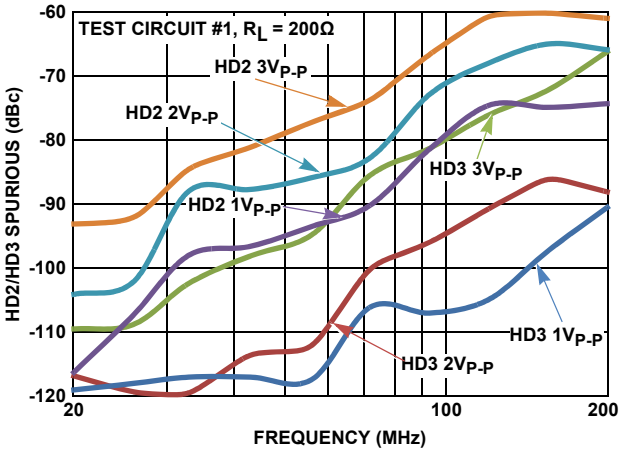


FIGURE 8. HD2/HD3 vs V_{OPP}

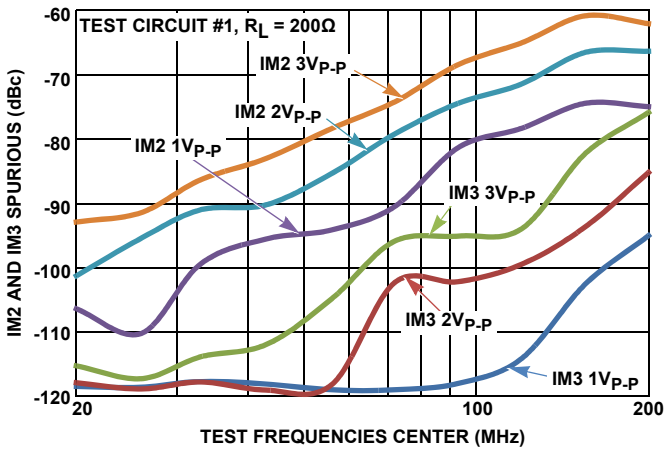


FIGURE 9. IM2 AND IM3 vs OUTPUT SWING

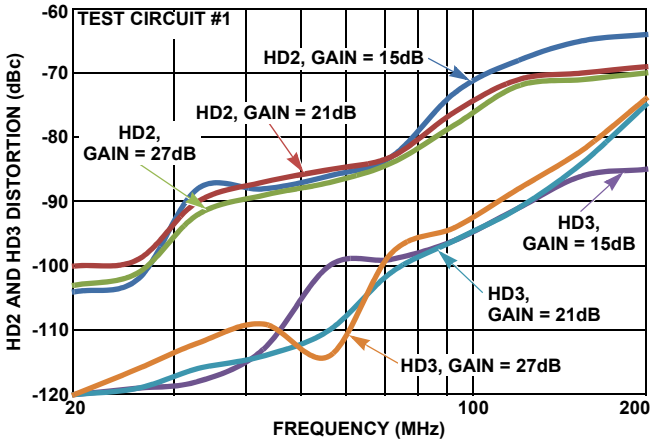


FIGURE 10. HD2 AND HD3 vs GAIN

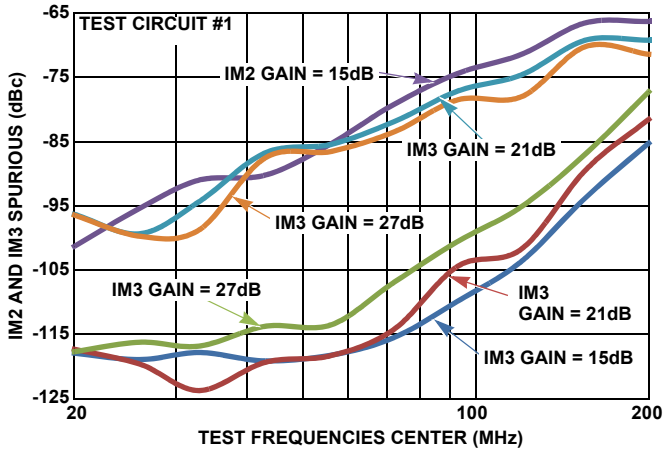


FIGURE 11. IM2 AND IM3 vs GAIN

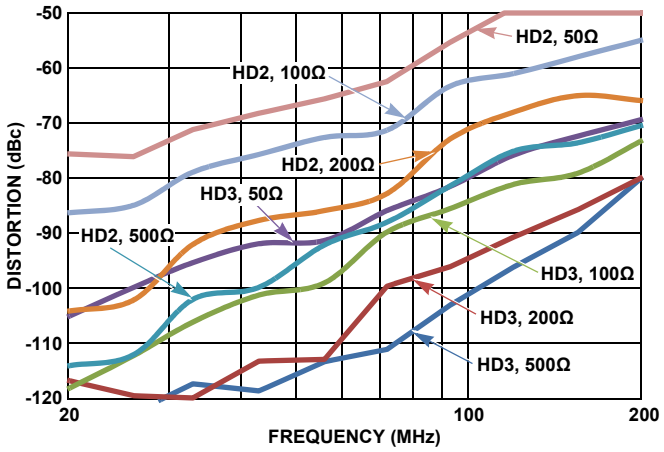


FIGURE 12. HD2 AND HD3 vs R_{LOAD}

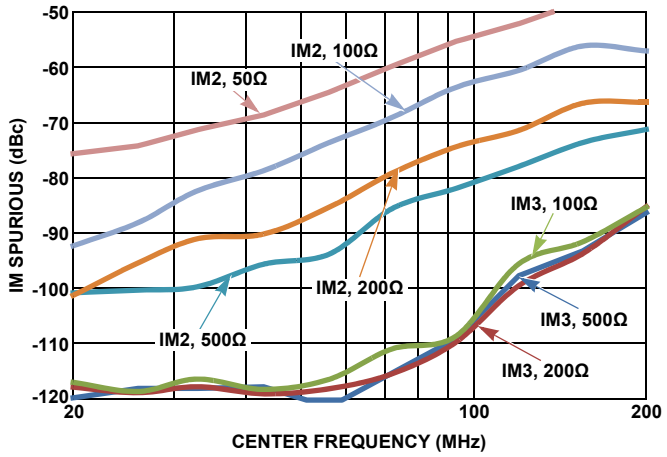


FIGURE 13. IM2 AND IM3 vs R_{LOAD}

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted. **(Continued)**

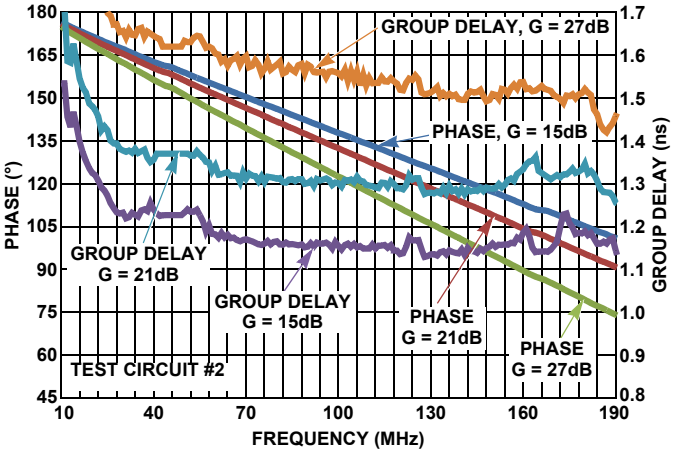


FIGURE 14. PHASE AND GROUP DELAY vs GAIN

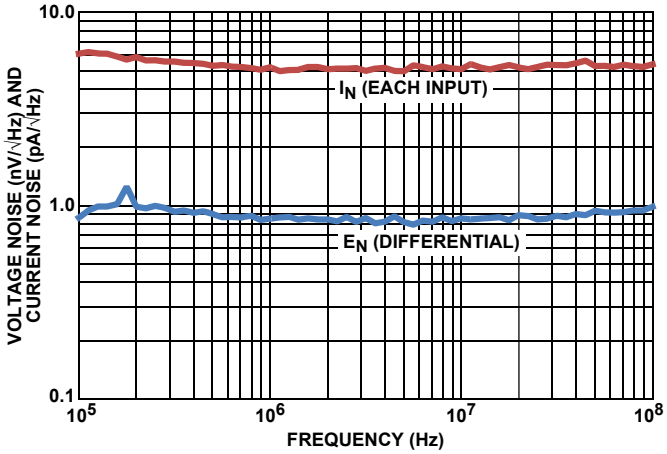


FIGURE 15. INPUT VOLTAGE AND CURRENT SPOT NOISE

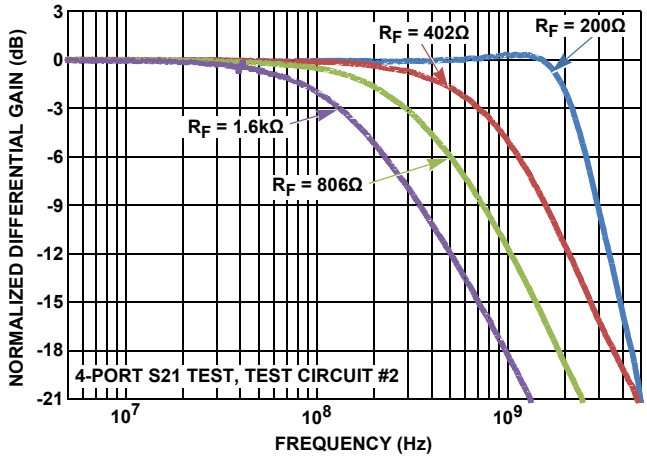


FIGURE 16. SMALL SIGNAL RESPONSE vs GAIN

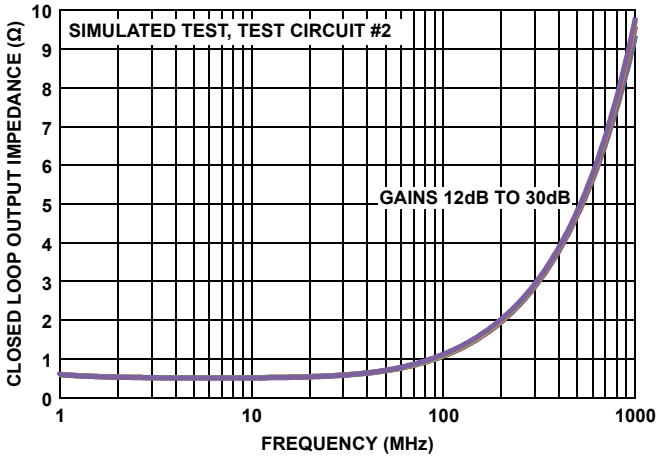


FIGURE 17. DIFFERENTIAL OUTPUT IMPEDANCE

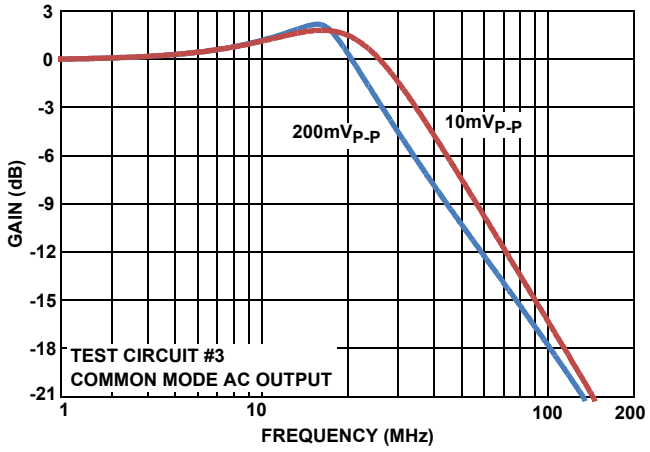


FIGURE 18. V_{CM} PIN INPUT FREQUENCY RESPONSE TO OUTPUT COMMON MODE

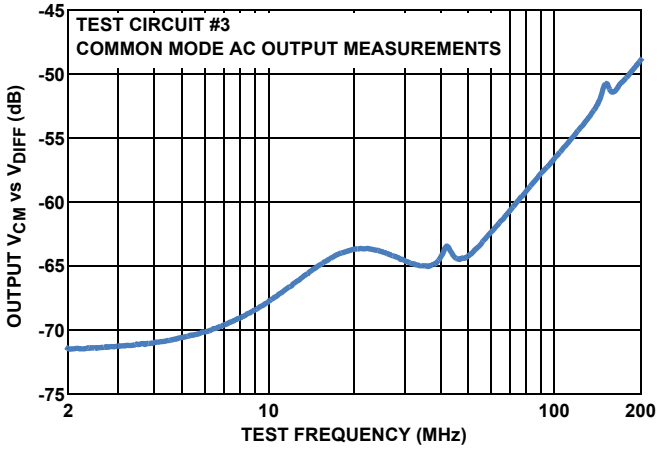


FIGURE 19. OUTPUT BALANCE ERROR

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted. **(Continued)**

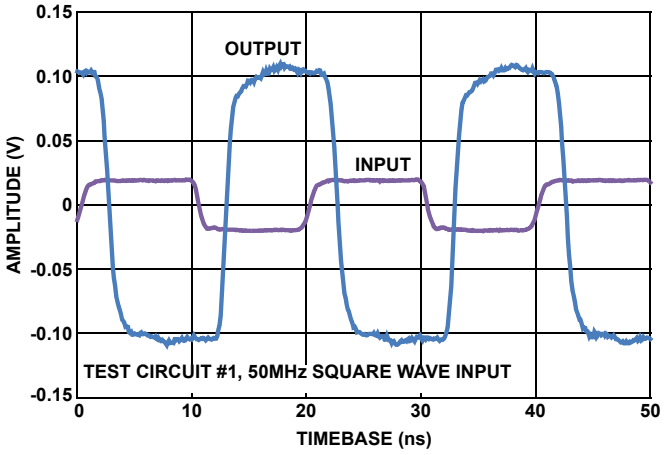


FIGURE 20. SMALL SIGNAL STEP RESPONSE

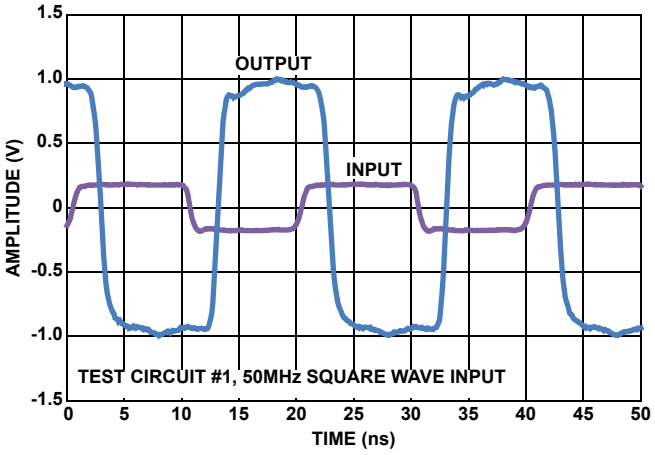


FIGURE 21. LARGE SIGNAL STEP RESPONSE

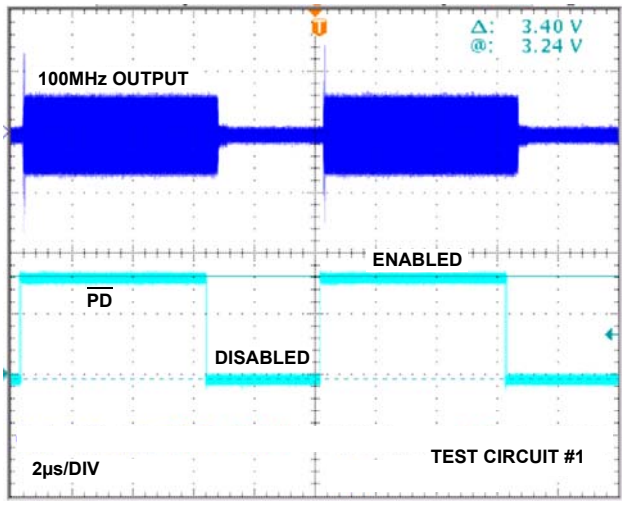


FIGURE 22. ENABLE/DISABLE TIMES

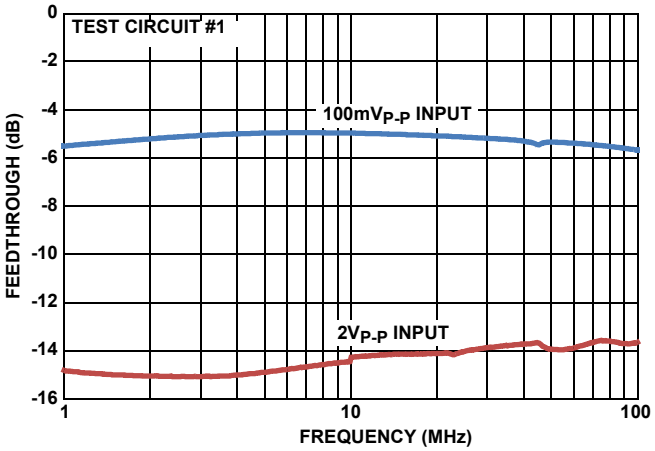


FIGURE 23. DISABLED FEEDTHROUGH

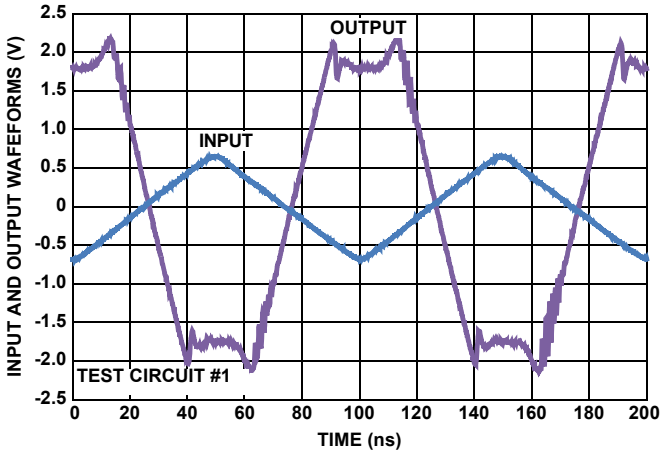


FIGURE 24. OVERDRIVE RECOVERY

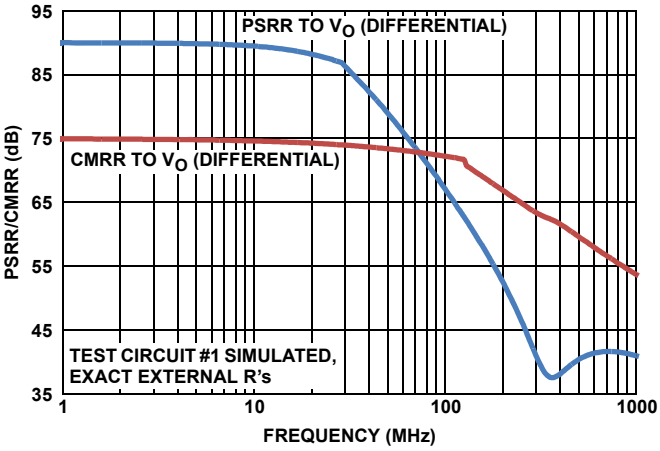


FIGURE 25. PSRR/CMRR TO DIFFERENTIAL V_O

Typical Performance Curves V_{S+} = 3.3V, $T_A \approx +25°C$, unless otherwise noted. **(Continued)**

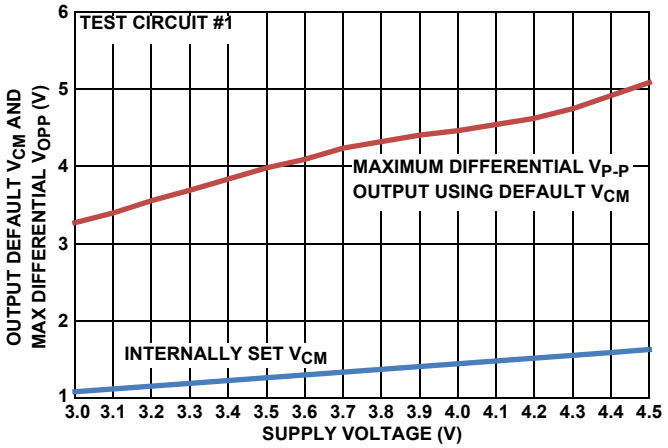


FIGURE 26. DEFAULT V_{CM} AND MAX V_{OPP} vs SUPPLY VOLTAGE

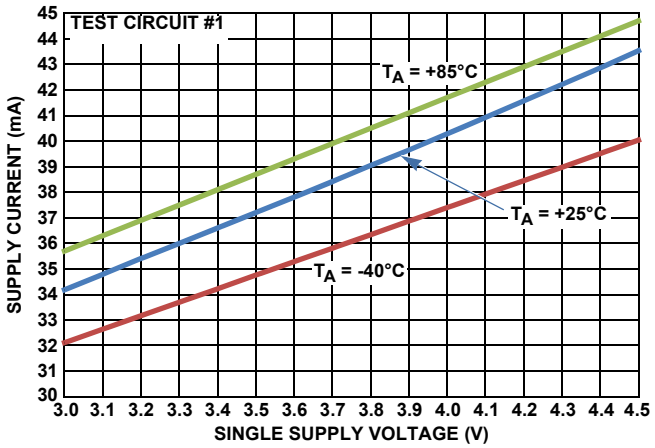


FIGURE 27. SUPPLY CURRENT vs SUPPLY VOLTAGE

Applications

Basic Operation

The ISL55210 is a very wideband, voltage feedback based, differential amplifier including an output common mode control loop and optional power shutdown feature. Intended for very low distortion differential signal driving, this non-unity gain stable device also delivers extremely low input noise terms of 0.85nV/√Hz and 5pA/√Hz. Most applications are intended for AC coupled I/O using a single 3.3V supply. It will operate over a single supply range of 3.0V to 4.2V. Where DC coupled operation is desired, using split power supplies will allow the ISL55210 I/O common mode range limits to be observed while giving either a differential I/O or single to differential configuration.

Most applications behave as a differential inverting op amp design. There is, therefore, an input gain resistor on each side of the inputs that must be driven. To retain overall low output noise, these resistors are normally of low value. The device can be powered down to <400µA supply current using the optional disable pin. To operate normally, this pin should be asserted high using a simple logic gate to $+V_S$ or tied high through a 10kΩ resistor to $+V_S$. When disabled, the power dissipation drops to <1mW but, due to the inverting op amp type architecture, the input signal will feed forward through the external resistors giving limited isolation.

Application and Characterization Circuits

The circuit of Figure 28 forms a starting point for many of the characterization curves for the ISL55210. Since most lab sources and measurement devices are single-ended, this circuit converts to differential at the input through a wideband transformer and would also be a typical application circuit coming from a single ended source. Assuming the source is a 50Ω impedance, the R_G resistors are set to provide both the input termination and the gain. Since the inverting summing nodes act as virtual ground points for AC signal analysis, the total termination impedance across the input transformer secondary will be 2 * R_G. Setting this equal to n^2*R_S will give a matched input impedance inside the bandwidth of the transformer (where "n" is the turns ratio). The amplifier gain is then set by adjusting the feedback resistors values. Since the ISL55210 is a VFA design, increasing the feedback resistor to get higher gain does not directly reduce the bandwidth as it would with a CFA based design. This gives increased flexibility in the input turns ratio and overall gain setting (while holding a matched input impedance) over alternate solutions.

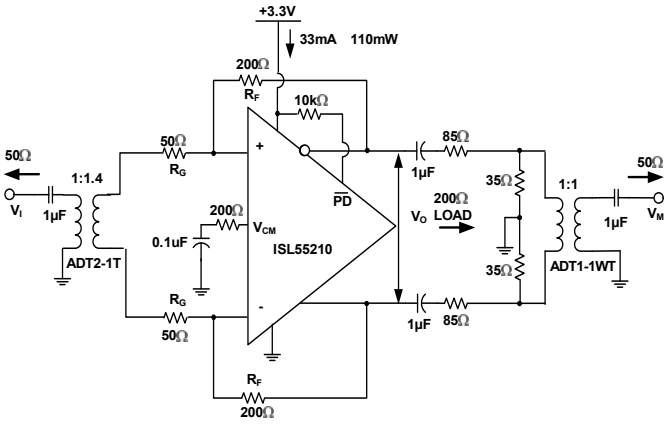


FIGURE 28. TEST CIRCUIT #1

Working with a transformer coupled input as shown in Figure 28, or with two DC blocking caps from a differential source, means the output common mode voltage set by either the default internal V_{CM} setting, or a voltage applied to the V_{CM} control pin, will also appear as the input common mode voltage. This provides a very easy way to control the ISL55210 I/O common mode operating voltages for an AC coupled signal path. The internal common mode loop holds the output pins to V_{CM} and, since there is no DC path for an I_{CM} current back towards the input in Figure 28, that V_{CM} setting will also appear as the input common mode voltage. It is useful, for this reason, to leave any input transformer secondary centertap unconnected. The internally set V_{CM} voltage is referenced from the negative supply pin. With a single 3.3V supply, it is very close to 1.2V but will change with total supply voltage across the device as shown in Figure 26.

Most of the characterization curves start with Figure 28 then get different gains by changing the feedback resistor, R_F, use different input transformers where then the R_G is also adjusted to hold an input match, or vary the loading. For load tests below the 200Ω shown in Figure 28, a simple added shunt resistor is placed across the output pins. For loads >200Ω, the series and shunt load R's are adjusted to show that total load (including the 50Ω measurement load reflected through the 1:1 output measurement port transformer) and provide an apparent 50Ω differential source to that transformer. This output side transformer is for measurement purposes only and is not necessary for final applications circuits. There are output interface designs that do benefit from a transformer as part of the signal path, but the one shown at the right of Figure 28 is used only for characterization to get a doubly terminated 50Ω measurement path going differential to single ended.

Where just the amplifier is tested, a 4 port network analyzer is used and the very simple test circuit of Figure 29 is implemented. This is used to extract the differential S21 curves and differential output impedance vs gain. Changing the gain is a simple matter of adjusting the two R_F resistors of Figure 29. This circuit depends on the two AC coupled source 50Ω of the 4 port network analyzer and presents an AC coupled differential 100Ω load to the amplifier as the input impedance of the remaining two ports of the network analyzer.

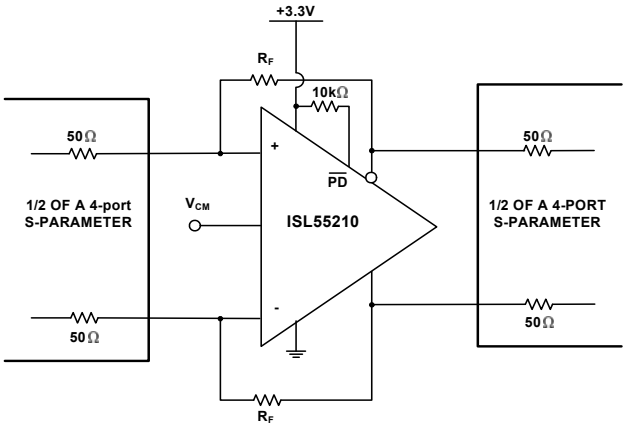


FIGURE 29. TEST CIRCUIT #2 4-PORT S-PARAMETER MEASUREMENTS

Using this measurement allows the full small single bandwidth of the ISL55210 to be exposed. Many of the other measurements are using I/O transformers that are limiting the apparent bandwidth to reduced level. Figure 16 shows a series of normalized differential S21 curves for gains of 12dB to 30dB in 6dB steps. These are simply stepping two feedback resistor values (R_F) up from 200Ω to 1600Ω in 2X steps. The lowest gain of 12dB (4V/V) is showing a 2.2GHz small signal bandwidth. This response gets some bandwidth extension due to phase margin <60degree effects, but by the gain of 24dB (16V/V), the bandwidth is following a Gain Bandwidth type characteristic showing 300MHz bandwidth or >4GHz Gain Bandwidth Product (GBP).

The closed loop differential output impedance of Figure 17 is simulated using Figure 29 in ADS. This shows a relatively low output impedance (<1Ω through 100MHz) constant with signal gain setting. Typical FDA outputs show a closed loop output impedance that increases with signal gain setting. The ISL55210 holds a more constant response vs gain due to internal design elements unique to this device.

Common mode output measurements are made using the circuit Figure 30. Here, the outputs are summed together through two 100Ω resistors (still a 200Ω differential load) to a center point where the average, or common mode, output voltage may be sensed. This is coupled through a 1µF DC blocking capacitor and measured using 50Ω test equipment. The common mode source impedance for this circuit is the parallel combination of the 2Ω - 100Ω elements, or 50Ω. Figure 18 uses this circuit to measure the small and large signal response from the V_{CM} control pin to the output common mode. This pin includes an internal 50pF capacitor on the default bias network (to filter supply noise when there is no connection to this pin) which bandlimits the response to approximately 30MHz. This is far lower than the actual bandwidth of the common mode loop. Figure 19 uses this output CM measurement circuit with a large signal ($2V_{P-P}$) differential output voltage (generated through the V_i path of Figure 30) to measure the differential to common mode conversion.

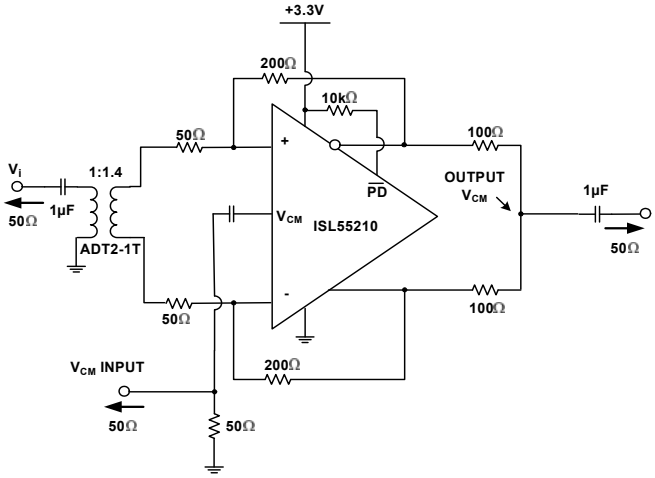


FIGURE 30. TEST CIRCUIT #3 COMMON MODE AC OUTPUT MEASUREMENTS

Single Supply, Input Transformer Coupled, Design Considerations

The characterization circuit of Figure 28 shows one possible input stage interface that offers several advantages. The ISL55210 can also support a DC coupled differential to differential or single ended input to differential requirement if needed. Where AC coupling is adequate, the circuit of Figure 28 simplifies the input common mode voltage control. If the source coming into this stage is single ended, the input transformer provides a zero power conversion to differential. The two gain resistors (R_G in Figure 28) provide both the input termination impedance and the gain element for the amplifier. For minimum noise, only R_G should be used and set to achieve the desired input impedance. Since the ISL55210 is a VFA device, these resistor values can be scaled up and down a bit more freely than a current feedback based FDA.

For instance, if a minimum noise configuration is not required, but it is desirable to increase the feedback resistors to reduce the added loading they present to the output stage, the R_G and R_F resistors can be scaled up to achieve the same gain with an additional termination resistance added across the input transformer to adjust the termination impedance. Figure 31 shows an example using a 1:2 input turns ratio where the R_G and R_F elements have been scaled up and a shunt termination resistance added. This example provides a single to differential signal gain of 20dB and input impedance of 50Ω to the source. The 1:2 turn ratio transformer needs a 200Ω differential secondary impedance to provide an input side 50Ω match. This is provided here by the parallel combination of the 2Ω - 200Ω R_G resistors and the 400Ω parallel impedance at the transformer secondary.

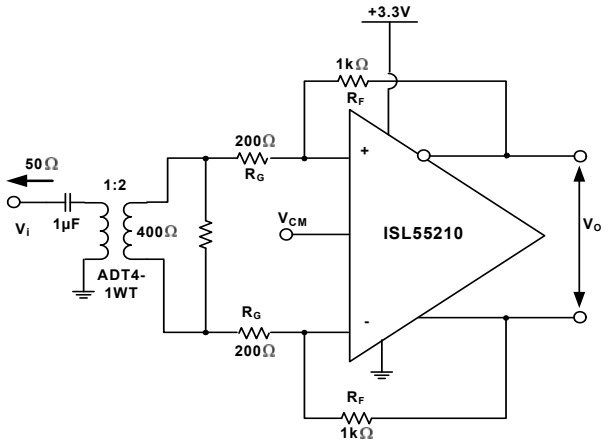


FIGURE 31. SINGLE TO DIFFERENTIAL WITH REDUCED FEEDBACK LOADING

This circuit has scaled the feedback resistor up to 1kΩ to still achieve the amplifier gain of 5V/V which gives the overall gain of 10V/V (20dB) when the 1:2 step up at the input is considered. The particular transformer shown is typical of 1:2 turns ratio broadband transformers, but there a many alternates with the similar or improved characteristics.

This input interface also simplifies the input common mode control. The V_{CM} pin controls the output common mode voltage. In most DC coupled FDA applications, the input common mode voltage is determined by both this output common mode and the source signal. In a configuration like Figure 31, there is no path for a common mode current to flow from output to input, so the input common mode voltage equals the output. A similar effect could be achieved with just two blocking caps on the two R_G resistors. A DC coupled, single to differential, configuration will also have a common mode input that is moving with the input signal. Converting to just a differential signal at the amplifier, as in Figure 31, removes any input signal related artifacts from the input common mode making the ISL55210 behave as a differential only VFA amplifier. There is only a very small differential error signal at the inputs set by the loop gain, as in a normal single ended VFA application, but no common mode signal related terms.

The examples shown are using the transformer to convert from single to differential. However, if the source is already differential, these same transformer input circuits can drive the transformer differentially still providing impedance scaling if needed and common mode rejection for both DC and AC common mode issues. A good example would be differential mixer outputs or SAW filter outputs. Those differential sources could also be connected into the ISL55210 R_G resistors through blocking caps as well eliminating the input transformer. The AC termination impedance for the differential source will then be the sum of the two R_G resistors when simple blocking caps are used.

Amplifier I/O Range Limits

The ISL55210 is intended principally to give the lowest IM3 performance on the lowest power for a differential I/O application. The amplifier will work DC coupled and over a relatively wide supply range of 3.0V to 4.2V supplies. The outputs have both a differential and common mode operating range while the input pins have a common operating range. For single supply operation, the ground pins are at ground as is the exposed metal pad on the underside of the package. The ISL55210 can operate split supply where then the ground pins will be a negative supply voltage and the exposed metal pad is either connected to this negative supply or left unconnected on an insulating board layer.

Briefly, the I/O and V_{CM} limits are:

1. Maximum V_{CM} setting = $-V_S + 2V$
2. Input common mode operating range of $-V_S + 1.1V$ or the output $V_{CM} + 0.5V$
3. Output V_O minimum (on each side) is either $-V_S + 0.3V$ or output $V_{CM} - 0.9V$
4. Output V_O maximum (on each side) is $+V_S - 1.5V$

The output swing limits are often asymmetrical around the V_{CM} voltage. The maximum single ended swings are set by these two limits:

V_{OMIN} is either $-V_S + 0.3V$ or $V_{CM} - 0.9V$ whichever is less. So for instance on a single 3.3V supply with the default V_{CM} voltage of 1.2V, these two limits give the same result and the output pins can swing down to 0.3V above $-V_S = 0V$. If, however, the V_{CM} pin is raised to 1.5V, then the minimum output voltage will become 1.5V - 0.9V = 0.6V.

V_{OMAX} is set by a headroom limit to the positive supply to be:

$V_{OMAX} = +V_S - 1.5V$. Again, on a 3.3V single supply and the default 1.2V V_{CM} setting, this mean the maximum referenced to ground output pin voltages can be 3.3V - 1.5V = +1.8V or 0.6V above the default V_{CM} voltage.

Using these default conditions, and the maximum positive excursion of 0.6V above the 1.2V output V_{CM} setting, the maximum differential V_{P-P} swing will be 4X this 0.6V single ended limit or $2.4V_{P-P}$. Where $+V_S$ is increased the limit then becomes the 0.9V below V_{CM}, but then the absolute maximum differential V_{P-P} is then 4X 0.9V to $3.6V_{P-P}$. So, for instance, to get this maximum output swing, increase the supply voltage until $+V_S - 1.5V > V_{CM} + 0.9V$. If we assume a V_{CM} voltage of 1.3V for instance, then 1.3V + 0.9V + 1.5V = 3.7V will give an unclipped

3.6V_{P-P} output capability. The V_{P-P} reported in Figure 26 is an asymmetrically clipped maximum swing. Going 10% above this 3.7V target to 4.1V will be within the recommended operating range and give some tolerancing headroom that would also suggest the V_{CM} voltage be moved up to approximately 1.5V. This coincides with the default output V_{CM} from Figure 26. Operating at +4.1V single supply in a Figure 28 type configuration will give the maximum linear available output swing of 3.6V_{P-P}.

The differential inputs of the ISL55210 also have operating range limits relative to the supply voltages. Operating in an AC coupled circuit like Figure 28 will produce an input common mode voltage equal to the outputs. The inputs can operate with full linearity with this V_{CM} voltage down to 1.1V above the GND connection (or -V_S supply). On the default 1.2V output V_{CM} on +3.3V supplies this gives a 100mV guardband on the input V_{CM} voltages. Overriding the default V_{CM} by applying a control voltage to the V_{CM} pin should be done with care in going towards the negative supply due to this limit. On the + side, the maximum V_{CM} above the -V_S supply is 2V so there is more room to move the output V_{CM} up than down from the default value.

When operated as a DC coupled single to differential amplifier, the input common mode voltage will move with the input signal and will be different than the output common mode voltage when the external resistors are set for gain. When the input common mode can be different than the output, the additional constraint that must be observed is that the input common mode voltage cannot be > output V_{CM} +0.5V. This would only occur if the single source was coming from a higher voltage than the output V_{CM} setting.

Power Supply, Shutdown, and Thermal Considerations

The ISL55210 is intended for single supply operation from 3.0V to 4.2V with an absolute maximum setting of 4.5V. The 3.3V supply current is trimmed to be nominally 35mA at +25°C ambient. Figure 27 shows the supply current for nominal +25°C and -40°C to +85°C operation over the specified maximum supply range. The input stage is biased from an internal voltage referenced from the negative supply giving the exceptional 90dB low frequency PSRR shown in Figure 25.

Since the input stage bias is from a re-regulated internal supply, a simple approach to single +5V operation can be supported as shown in Figure 32. Here, a simple IR drop from the +5V supply will bring the operating supply voltage for the ISL55210 into its allowed range. Figure 32 shows example calculations for the voltage range at the ISL55210 +V_S pin assuming a ±5% tolerance on the +5V supply and a 35mA to 55mA range on the total supply current. Considering the 34mA to 44mA quiescent current range from Figure 27 over the -40°C to +85°C ambient, and the 3.4V to 4.4V supply voltage range assumed here, this is designing for a 1mA to 11mA average load current which should be adequate for most intended application loads. Good supply decoupling at the device pins is required for this simple solution to still provide exceptional SFDR performance.

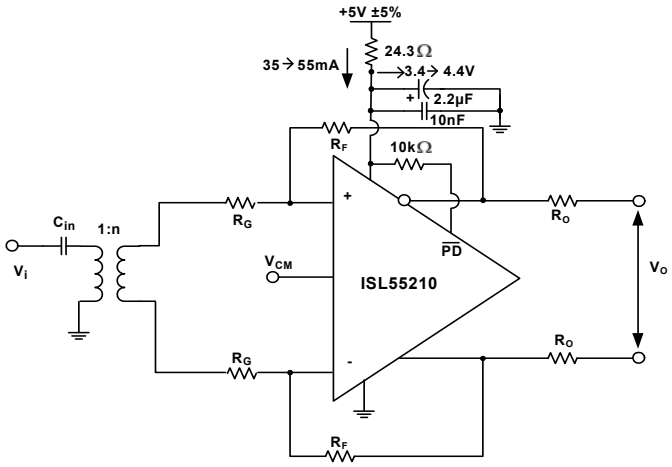


FIGURE 32. OPERATING FROM A SINGLE +5V SUPPLY

The ISL55210 includes a power shutdown feature that can be used to reduce system power dissipation when signal path operation is not required. This pin ($\overline{PD}$) is referenced to the ground pins and must be asserted low to activate the shutdown feature. When not used, a 10kΩ external resistor to +V_S should be used to assert a high level at this pin. Digital control on this pin can be either an open collector output (using that 10kΩ pullup) or a CMOS logic line running off the same +V_S as the amplifier. For split supply operation, the PD pins must be pulled to below -V_S + 0.54V to disable.

Since the ISL55210 operates as a differential inverting op amp, there is only modest signal path isolation when disabled as shown in Figure 23. For small input signals, Figure 23 shows about 5dB to 6dB isolation while for large signals, back to back protection diodes across the inputs compress the signal to show actually an improved isolation. This is intended to protect any subsequent devices from large input signals during shutdown. Those diodes limit the maximum overdrive voltage across the input to approximately 0.5V in each polarity. The R_G resistors of Test Circuit #1 limit the current into those diodes under this condition.

The supply current in shutdown does not reduce to zero as internal circuitry is still active to hold the output common mode voltage at the V_{CM} control input voltage even during shutdown (or the default value). This is intended to hold the ISL55210 output near the desired common mode output level during shutdown. This improves turn on characteristic and keeps the output voltages in a safe range for downstream circuitry.

DISABLED OPERATION WARNING IN DC COUPLED DESIGNS

When disabled, the output stage provides a nominal DC voltage at the Vcm control pin input or the default internal 1.2V value. Being very low power, any external circuit condition that can cause the output pins to source or sink DC current can move the ISL55210 internal operating points into regions from which it may not recover when the device is enabled. If the external circuitry can force >20µA into the output pins or pull > 1.5mA out of the output pins correct operation is not guaranteed. For designs that might force current into the output stage during disable, adding a resistor to ground on the outputs might provide

an effective means of turning that into a low sourcing current condition with minimal impact to the desired signal path operation when enabled.

The very low internal power dissipation of the ISL55210, along with the excellent thermal conductivity of the QFN package when the exposed metal pad is tied to a conductive plate, reduces the T_J rise above ambient to very modest levels. Assuming a nominal 115mW dissipation and using the +63°C/W measured thermal impedance from Junction to ambient, gives a rise of only 0.12 * 63 = +7.6°C. Operation at elevated ambient temperatures is easily supported given this very low internal rise to junction.

The maximum internal junction temperatures would occur at maximum supply voltage, +85°C maximum ambient operating, and where the QFN exposed pad is not tied to a conductive layer. Where the QFN must be mounted with an insulating layer to the exposed metal plate, such as in a split supply application, device measurements show an increased thermal impedance junction to ambient of +120°C/W. Using this, and a maximum quiescent internal power on 4.5V absolute maximum, which shows 45mA for +85°C maximum operating ambient from Figure 27, we get 4.5V * 45mA * +120°C/W = +24°C rise above +85°C or approximately +109°C operating T_J maximum - still well below the specified Absolute Maximum operating junction temperature of +135°C.

Noise Analysis

The decompensated voltage feedback design of the ISL55210 provides very low input voltage and current noise. While a detailed noise model using arbitrary external resistors can be made, most applications will have a balanced feedback network with the two R_F (feedback) resistors equal and the two R_G (gain) resistors equal. Figure 33 shows the test circuit used to measure the output noise with the noise terms detailed. The aim here was to measure the output noise with two different resistor settings to extract out a model for the input referred En and In terms for just the amplifier itself.

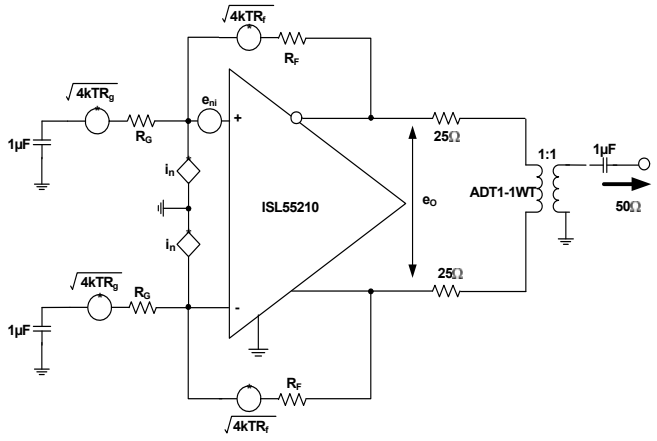


FIGURE 33. NOISE MODEL AND TEST CIRCUIT

With equal feedback and gain resistors, the total output noise expression becomes very simple. This is:

$$e_0 = \sqrt{(e_{ni} \bullet NG)^2 + 2(i_n R_f)^2 + 2(4kTR_f NG)} \quad \text{(EQ. 1)}$$

The NG term in Equation 1 is the Noise Gain = 1 + R_F/R_G. The last term in Equation 1 captures both the R_F and R_G resistor noise terms. If we assume a 50Ω source in Test Circuit #1, the total R_G resistor value will be 100Ω as that 50Ω will come through the transformer to look like a 50Ω source on each side. This gives a lower noise gain (3V/V) than signal gain (4V/V) for just the amplifier. The total gain in Test Circuit #1 is still approximately 1.4 * 4 = 5.6V/V including the transformer step up.

Putting in NG = 3, R_F = 200Ω, R_G = 100Ω with the ISL55210 noise terms of e_{ni} = 0.85nV/√Hz and In = 5pA/√Hz into Equation 1 (4kT = 1.6E - 20J) gives a total output differential noise voltage = 5.26nV/√Hz. Input referring this to the input side of the transformer of Test Circuit #1 gives an input referred spot noise of only 0.88nV/√Hz. This extremely low input referred noise is a combination of low amplifier noise terms and the effect of the input transformer configuration.

Driving Cap and Filter Loads

Most applications will drive a resistive or filter load. The ISL55210 is robust to direct capacitive load on the outputs up to approximately 10pF. For frequency response flatness, it is best to avoid any output pin capacitance as much as possible - as that capacitance increases, the high frequency portion of the ISL55210 (>1GHz) response will start to show considerable peaking. No oscillations were observed up through 10pF load on each output.

For AC coupled applications, an output network that is a small series resistor (10Ω to 50Ω) into a blocking cap is preferred. This series resistor will isolate parasitic capacitance to ground from the internally closed loop output stage of the amplifier and de-queue the self resonance of the blocking capacitors. Once the output stage sees this resistive element first, the remaining part of the filter design can be done without fear of amplifier instability.

Driving ADCs

Many of the intended applications for the ISL55210 are as a low power, very high dynamic range, last stage interface to high performance ADCs. The lowest power ADCs, such as the ISLA112P50 shown on the front page, include an innovative "Femto-Charge" internal architecture that eliminates op amps from the ADC design and only passes signal charge from stage to stage. This greatly reduces the required quiescent power for these ADCs but then that signal charge has to be provided by the external circuit at the two input pins. This appears on an ADC like the ISLA112P50 as a clock rate dependent common mode input current that must be supplied by the interface circuit. At 500MHz, this DC current is 1.3mA on each input for the ISLA112P50.

Most interfaces will also include an interstage noise power bandlimiting filter between the amplifier and the ADC. This filter needs to be designed considering the loading of the amplifier,

any V_{CM} level shifting that needs to take place, the filter shape, and this I_{CM} issue into the ADC input pins. Here are 4 example topologies suitable for different situations.

1. AC coupled, broadband RLC interstage filter design. This approach lets the amplifier operate at its desired output common mode, then provides the ADC common mode voltage and current through a bias path as part of the filter design's last stage R values. The V_B is set to include the IR loss from that voltage to the ADC inputs due to the I_{CM} current. This circuit is the one shown on the front page where we get a usable frequency range from about 500kHz to 150MHz.

2. AC coupled, higher frequency range interstage filter design. This design replaces the R_t resistors in Figure 34 with large valued inductors and implements the filter just using shunt resistors at the end of the RLC filter (here, that is just the ADC internal differential Rin). In this case, the ADC V_{CM} can be tied to the centerpoint of the bias path inductors (very much like a Bias-T) to provide the common mode voltage and current to the ADC inputs. These bias inductors do limit the low frequency end of the operation where, with 1µH values, operation from 10MHz to 200MHz is supported using the approach of Figure 35.

3. AC coupled with output side transformer. This design includes an output side transformer, very similar to ADC characterization circuits. This approach allows a slightly lower amplifier output swing (if N > 1 is used) and very easy 2nd order low pass responses to be implemented. It also provides the I_{CM} and V_{CM} bias to the ADC through the transformer centertap. This approach would be attractive for higher ADC input swing targets and more aggressive noise power bandwidth control needs.

4. DC coupled with ADC V_{CM} and I_{CM} provided from the amplifier. Here, DC to very high frequency interstage low pass filters can be provided. Again, the R_S element must be low to reduce the IR drop from the V_{CM} of the converter, which now shows up on the output of the ISL55210, to the ADC input pins. In this case, split supplies are required to satisfy the amplifier output and input common mode range limits discussed earlier.

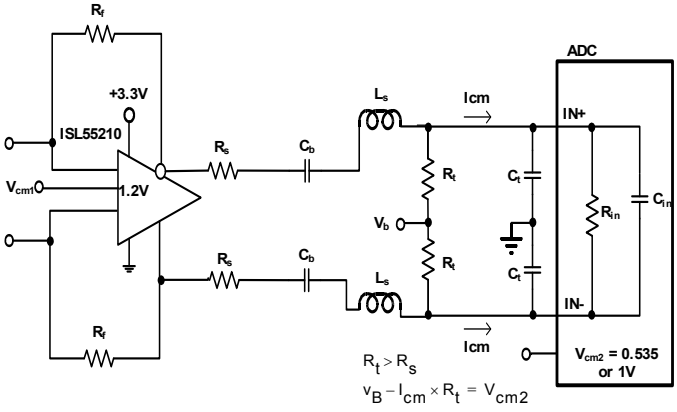


FIGURE 34. AC COUPLED, BROADBAND RLC INTERSTAGE FILTER DE SIGN

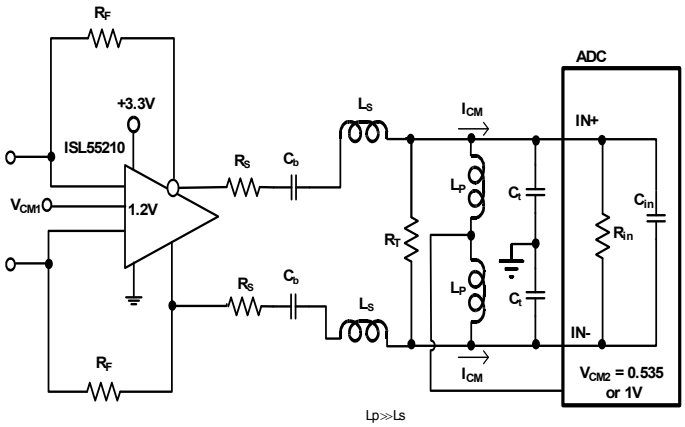


FIGURE 35. AC COUPLED, HIGHER FREQUENCY RLC FILTER DESIGN

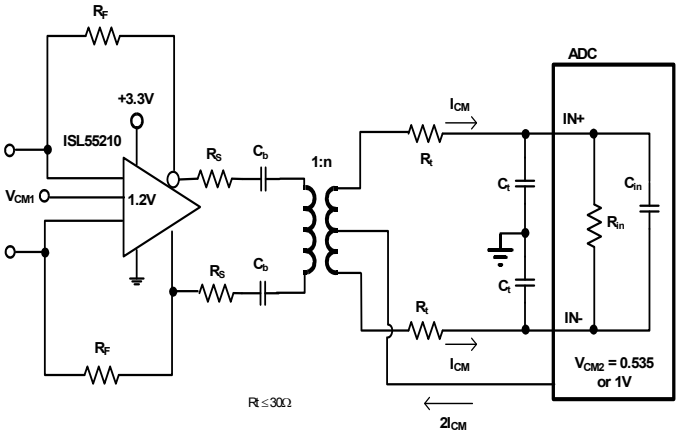


FIGURE 36. AC COUPLED WITH OUTPUT SIDE TRANSFORMER

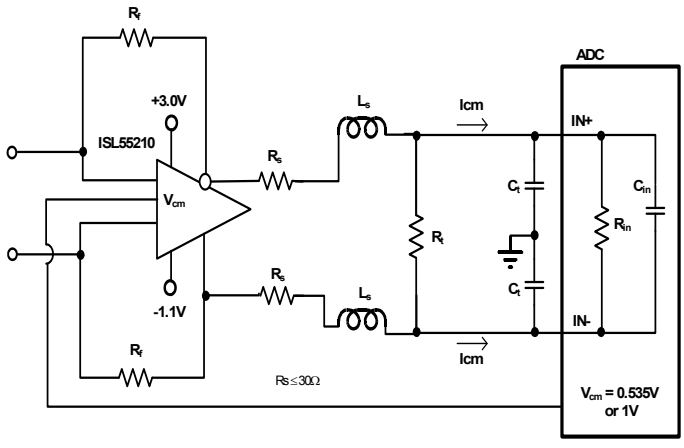


FIGURE 37. DC COUPLED WITH A COMMON V_{CM} VOLTAGE FROM THE ADC

Layout Considerations

The ISL55210 pinout is organized to isolate signal I/O along one axis of the package with ground, power and control pins on the other axis. Ground and power should be planes coming into the upper and lower sides of the package (see the Pin Configuration on page 1). The signal I/O should be laid out as tight as possible with parasitic C to the ground and/or power planes reduced as much as possible by opening up those planes under the I/O elements.

The ground pins and package backside metal contact should be connected into a good ground plane. The power supply should have both a large value electrolytic cap to ground, then a high frequency ferrite beads, then 0.01µF SMD ceramic caps at the supply pins. Some improvement in HD2 performance may be experienced by placing and X2Y cap between the two V_{S+} pins and ground underneath the package on the board back side. This is 4 terminal device that is included in the EVM board layout.

EVM Board (Rev. C)

Test circuit #1 (Figure 28) is implemented on an Evaluation Module Board available from Intersil. This board includes a number of optional features that are not populated as the board is delivered. The full EVM board circuit is shown in Figure 38 where unloaded (optional) elements are shown in green.

The nominal supply voltage for the board and device is a single 3.3V supply. From this, the ISL55210, ISL55211 generates an internal common mode voltage of approximately 1.2V. That voltage can be overridden by populating the two resistors and potentiometer shown as R19 to R21 above.

The primary test purpose for this board is to implement different interstage differential passive filters intended for the ADC interface along with the ADC input impedances. The board is delivered with only the output R's loaded to give a 200Ω differential load. This is done using the two 85Ω resistors as R9 and R10, then the 4 zero ohm elements (R10, R12, R24, and R25) and finally the two shunt elements R13 and R14 set to 35.5Ω. Including the 50Ω measurement load on the output side of the 1:1 transformer reflecting in parallel with the two 35Ω resistors takes the nominal AC shunt impedance to 71Ω||50Ω = 29.3Ω. This adds to the two 85Ω series output elements to give a total load across the amplifier outputs of 170Ω + 29.3Ω = 199.3Ω.

To test a particular ADC interface RLC filter and converter input impedance, replace R11 and R12 with RF chip inductors, load C10 and C11 with the specified ADC input capacitance and R26 with the specified ADC differential input R. With these loaded, the remaining resistive elements (R24, R25, R13, R14) are set to hit a desired total parallel impedance to implement the desired filter (must be < than the ADC input differential R since that sits in parallel with any "external" elements) and achieve a 25Ω source looking into each side of the tap point transformer.

This EVM board includes a user's manual showing a number of example circuits and tested results. Available on the Intersil web site in the ISL55210 Product Information Page.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 6, 2013	FN7811.2	Added Related Literature on page 1. Updated Figure “NOISE MODEL AND TEST CIRCUIT” on page 14 that was incorrectly drawn.
July 30, 2012	FN7811.1	Added 6th paragraph to section “Power Supply, Shutdown, and Thermal Considerations” on page 13 describing the outputs can not source or sink current during disable mode.
March 2, 2011	FN7811.0	Initial Release

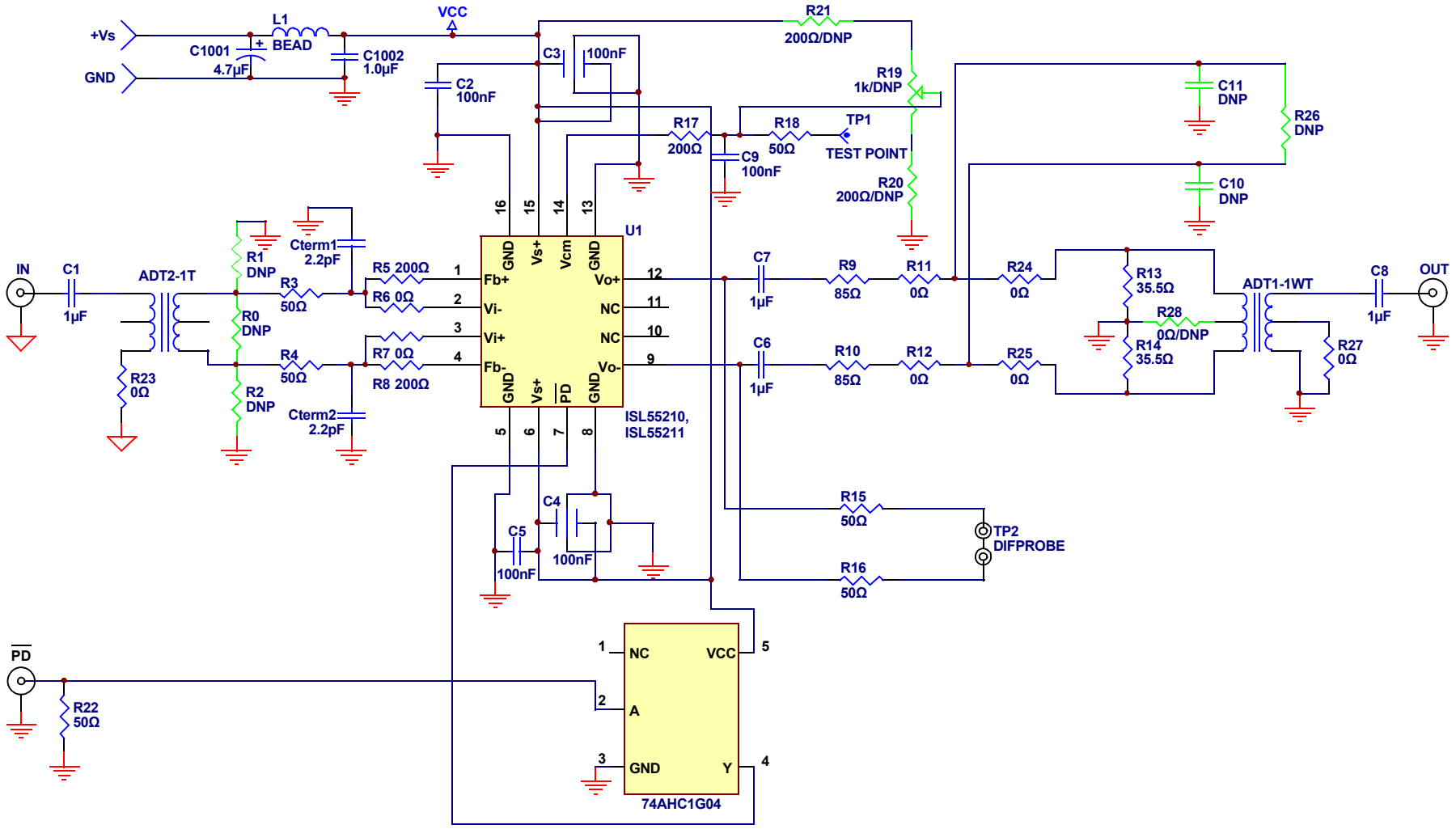


FIGURE 38. SCHEMATIC FOR ISL55210, ISL55211 SINGLE INPUT TRANSFORMER EVM REV. C

About Intersil

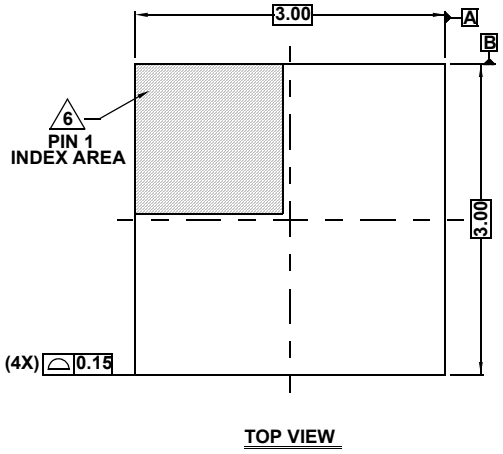
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

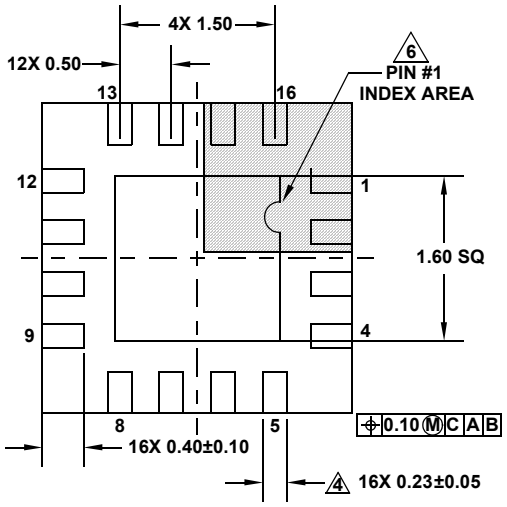
Package Outline Drawing

L16.3x3D

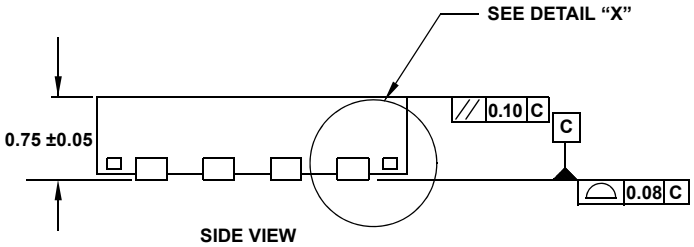
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 3/10



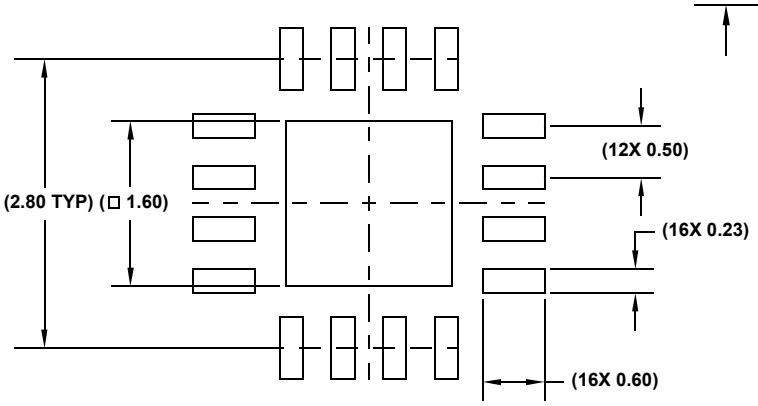
TOP VIEW



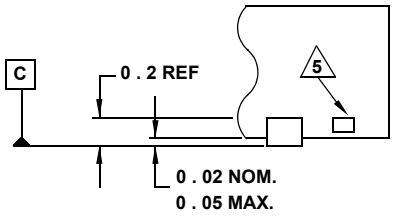
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.