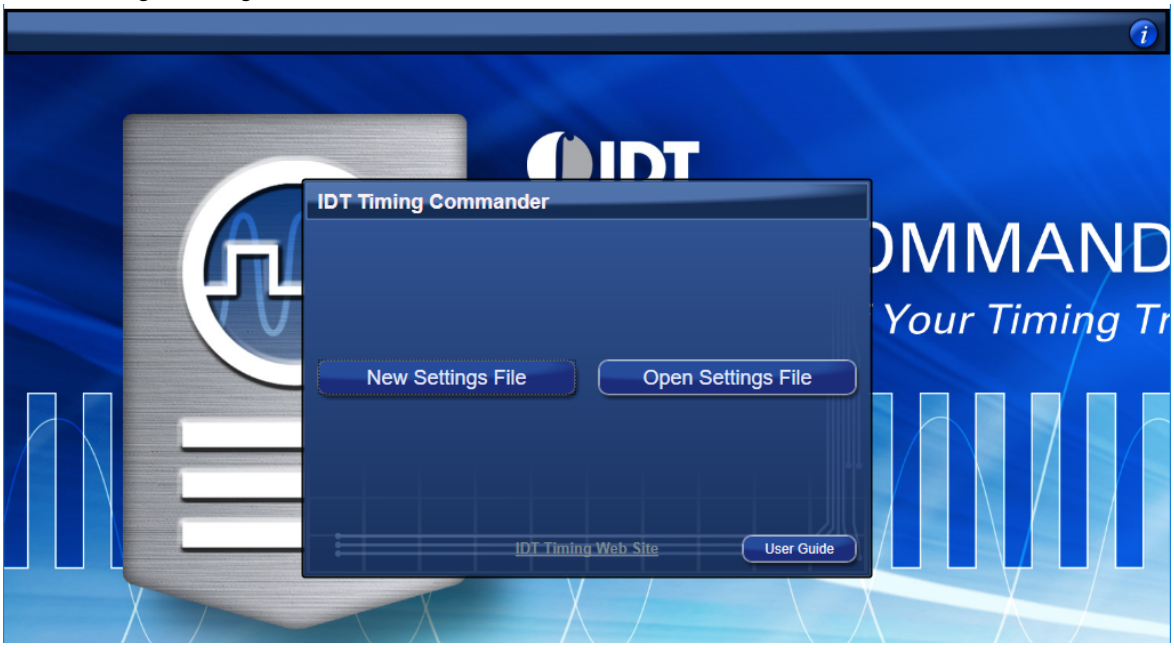
Getting Started

Follow the steps below to start a new setting or open an existing Settings File and configure the device to meet your timing requirements.

Note: Ensure to install the latest Timing Commander version before proceeding with the next step.

1. Launch Timing Commander GUI – upon launching the software for the first time, you will see the following window:

Figure 1. Launching Timing Commander for the First Time



A settings file (.tcs) is a text file where the device input and output requirements are stored. From this window, an existing setting file can be opened to restore a configuration, or a new setting file can be created.

2. Click on "New Setting File" button – a personality file (.tcp) will be requested and can be opened by browsing to the folder where a personality file is stored. Once the personality file is opened (click OK), the following page will be displayed, where the PhiClock plus PCIe Clock Generator product can be selected (see Figure 2). As soon as the product is selected, a configuration window for the selected product will appear as in Figure 4.

Figure 2. Choosing the Correct PhiClock plus PCIe Clock Generator Part Number

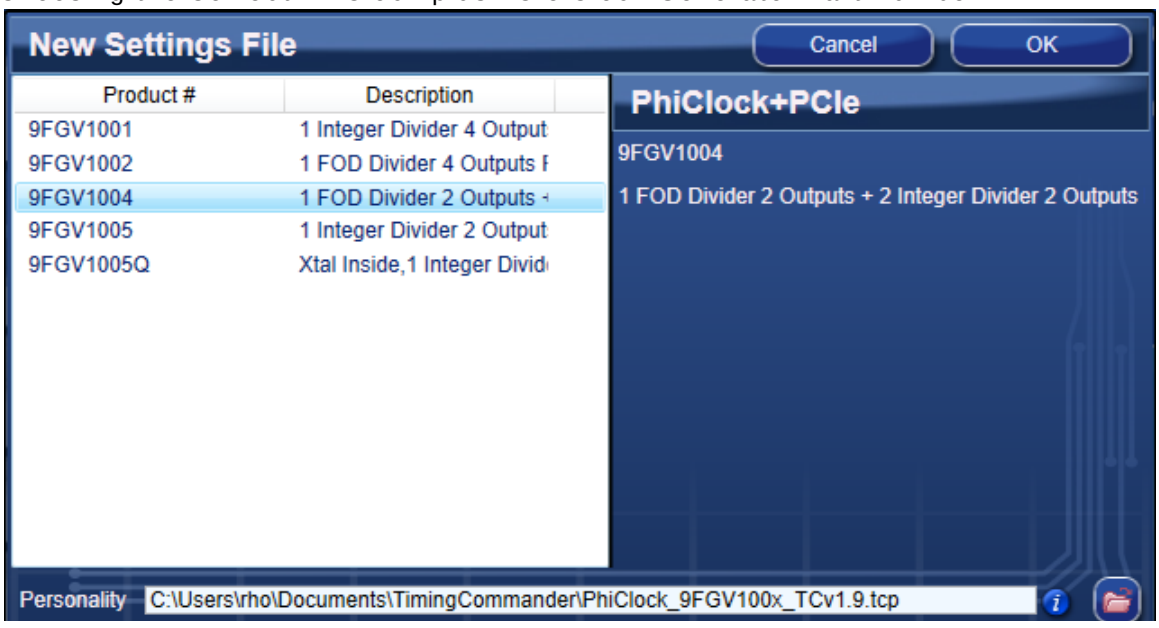
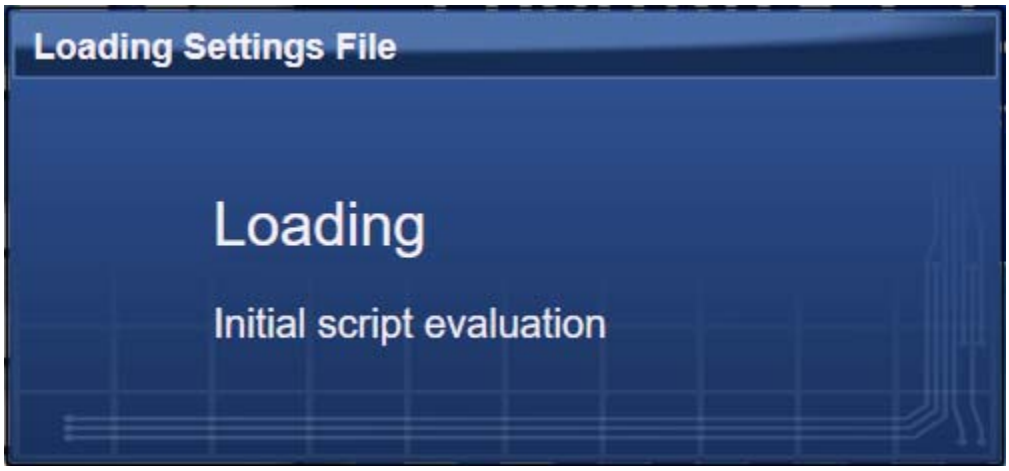


Figure 3. Loading Settings File Window



Settings File Window Fields and Descriptions

A block diagram is displayed when a Settings File is loaded with a personality of a device. The different areas of the block diagram are shown in Figure 4, along with detailed explanations of the labels in Table 1.

Figure 4. 9FGV1004 Settings File Window Descriptions

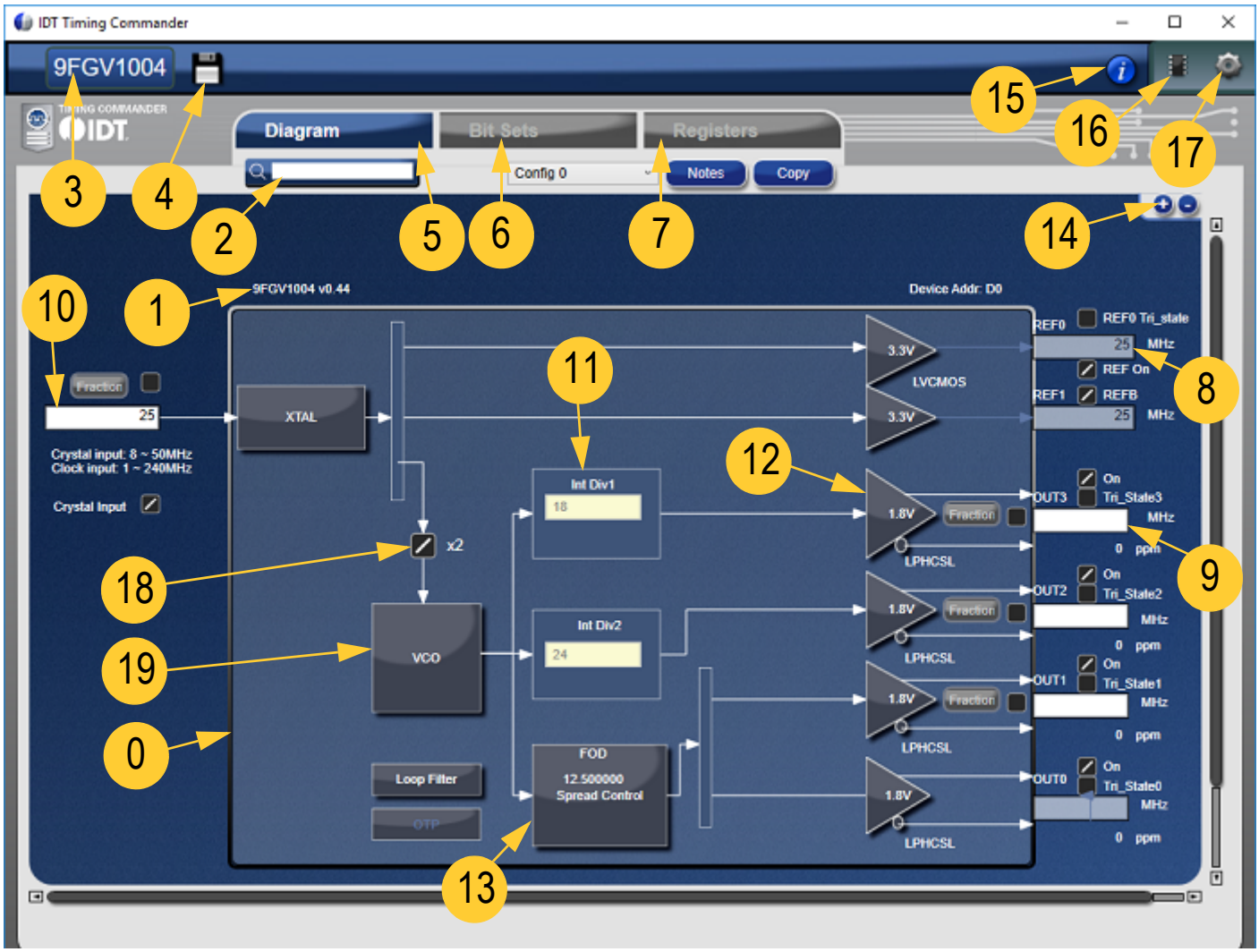


Table 1. 9FGV1004 Settings File Window Label Descriptions

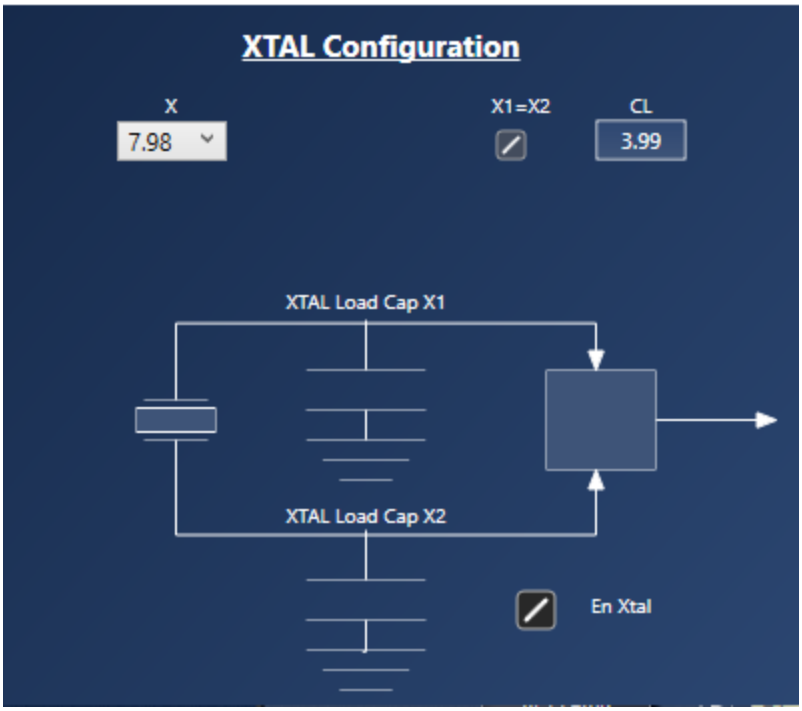
Label Number	Timing Commander Field Name	Description
0	9FGV100x	The detailed block diagram of the selected device.
1	9FGV100x vn.nn	Personality revision.
2	Search Box	This is used to search for items on the screen.
3	9FGV100x	Part number corresponding to the personality being used.
4	Save	Enable to save the current configuration as a .tcs file.
5	Diagram	Default tab.
6	Bit Sets	Tab that shows all bit set used in this personality for 9FGV100x.
7	Registers	Register table tab shows all register bits settings and address.
8	Enable Check Box	If checked it enables the corresponding outputs.
9	Output Frequency	Field to enter the output frequencies.
10	Source Frequency	Field to enter the source frequency either as crystal or input clock.
11	Integer Divider	Integer divider factor.
12	VDDO	Drop down button to enter the voltage for each output.
13	Spread Spectrum	Enable or disable the spread spectrum feature on the selected outputs.
14	+ -	Enable to zoom in or zoom out the tab.
15	*i*	Display information about timing commander.
16	Connect	Enable the connection to the evaluation board.
17	Settings	Setting window for I^2C connection.
18	x2	Input clock doubler.
19	VCO	VCO frequency setting.

Input Clock Selection

Input source can be selected between a crystal and an external reference clock. The frequency can be entered under “Source Frequency”. There are two source options – crystal and clock. The maximum input frequency the crystal supports is 50MHz, and maximum input frequency from clock should be 200MHz. The “Source Frequency” (see Figure 5) can be entered as a fraction by clicking on the *Fraction* check box.

Figure 5. Input Clock Reference Selection

Figure 6. Crystal Tuning



If the source is a crystal, clicking the XTAL block displays the XTAL Configuration popup window (see Figure 6), and the frequency of the crystal can be tuned by adding a total load capacitance of 4–14pF between X1 and X2.

Output Selection and Configuration

There are 4 copies of output pairs from the PLL, and two single-ended REF outputs. Clicking on one of the output drivers displays the "Output Clock Configuration" popup (see Figure 7), where all outputs can be enabled and configured individually or by applying global settings by clicking on the "Apply global settings to all outputs" button. Table 2 outlines the signal types, while Table 3 summarizes the output voltages available for various output types. Table 3 also summarizes the default settings upon power-up. There is an option for the LP-HCSL outputs to be configured as PCIe outputs by selecting the "Set PCIeSig Default" button.

Figure 7. Output Clock Configuration Window

Table 2. Output – Signal Type

Signal Type	Number of Outputs	Output Type
LVCMOS	1	Single-ended for REF0/REF1.
LVCMOS1	1	Single-ended output.
LVCMOSX2	2	Two copies of the True terminal from OUT0–OUT3.
LVCMOSD	2	Two copies of the True and Complement from OUT0–OUT3.
LVDS	2	Differential OUT0–OUT3.
LP-HCSL	2	Differential OUT0–OUT3.

Table 3. Output – VDDO

VDDO (V)	Available for Output Types
1.8	All differential and single-ended output types.
2.5	All differential and single-ended output types.
3.3	All differential and single-ended output types.

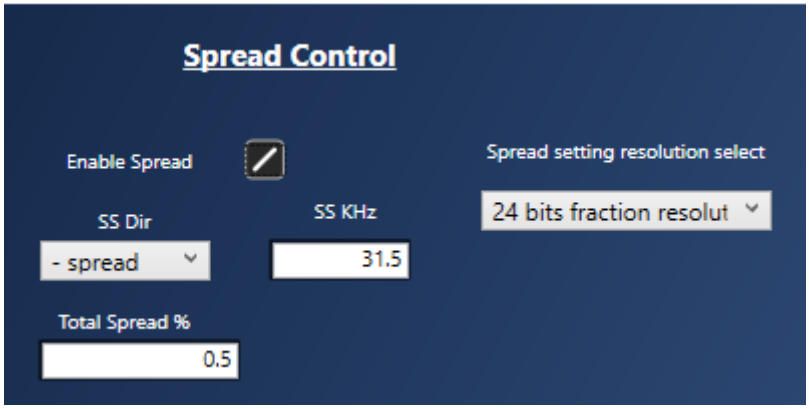
Table 4. Factory Defaults

Output Type	Frequency (MHz)	Signal Type	VDDO (V)
REF Output 0	25	LVCMOS	3.3
REF Output 1	25	LVCMOS	3.3
Differential 0	100	LP-HCSL	3.3
Differential 1	100	LP-HCSL	3.3
Differential 2	100	LP-HCSL	3.3
Differential 3	100	LP-HCSL	3.3

Spread Spectrum

Note: Only 9FGV1004 has the spread spectrum function. Clicking on the “FOD” block displays the *Spread Control* settings window (see Figure 8). The “Enable Spread” button enables or disables the spread spectrum as required by the user. Note that the spread spectrum is only available for differential outputs OUT0 and OUT1. The “Total Spread %” field accepts values from 0 to 0.5%, while the “SS Dir” and “SS KHz” fields are used to set the spread direction (center or down) and spread modulation frequency (31.5kHz) respectively.

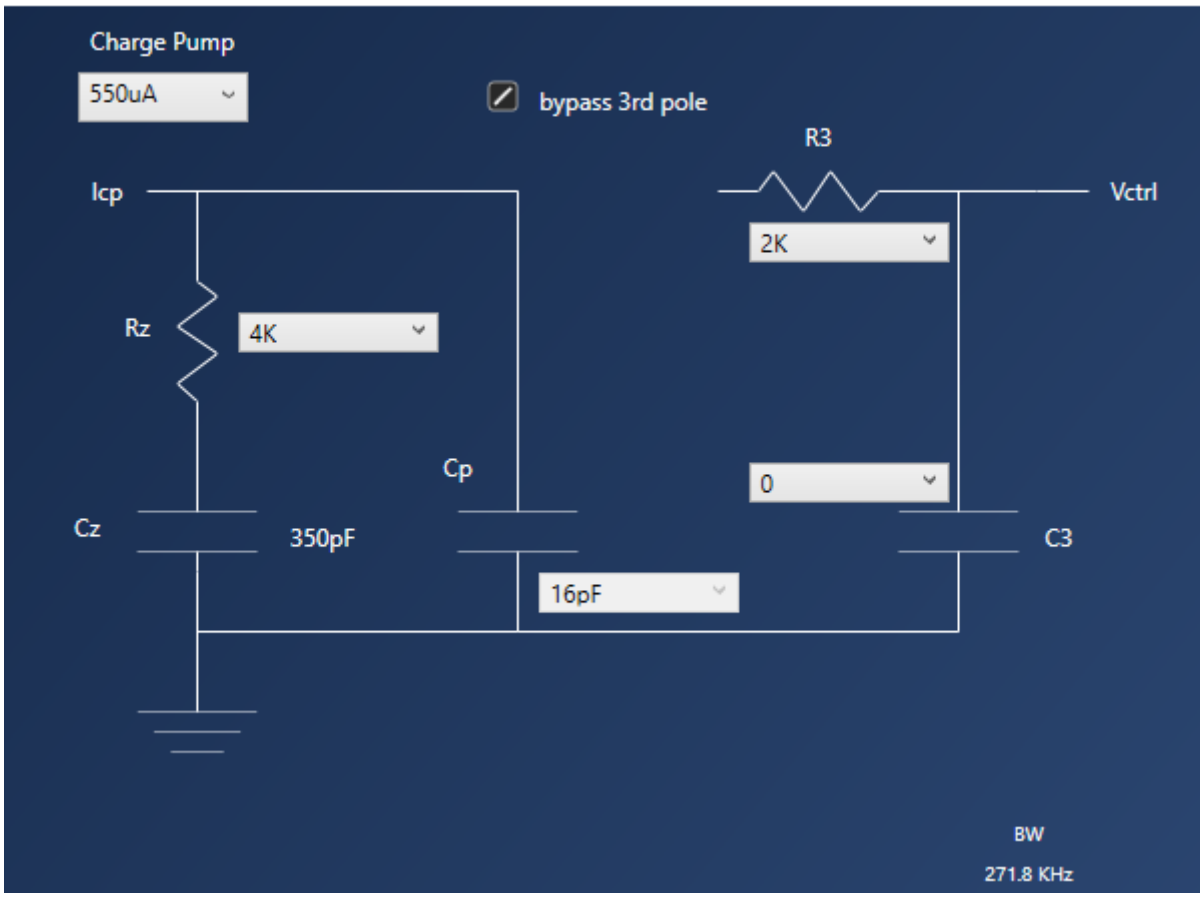
Figure 8. Spread Control Window



PLL Loop Filter

Clicking on the “Loop Filter” block displays the Loop Filter Configuration window. The charge pump current, Rz, and 3rd pole filter settings can be trimmed to optimize the PLL loop parameters and bandwidth.

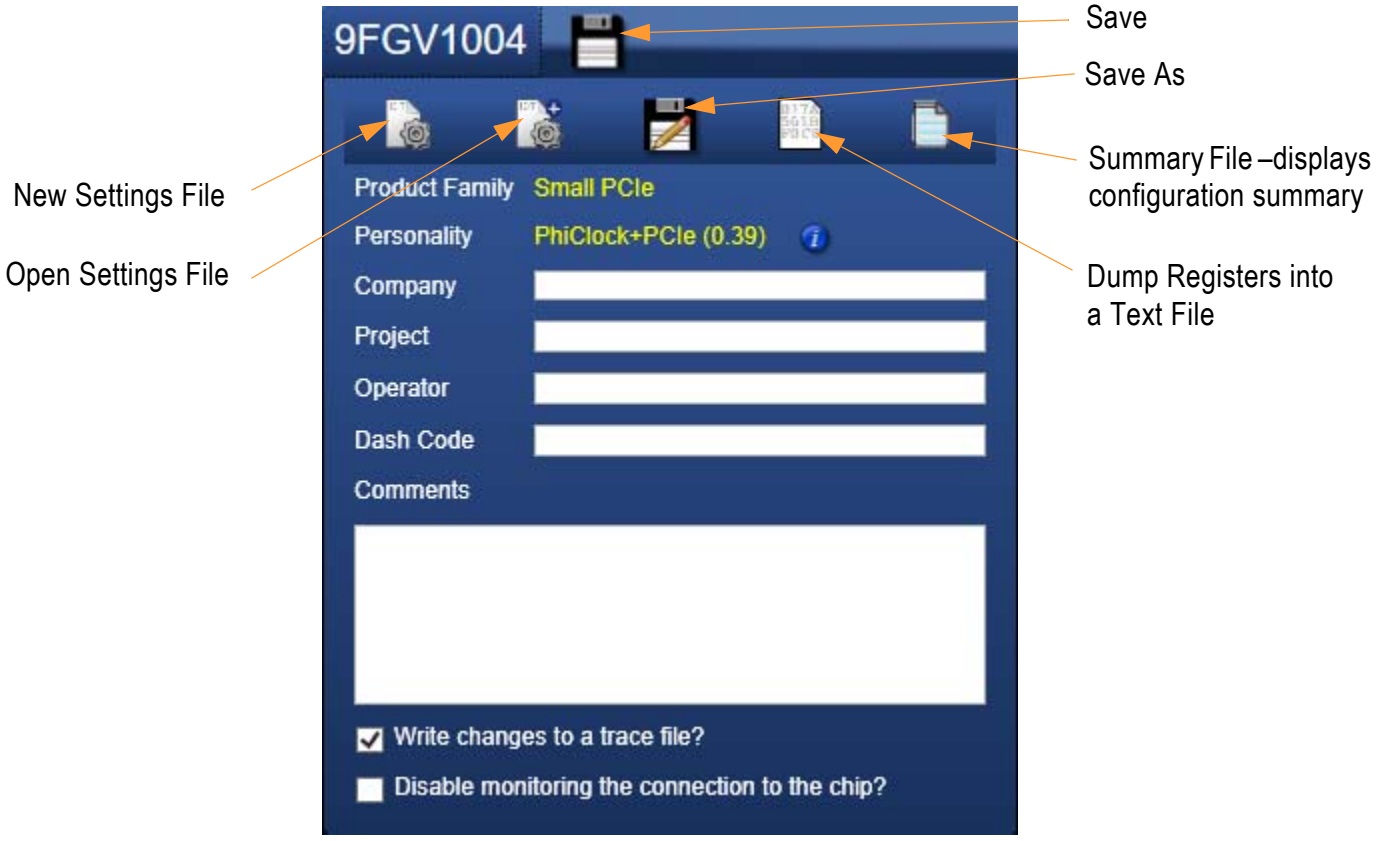
Figure 9. PLL Loop Filter Configuration Window



Entering Project Details

By clicking on the 9FGV100x part number, a window displays tasks that can be performed such as opening settings files, new settings file, save as, and entering project details. These should be filled out for proper documentation.

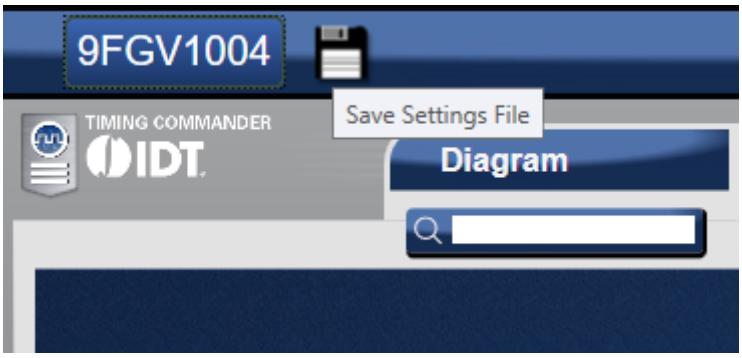
Figure 10. Project Details Information and File Tools Window



Save the Settings File

After the configuration is complete, click on the disk symbol at the upper left corner to save the setting file (see Figure 11).

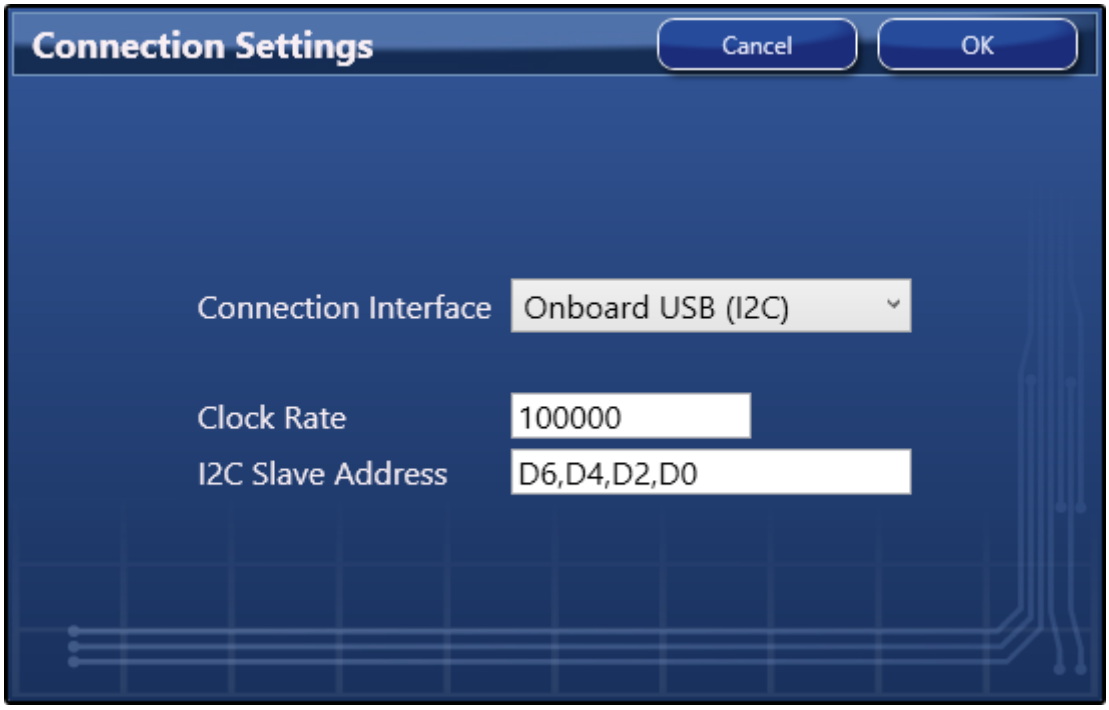
Figure 11. Save the Settings File Window



Connecting to the Chip

If a 9FGV100x evaluation board is connected, the settings can be written to the chip registers through the I^2C interface. In the GUI software, the connection to the chip can be made by clicking on the round button at upper right corner of the GUI (see Figure 4, label 17). The “Connections Settings” window displays as shown in Figure 12.

Figure 12. Connection Settings Window for Connecting to the Chip



Use the default values in *Connection Settings* window and click OK to close it. Click the chip symbol in the upper right corner (see Figure 4, label 16) to start the read/write command. While connecting, the read/write indicators are red, and when connected and functioning, the indicators change from red to green with “read” or “write” indicators (see Figure 13). The arrow pointing out of the chip means “reading from the chip”; the arrow pointing into the chip means “writing to the chip”.

To read from the device, ensure that the device configuration is written at least once and the proper configuration is selected for read back.

Figure 13. Read/Write to Device Registers Symbols

OTP Programming

When a configuration is ready for programming, the chip can be programmed directly within the Timing Commander GUI software.

1. Before starting the OTP burn process, it is important to disable the monitoring connection to the chip as shown in Figure 15.
2. Set Auto Poll to “NO” as shown in Figure 16.
3. Click on the OTP button to display the “OTP” programing window (see Figure 14).
4. Within this window, select the configurations needed to OTP. It can OTP one configuration at a time, but the config0 must be OTP at the first time.
5. Disconnect the OTP_VPP pin on the Evaluation/Programming board from V_{DDD} and connect to 6V. See Figure 16.
6. Click “Burn 4 Cfgs” button.
7. To complete the OTP process, remove 6V V_{DDD} and plug in 3.3V V_{DDD} jumper.

Figure 14. OTP Programming Window

Figure 15. Disable Monitoring the Connection to the Chip

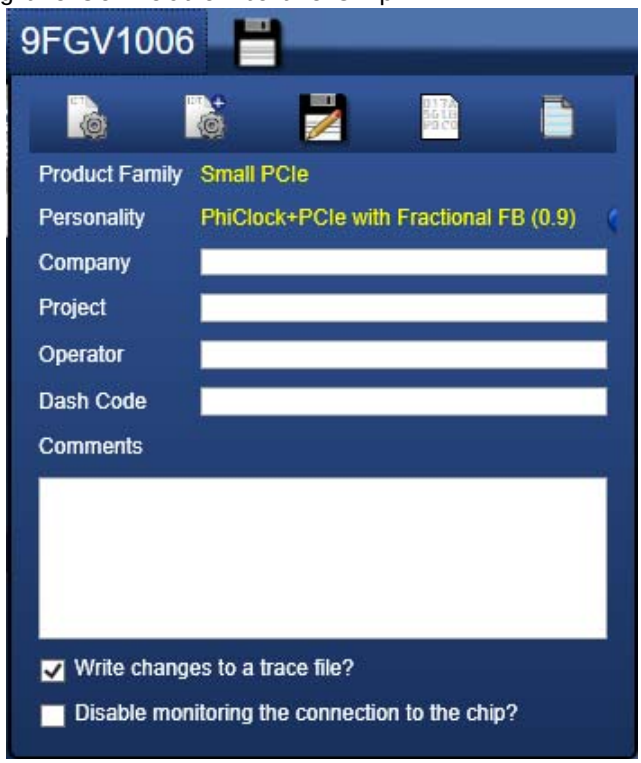


Figure 16. Setting Auto Poll to “No”

Glossary

IDT Timing Commander Software – Executable file that will execute a personality, connect to a timing chip on an evaluation board, and read or write settings files.

Personality – Encrypted file with an extension .tcp. Used by IDT Timing Commander software to determine the characteristics for a specific family of timing devices. A personality file may refer to a single device or an entire family of similar devices. Contact IDT to obtain the most current version of a personality file for the devices of interest.

Settings File – Text file with extension .tcs. Written or read by IDT Timing Commander software to save or restore a particular setup for a specific version of a device personality and version of IDT Timing Commander software. Settings files created with newer versions of IDT Timing Commander software or a device personality may not be compatible when read into older version of IDT Timing Commander software, or, if an older version of the personality is installed. Forward compatibility (older settings files read by newer software and/or personality) will be maintained.

Bit Set – A single variable stored within the registers of the device. A bit set may use only part of a register or many span multiple registers, but is thought of as a single field. For example, a 20-bit output divider ratio may be defined as a single bit set of length 20-bits, but may be stored in Register 0x4A, bits [3:0], Register 0x4B, bits [7:0] and Register 0x4c, bits [7:0].

Metadata – Variable used within the personality, but not stored directly in device registers. For example, an output frequency is generally not stored anywhere in a device's registers, but must be known to calculate register settings for the device with which we achieve those frequencies.

Tooltip – Context-sensitive pop-up that appears briefly as the mouse pointer hovers over an icon or element on the screen. These are intended to provide useful information about the specific hovered-over item.

Value – When referring to any field that the user can edit, Value means the current internally-represented value of that field.

Default Value – When referring to any field that the user can edit, Default Value means the value recommended by the personality for that field, taking into account the settings in other fields in the device. Changes of other fields may result in a change to the Default Value. Whenever a field is unlocked, Default Value = Value. Only by locking a field can a user set a field to a value other than the Default Value or prevent a field's Value from changing if Default Value changes.

Display Value – A field may be controlled by a personality to display its Value or Default Value in a more meaningful way. For example, if the value is defined in MHz, but the actual value is 0.008MHz, the personality may choose to display this to the user as 8kHz. In another example, if a bit set represents a divider ratio that can only be an even number and so does not implement the least significant bit, the personality may choose to show a divider ratio of 2 when the bit set value is 1 (i.e., 1 increment of divide-by-2).

Revision History

Revision Date	Description of Change
February 23, 2018	▪ Corrected minor typos throughout. ▪ Updated *OTP Programming* section. ▪ Updated images for figures 4 and 5. ▪ Moved Glossary to be the last section of the document.
November 22, 2017	Initial release.

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