MP8862

2.8V-22V V_{IN}, 2A I_{OUT}, 4-Switch, Integrated Buck-Boost Converter with I^2C Interface

DESCRIPTION

The MP8862 is a synchronous, 4-switch, integrated buck-boost converter capable of regulating the output voltage across a 2.8V to 22V wide input voltage range with high efficiency.

The MP8862 uses constant-on-time (COT) control in buck mode and constant-off-time control in boost mode, providing fast load transient response and smooth buck-boost mode transient. The MP8862 provides auto PFM/PWM or forced PWM switching modes, and programmable output constant current (CC) current limit, which support flexible design for different applications.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), programmable soft start, and thermal shutdown.

The MP8862 is available in a 16-pin QFN (3mmx3mm) package.

FEATURES

- Wide 2.8V to 22V Operating Input Voltage Range
- 1V (1) to 20.47V Output Voltage Range (5V Default) with 10mV Resolution through I^2C
- 2A Output Current or 4A Input Current
- Four Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- Adjustable Accurate CC Output Current Limit with Internal Sensing MOSFET via I^2C
- 500kHz (1) Switching Frequency
- Output Over-Voltage Protection (OVP) Hiccup
- Output Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Warning and Shutdown
- I^2C Interface with ALT Pin
- Four Programmable I^2C Addresses
- One-Time Programmable (OTP) Non-Volatile Memory
- I^2C Programmable Line Drop Compensation, PFM/PWM Mode, Soft Start, and OCP, etc.
- EN Shutdown Discharge Programmable
- Available in a QFN-16 (3mmx3mm) Package

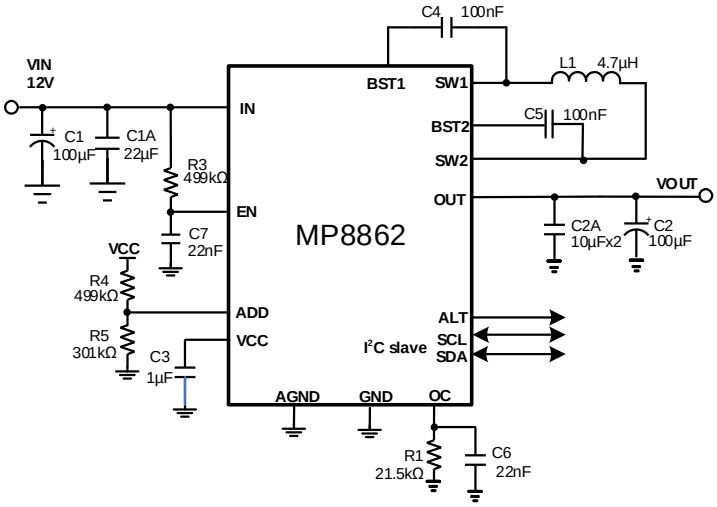
APPLICATIONS

- Buck-Boost Bus Supplies
- Industrial Systems
- Personal Medical Products
- DSLR Cameras

Note:

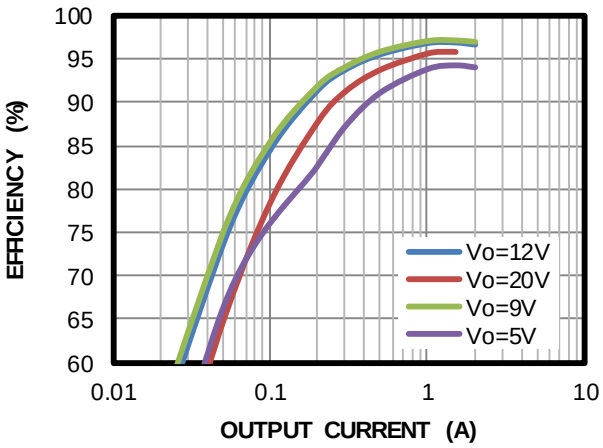
1) For V_{OUT} < 3V applications, the switching frequency decreases.

TYPICAL APPLICATION



Efficiency

V_{IN} = 12V, V_{OUT} = 5V to 20V, L = 4.7µH, R_{DC} = 19.5mΩ, forced PWM mode



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8862GQ-xxxx**	QFN-16 (3mmx3mm)	*See Below*
MP8862GQ-0000	QFN-16 (3mmx3mm)	*See Below*
EVKT-MP8862	Evaluation kit	

* For Tape & Reel, add suffix –Z (e.g. MP8862GQ-XXXX–Z).

** "xxxx" is the configuration code identifier for the register setting stored in the OTP. The default number is "0000". Each "x" can be a hexadecimal value between 0 and F. Please work with an MPS FAE to create this unique number, even if ordering the "0000" code. MP8862GQ-0000 is the default version.

TOP MARKING

BJTY
LLL

BJT: Product code of MP8862GQ
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP8862

EVKT-MP8862 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV8862-Q-00A	MP8862GQ-0000 evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1

Order directly from MonolithicPower.com or our distributors.

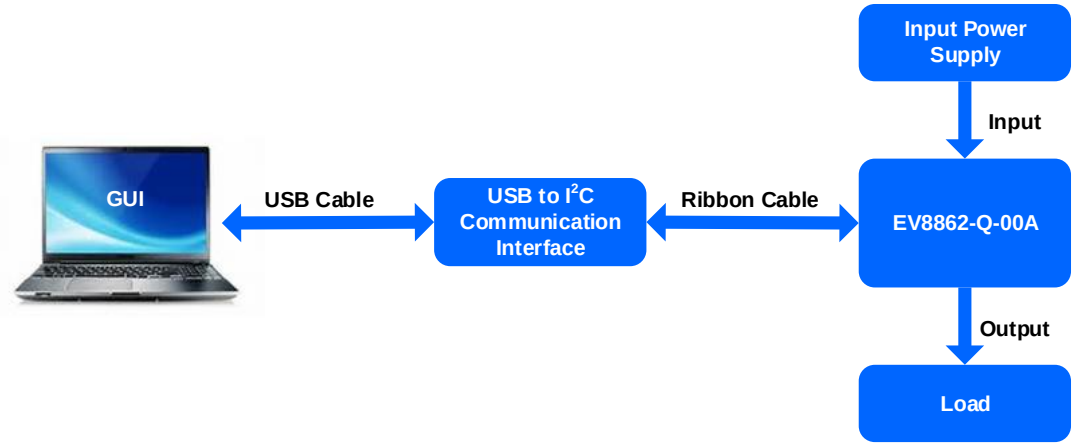
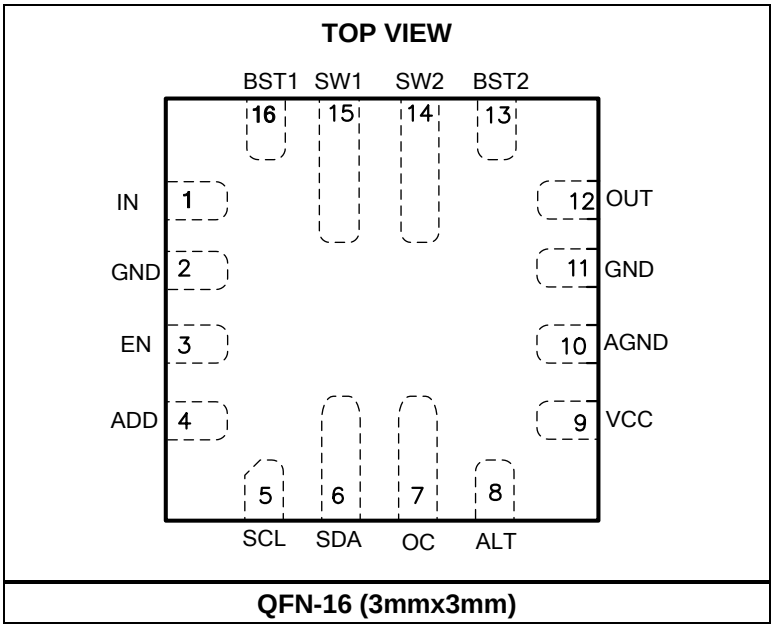


Figure 1: EVKT-MP8862 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Supply voltage.** IN is the drain of the internal power device and provides power to the entire chip. The MP8862 operates from a 2.8V to 22V input voltage. A capacitor (C_{IN}) is required to prevent large voltage spikes from appearing at the input. Place C_{IN} as close to the IC as possible.
2, 11	GND	**Power ground.** GND is the reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect GND with copper traces and vias.
3	EN	**On/off control for entire chip.** Drive EN high to turn on the chip. Drive EN low or float EN to turn off the device. EN has an internal 2MΩ pull-down resistor to ground.
4	ADD	**I^2C slave addresses program pin.** Connect a resistor divider from VCC to ADD to set four different I^2C slave addresses.
5	SCL	**Clock pin of the I^2C interface.** SCL can support an I^2C clock up to 3.4MHz.
6	SDA	**Data pin of the I^2C interface.**
7	OC	**Output constant current limit set pin.**
8	ALT	**Alert output.** ALT pulling to logic low indicates that a fault or warning has occurred.
9	VCC	**Internal 3.65V LDO regulator output.** Decouple VCC with a 1µF capacitor.
10	AGND	**Analog ground.** Connect AGND to GND.
12	OUT	**Output power pin.** Place the output capacitor close to OUT and GND.
13	BST2	**Bootstrap.** Connect a 0.1µF capacitor between SW2 and BST2 to form a floating supply across the high-side switch driver.
14	SW2	**Switching node of the second half-bridge.** Connect one end of the inductor to SW2 for the current to run through the bridge.
15	SW1	**Switching node of the first half-bridge.** Connect one end of the inductor to SW1 for the current to run through the bridge.
16	BST1	**Bootstrap.** Connect a 0.1µF capacitor between SW1 and BST1 to form a floating supply across the high-side switch driver.

ABSOLUTE MAXIMUM RATINGS (2)

Supply voltage (V_{IN}, V_{OUT}) 24V
$V_{SW1, SW2}$ ..... -0.3V (-7V for <10ns) to V_{IN} + 0.3V (26V for <10ns)
$V_{BST1, BST2}$ ..... V_{SWx} + 4V (V_{SWx} + 5V < 10ns)
V_{EN} ..... -0.3V to 24V
V_{ALT} ..... -0.3V to +5.5V
All other pins ..... -0.3V to +4V
Continuous power dissipation (T_A = +25°C) (3) (5) 4.8W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Operation input voltage range ..... 2.8V to 22V
Output voltage range ..... 1V to 20.47V
Output current ..... 2A continuous current or 4A input current
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-16 (3mmx3mm)			
EV8862-Q-00A (5)	26	3	°C/W
JESD51-7 (6)	50	12	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV8862-Q-00A, 4-layer PCB, 64mmx64mm.
6) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

OTP E-Fuse Selection Table by Default (MP8862GQ-0000)

OTP Items	Default Value
Output voltage	5V
IOUT_LIMIT	3A (for 21.5kΩ OC resistor)
Switching frequency	500kHz
Mode	Forced PWM mode
Soft-start time	900μs
Line drop compensation	No line drop compensation
Output voltage discharge mode	Enabled
OCP_OVP protection mode	Hiccup mode
OTP configure code (ID1)	0x00

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		0	3	μA
Supply current (quiescent)	I_Q	Non-switching, I^2C sets PFM mode		1		mA
EN rising threshold	V_{EN_Rising}		1.00	1.10	1.20	V
EN hysteresis	$V_{EN\_Falling}$		65	110	160	mV
EN to ground resistance	R_{EN}	V_{EN} = 2V		2		MΩ
EN on to V_{OUT} > 90% delay	T_{Delay}	See Figure 8		900		μs
VCC regulator	V_{CC}		3.3	3.65	4	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 10mA		1		%
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}		2.50	2.65	2.8	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}		95	160	205	mV
Power Converter						
HS switch on resistance	R_{DSON_HS}	Switch A, D		35	80	mΩ
LS switch on resistance	R_{DSON_LSB}	Switch B, C		30	70	mΩ
Output voltage	V_{OUT}		-1.5%	5.0	+1.5%	V
Output discharge resistance	R_{DIS}			60	100	Ω
Switch leakage	SW_{LKG}	V_{EN} = 0V, $V_{SW1, SW2}$ = 22V, T_J = +25°C			1	μA
		V_{EN} = 0V, $V_{SW1, SW2}$ = 22V, T_J = -40°C to +125°C			5	
Oscillator frequency	Fs	T_J = +25°C	-20%	530	20%	kHz
Minimum on time [8]	T_{ON_MIN1}	Switch A, B, C, D		160		ns
Maximum duty cycle	D_{MAX}	Buck mode, f_{REQ} = 500kHz		85		%
Minimum duty cycle [8]	D_{MIN}	Boost mode, f_{REQ} = 500kHz		15		%
Protection						
Output over-voltage protection	V_{OVP_R}		150	160	170	%
Output OVP recovery	V_{OVP_F}		130	140	150	%
Low-side B valley limit	I_{LIMIT2}	Switch B	6	8	10	A
Low-side C peak current limit	I_{LIMIT3}	Switch C		10		A
Output average current [8]	I_{OUT_LIM1}	V_{OUT} = 5V, over 0-125°C temp range	0.85	1	1.15	A
	I_{OUT_LIM2}	V_{OUT} = 5V, over 0-125°C temp range	-7.5%	3	7.5%	A
Output UV threshold	V_{UVP}	20μs deglitch, UV falling	45%	50%	55%	V_{REF}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ALT sink current capability	$ALT_{\_LOW}$	Sink 4mA		0.2	0.4	V
ALT leakage	$ALT_{\_LKG}$	V_{PULL} = 5V			1	µA
Thermal shutdown rising threshold [8]	T_{STD}			150		°C
Thermal hysteresis [8]	T_{STD_HYS}			20		°C
I^2C Specification [8]						
ADD voltage threshold 1	V_{ADD_1}	ADD pin float		69H		
ADD voltage threshold 2	V_{ADD_2}	R4 = 499kΩ, R5 = 301kΩ		6BH		
ADD voltage threshold 3	V_{ADD_3}	R4 = 301kΩ, R5 = 499kΩ		6DH		
ADD voltage threshold 4	V_{ADD_4}	R4 = 100kΩ		6FH		
ADD to GND pull-down resistor	R_{ADD}			2		MΩ
Input logic high	V_{IH}	I^2C pull-up VDD can be 1.8V to 5V	1.4			V
Input logic low	V_{IL}				0.4	V
Output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	3400	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	$t_{SU.DAT}$		10			ns
Data hold time	$t_{HD.DAT}$		0	60		ns
Set-up time for (repeated) start condition	$t_{SU.STA}$		160			ns
Hold time for (repeated) start condition	$t_{HD.STA}$		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	$T_{SU.STO}$		160			ns
Rise time of SCL and SDA	t_R		10		300	ns
Fall time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF

Notes:

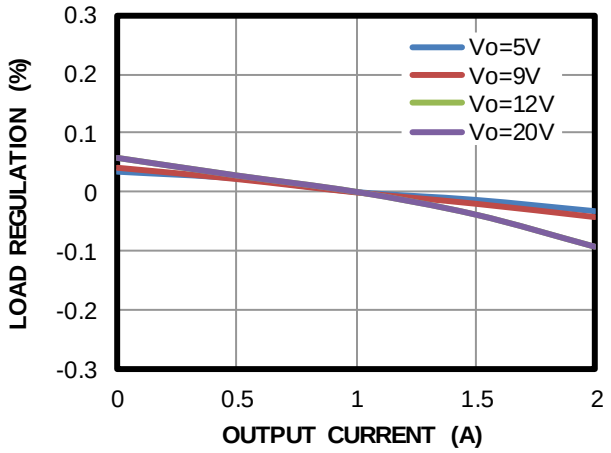
7) All min/max parameters are tested at T_J = 25°C. Limits over temperature are guaranteed by design, characterization, and correlation.
8) Guaranteed by engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

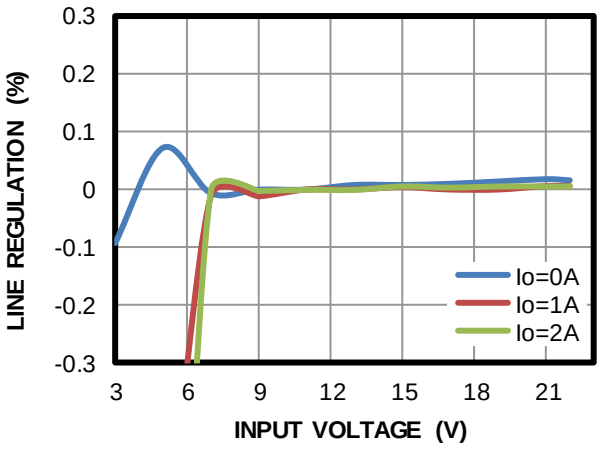
Load Regulation vs. Output Current

V_{IN} = 12V, V_{OUT} = 5V/9V/12V/20V,
I_{OUT} = 0A to 2A, no line drop compensation



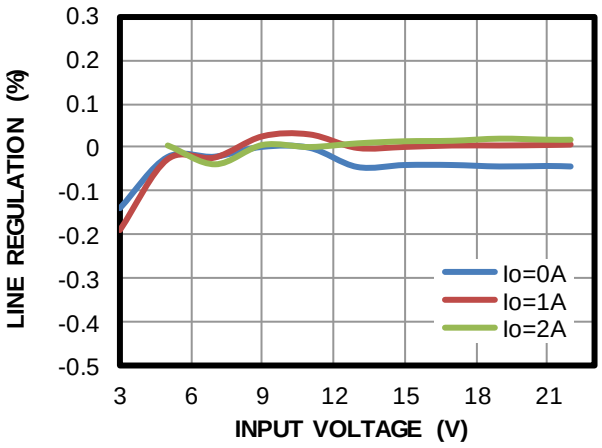
Line Regulation vs. Input Voltage

V_{IN} = 3V to 22V, V_{OUT} = 5V, I_{OUT} = 0A to 2A



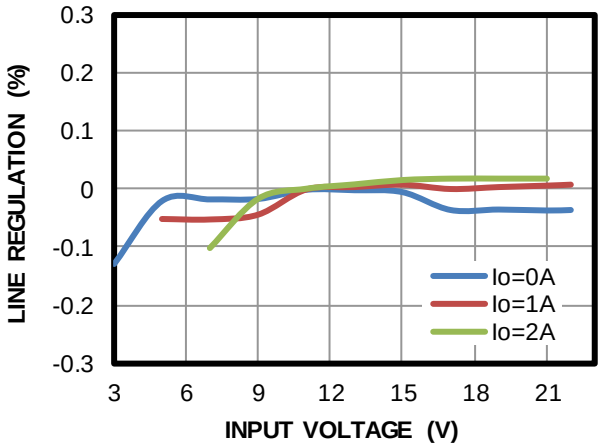
Line Regulation vs. Input Voltage

V_{IN} = 3V to 22V, V_{OUT} = 9V, I_{OUT} = 0A to 2A



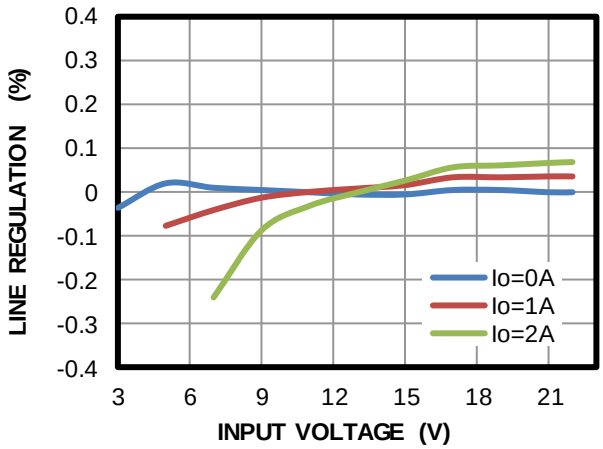
Line Regulation vs. Input Voltage

V_{IN} = 3V to 22V, V_{OUT} = 12V, I_{OUT} = 0A to 2A



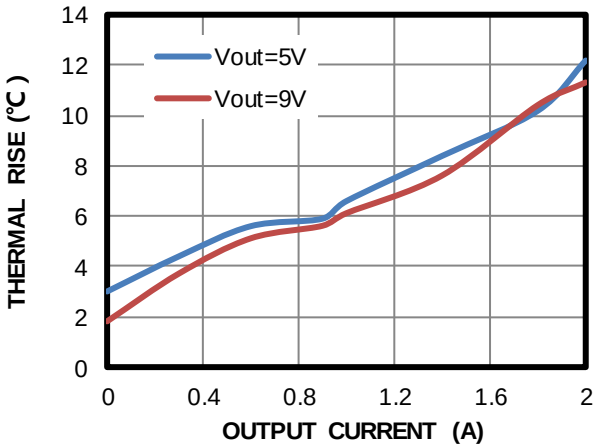
Line Regulation vs. Input Voltage

V_{IN} = 3V to 22V, V_{OUT} = 20V, I_{OUT} = 0A to 2A



Thermal Rising

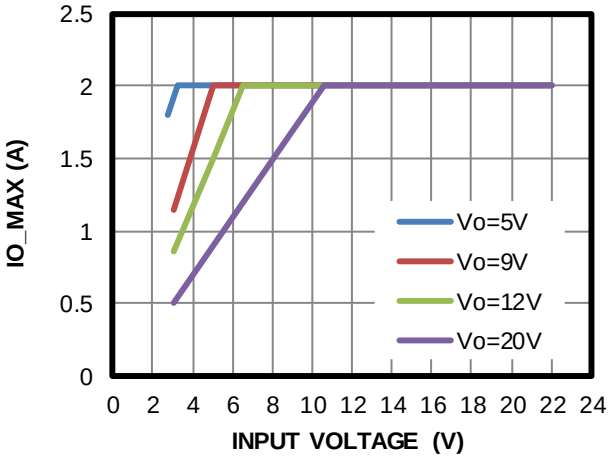
V_{IN} = 12V, I_{OUT} = 0A to 2A



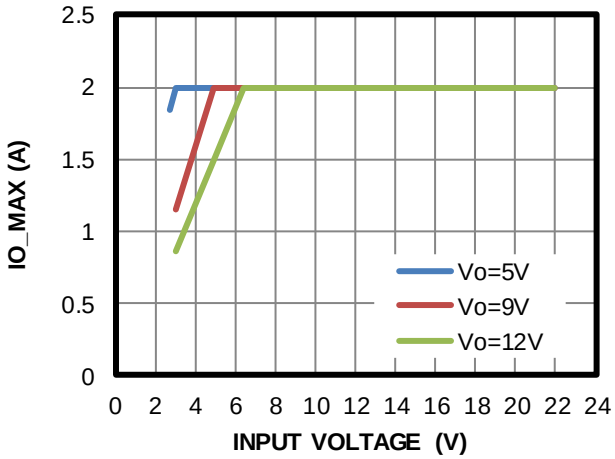
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

Recommended Maximum I_{OUT} vs. V_{IN} and V_{OUT} with 120µF Low-ESR C_{OUT} Capacitor

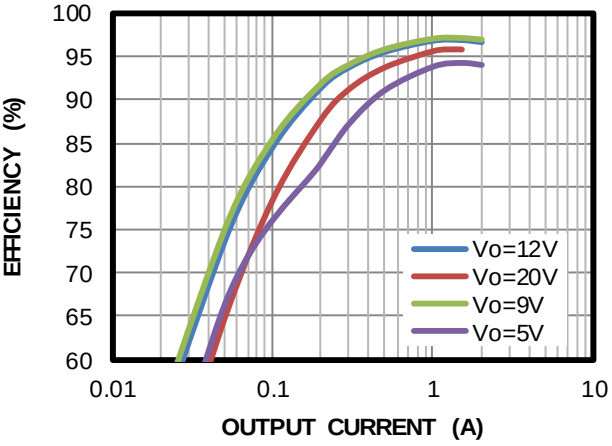


Recommended V_{IN}, V_{OUT}, I_{OUT} Operation Range with 22µFx5 Ceramic C_{OUT} Capacitor



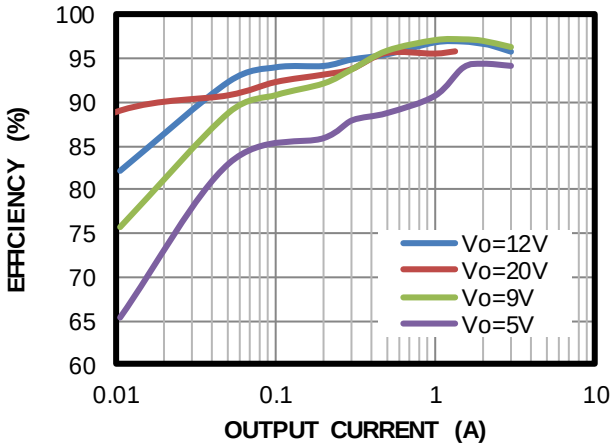
Efficiency

V_{IN} = 12V, V_{OUT} = 5V to 20V, L = 4.7µH,
R_{DC} = 19.5mΩ, forced PWM mode

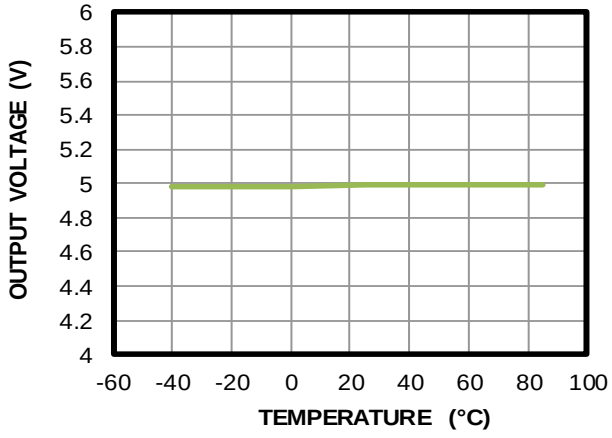


Efficiency

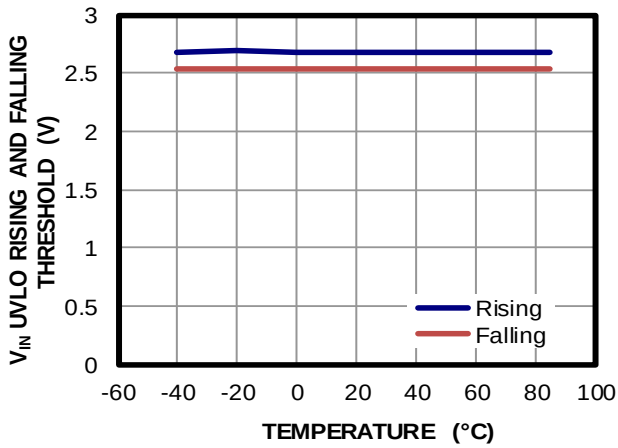
V_{IN} = 12V, V_{OUT} = 5V to 20V, L = 4.7µH,
R_{DC} = 19.5mΩ, PFM mode



Output Voltage vs. Temperature



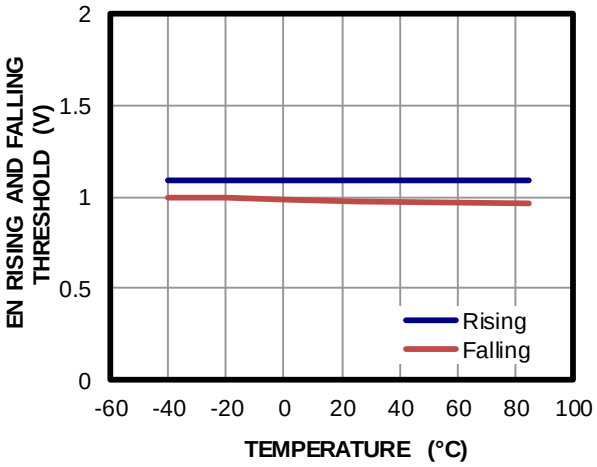
V_{IN} UVLO Rising and Falling Threshold vs. Temperature



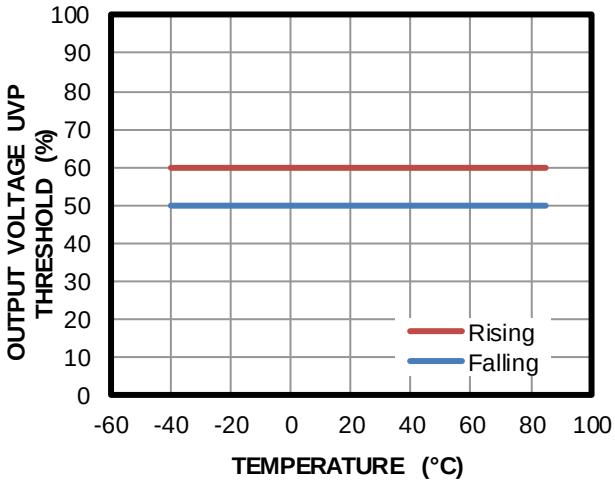
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

EN Rising and Falling Threshold vs. Temperature



Output Voltage UVP Threshold vs. Temperature

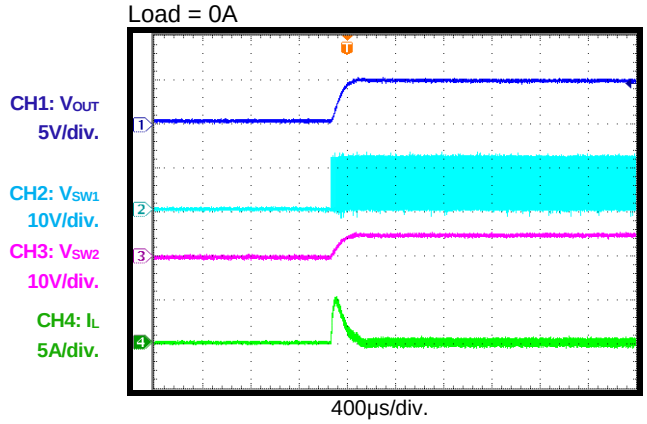


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, test waveform is based on Figure 13, unless otherwise noted.

EN Bit Enable through I^2C Command

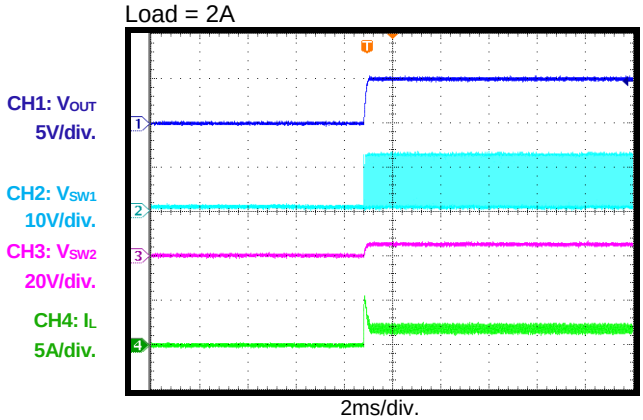
Load = 0A



400µs/div.

EN Bit Enable through I^2C Command

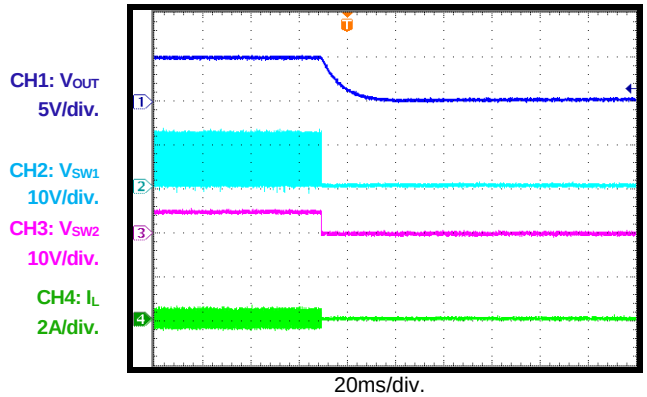
Load = 2A



2ms/div.

EN Bit Disable through I^2C Command

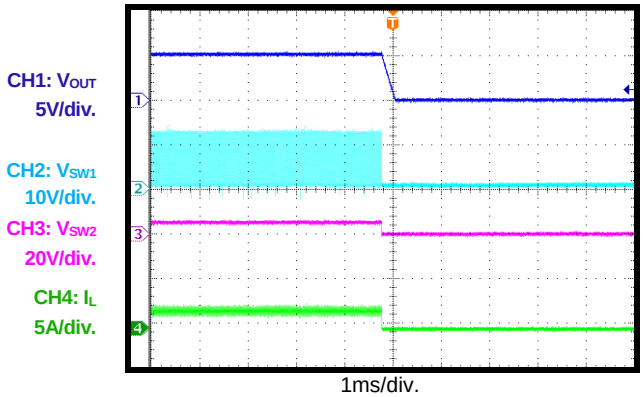
Load = 0A



20ms/div.

EN Bit Disable through I^2C Command

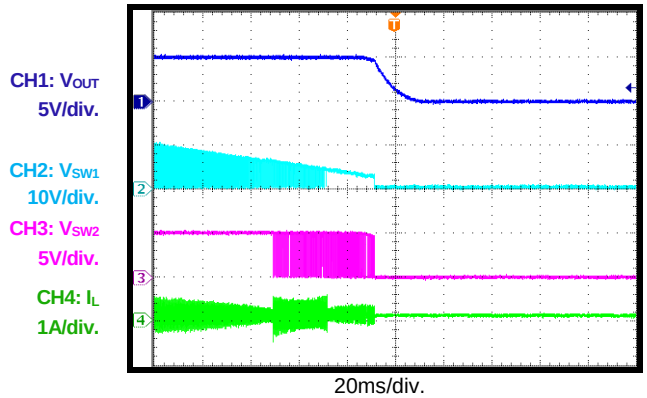
Load = 2A



1ms/div.

V_{IN} Power Off

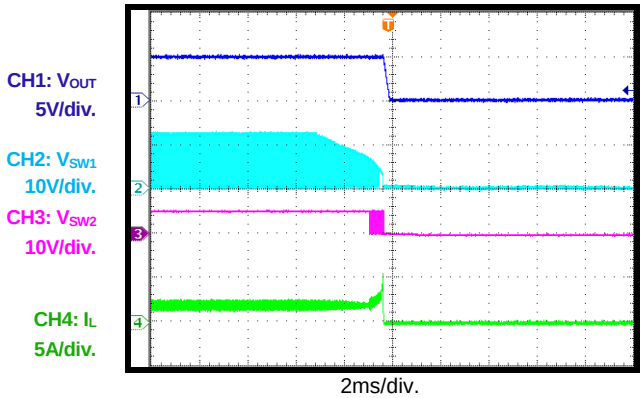
Load = 0A



20ms/div.

V_{IN} Power Off

Load = 2A

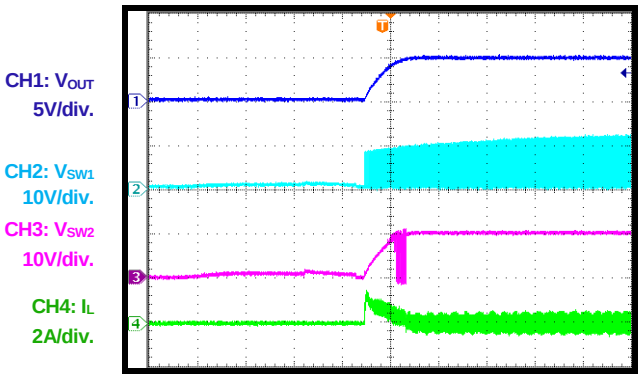


2ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

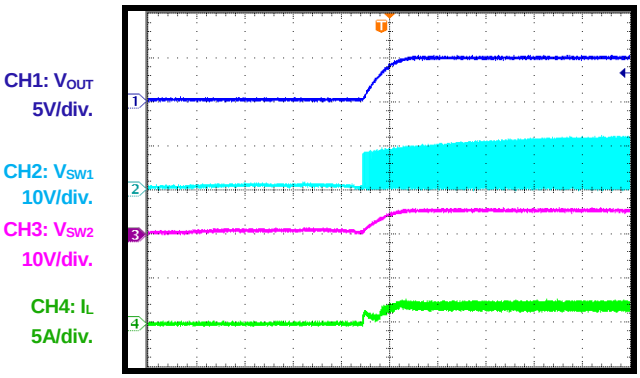
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, test waveform is based on Figure 13, unless otherwise noted.

V_{IN} Start-Up
Load = 10mA



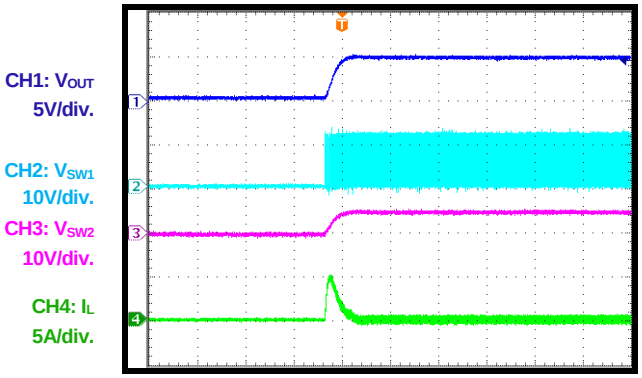
1ms/div.

V_{IN} Start-Up
Load = 2A



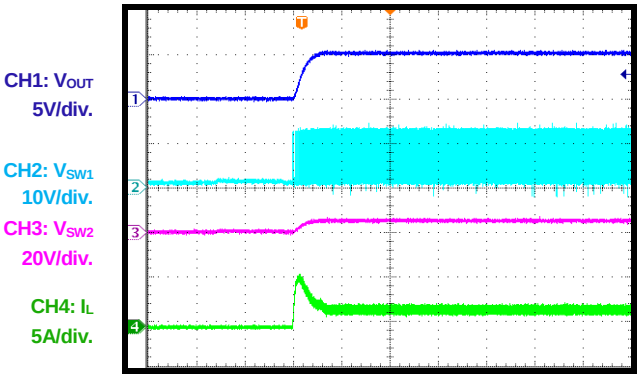
1ms/div.

EN Pin Enable
Load = 0A



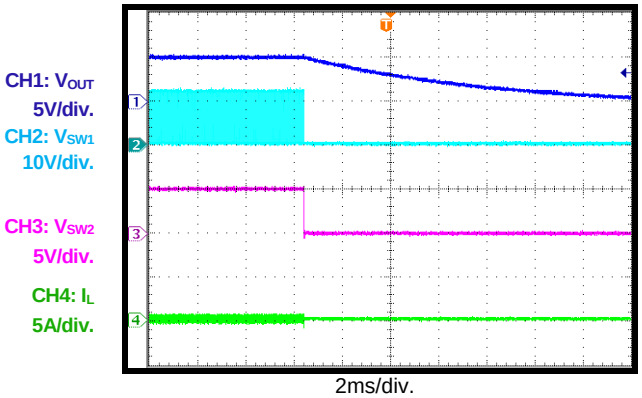
400µs/div.

EN Pin Enable
Load = 2A



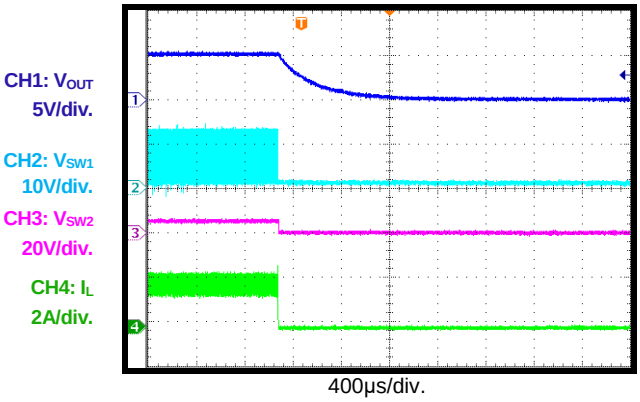
400µs/div.

EN Pin Disable
Load = 0A



2ms/div.

EN Pin Disable
Load = 2A

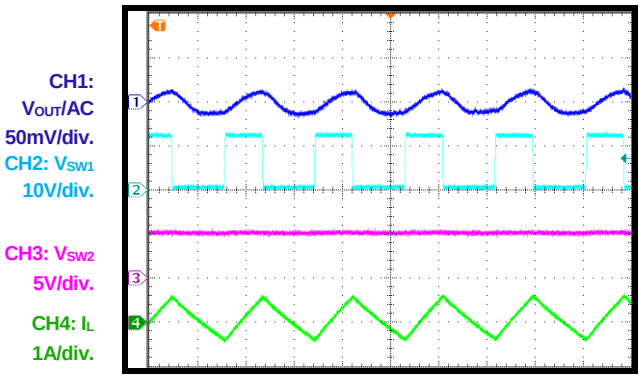


400µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

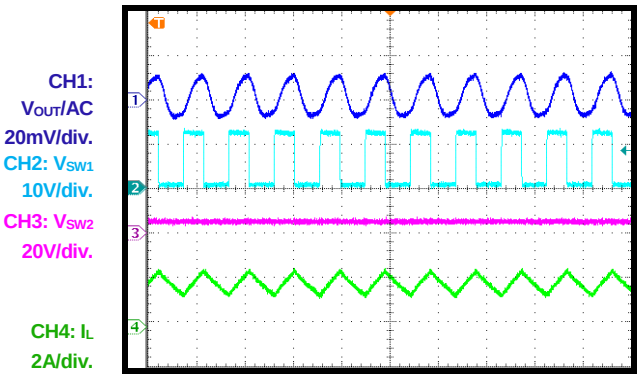
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, test waveform is based on Figure 13, unless otherwise noted.

Steady State
V_{OUT} = 5V, load = 0A



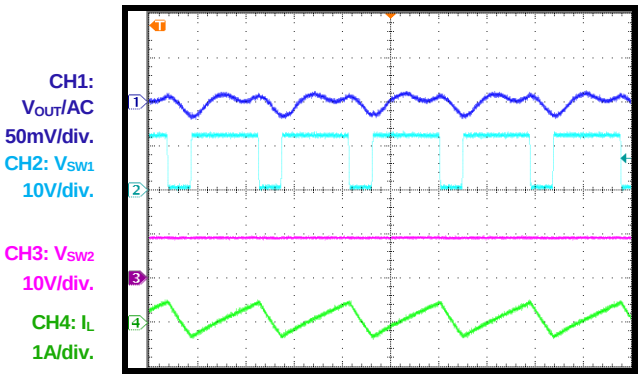
1µs/div.

Steady State
V_{OUT} = 5V, load = 2A



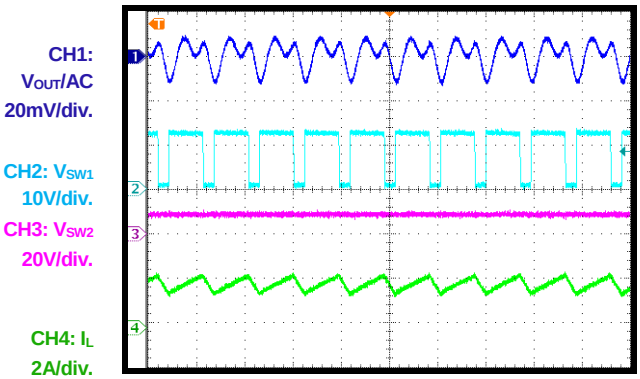
2µs/div.

Steady State
V_{OUT} = 9V, load = 0A



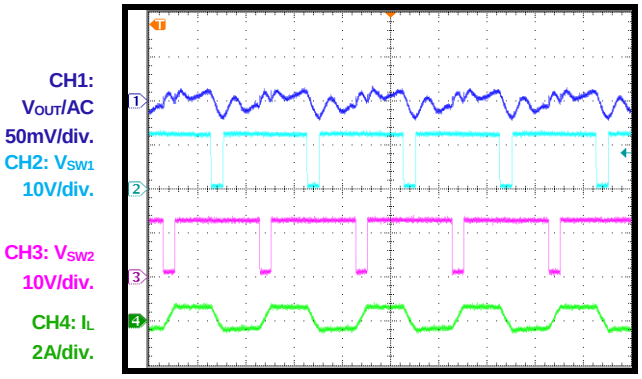
1µs/div.

Steady State
V_{OUT} = 9V, load = 2A



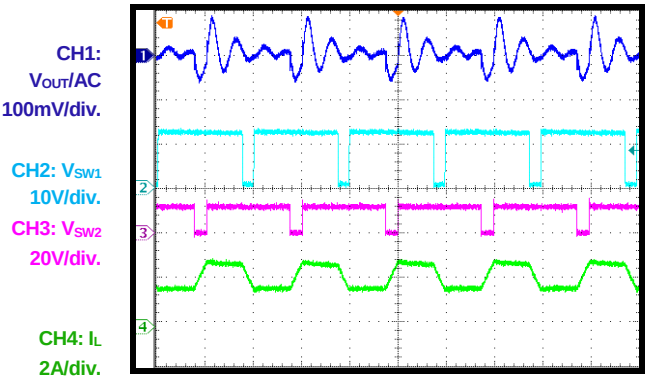
2µs/div.

Steady State
V_{OUT} = 12V, load = 0A



2µs/div.

Steady State
V_{OUT} = 12V, load = 2A



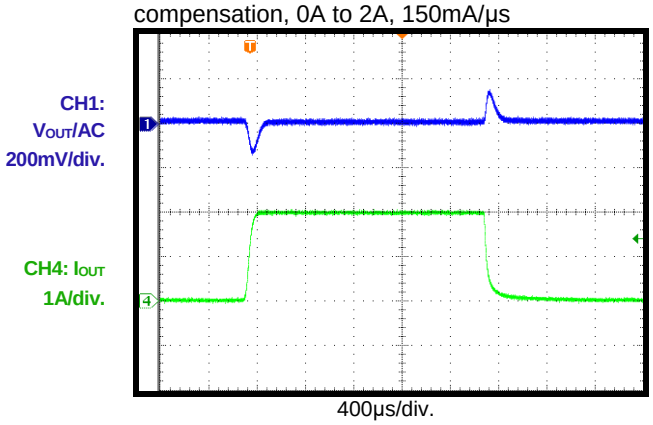
2µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, test waveform is based on Figure 13, unless otherwise noted.

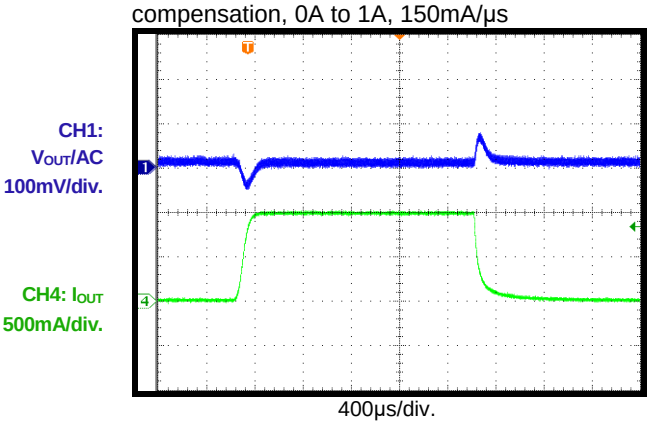
Load Transient

V_{IN} = 12V, V_{OUT} = 5V, no line drop compensation, 0A to 2A, 150mA/µs



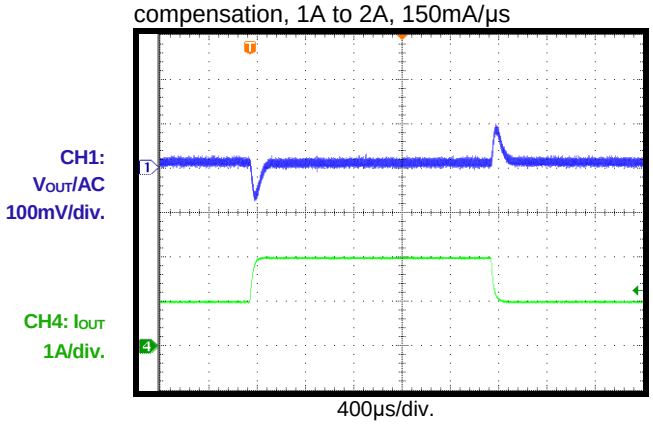
Load Transient

V_{IN} = 12V, V_{OUT} = 5V, no line drop compensation, 0A to 1A, 150mA/µs



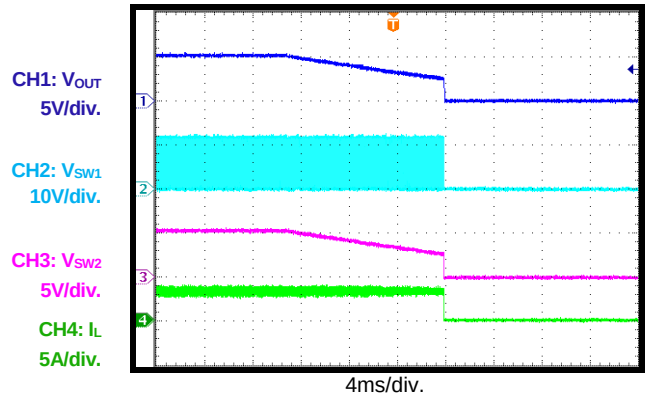
Load Transient

V_{IN} = 12V, V_{OUT} = 5V, no line drop compensation, 1A to 2A, 150mA/µs



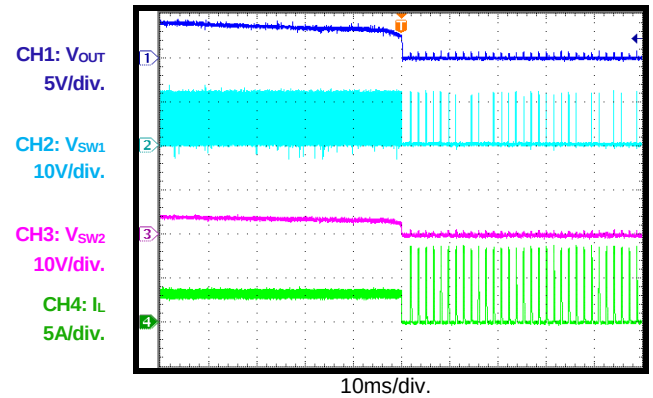
OCP Entry

V_{IN} = 12V, V_{OUT} = 5V, latch-off mode



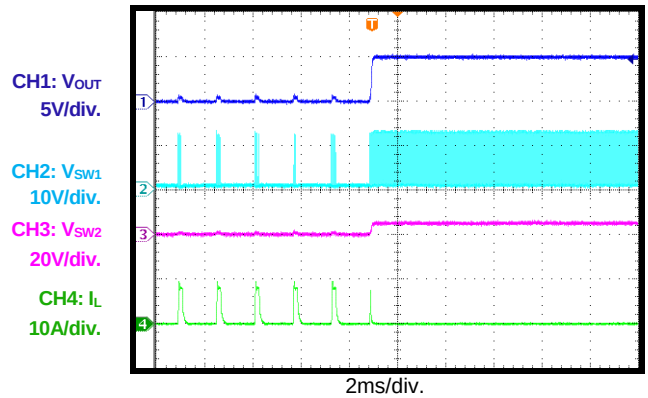
OCP Entry

V_{IN} = 12V, V_{OUT} = 5V, hiccup mode



OCP Recovery

V_{IN} = 12V, V_{OUT} = 5V, hiccup mode

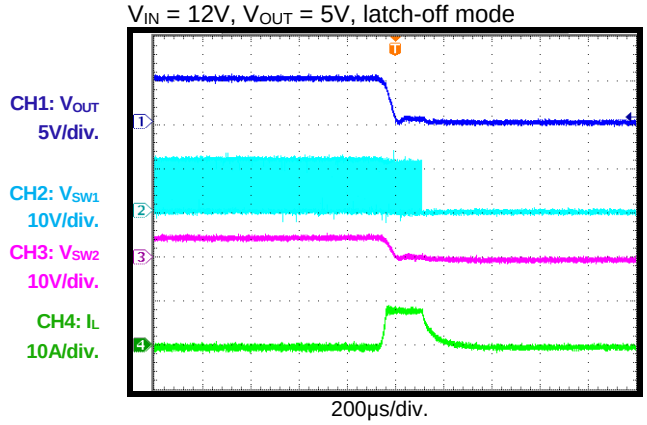


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, test waveform is based on Figure 13, unless otherwise noted.

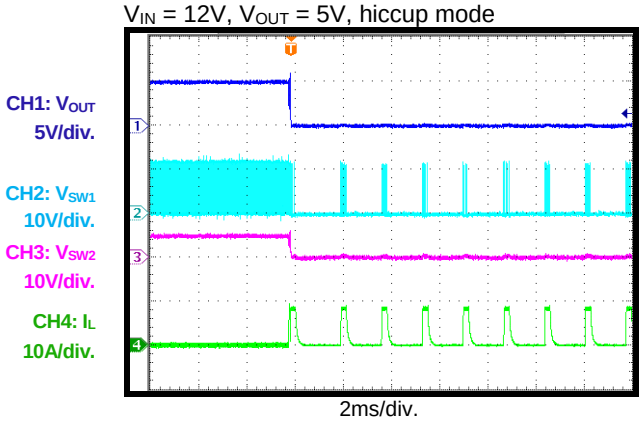
SCP Entry

V_{IN} = 12V, V_{OUT} = 5V, latch-off mode



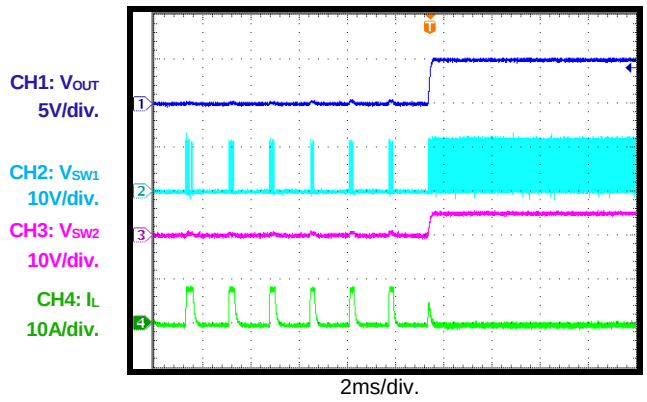
SCP Entry

V_{IN} = 12V, V_{OUT} = 5V, hiccup mode



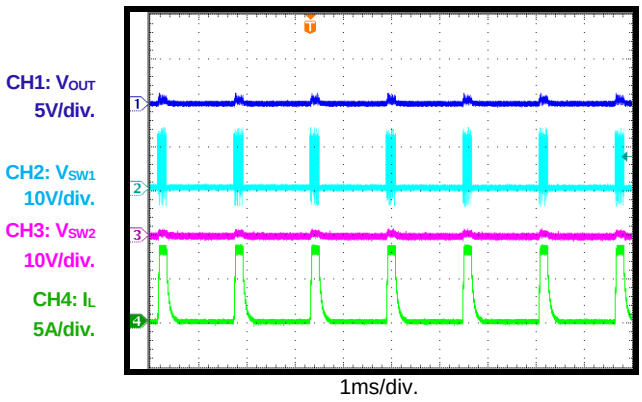
SCP Recovery

V_{IN} = 12V, V_{OUT} = 5V, hiccup mode

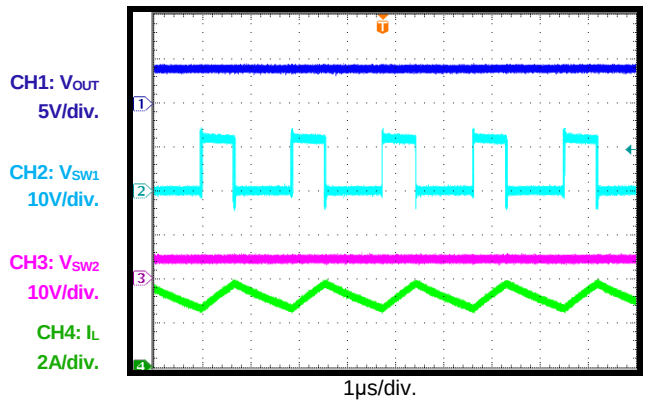


SCP Steady

V_{IN} = 12V, V_{OUT} = 5V, hiccup mode

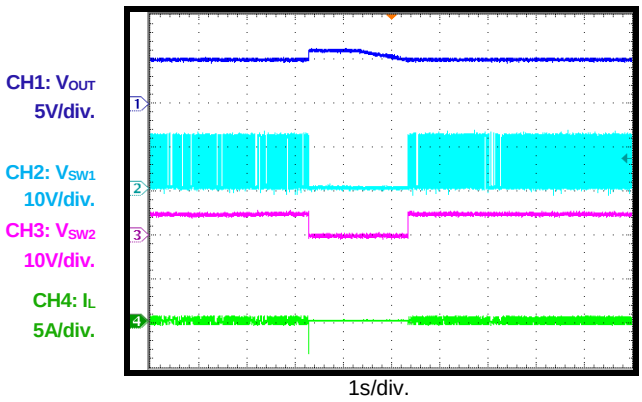


CC Current Limit Steady State



OVP

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, hiccup mode

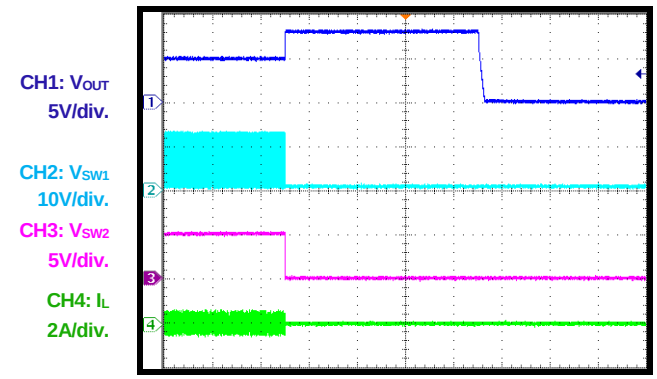


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, test waveform is based on Figure 13, unless otherwise noted.

OVP

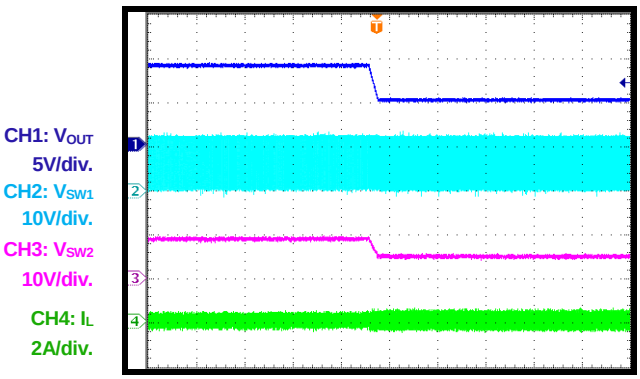
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, latch-off mode



1s/div.

I^2C VID

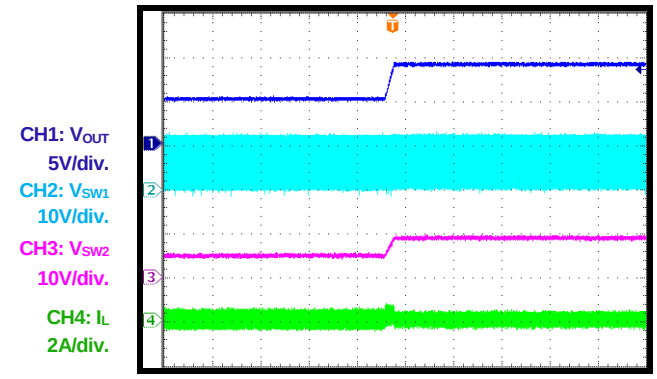
V_{IN} = 12V, V_{OUT} = 9V to 5V, I_{OUT} = 0A



20ms/div.

I^2C VID

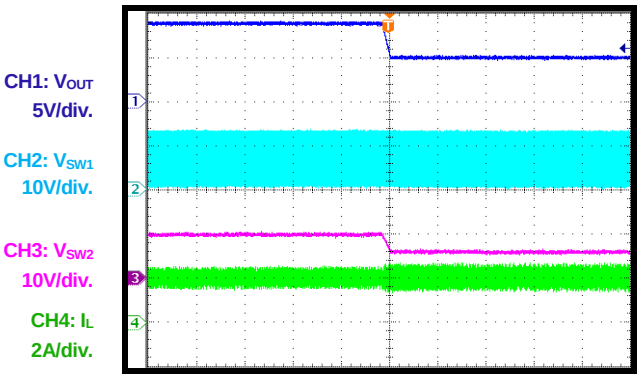
V_{IN} = 12V, V_{OUT} = 5V to 9V, I_{OUT} = 0A



20ms/div.

I^2C VID

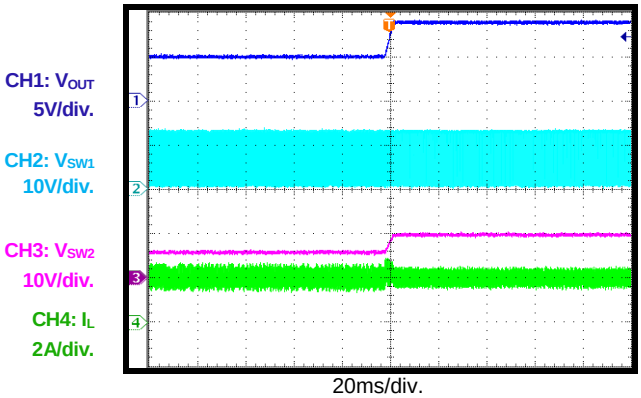
V_{IN} = 12V, V_{OUT} = 9V to 5V, I_{OUT} = 2A



20ms/div.

I^2C VID

V_{IN} = 12V, V_{OUT} = 5V to 9V, I_{OUT} = 2A



20ms/div.

FUNCTIONAL BLOCK DIAGRAM

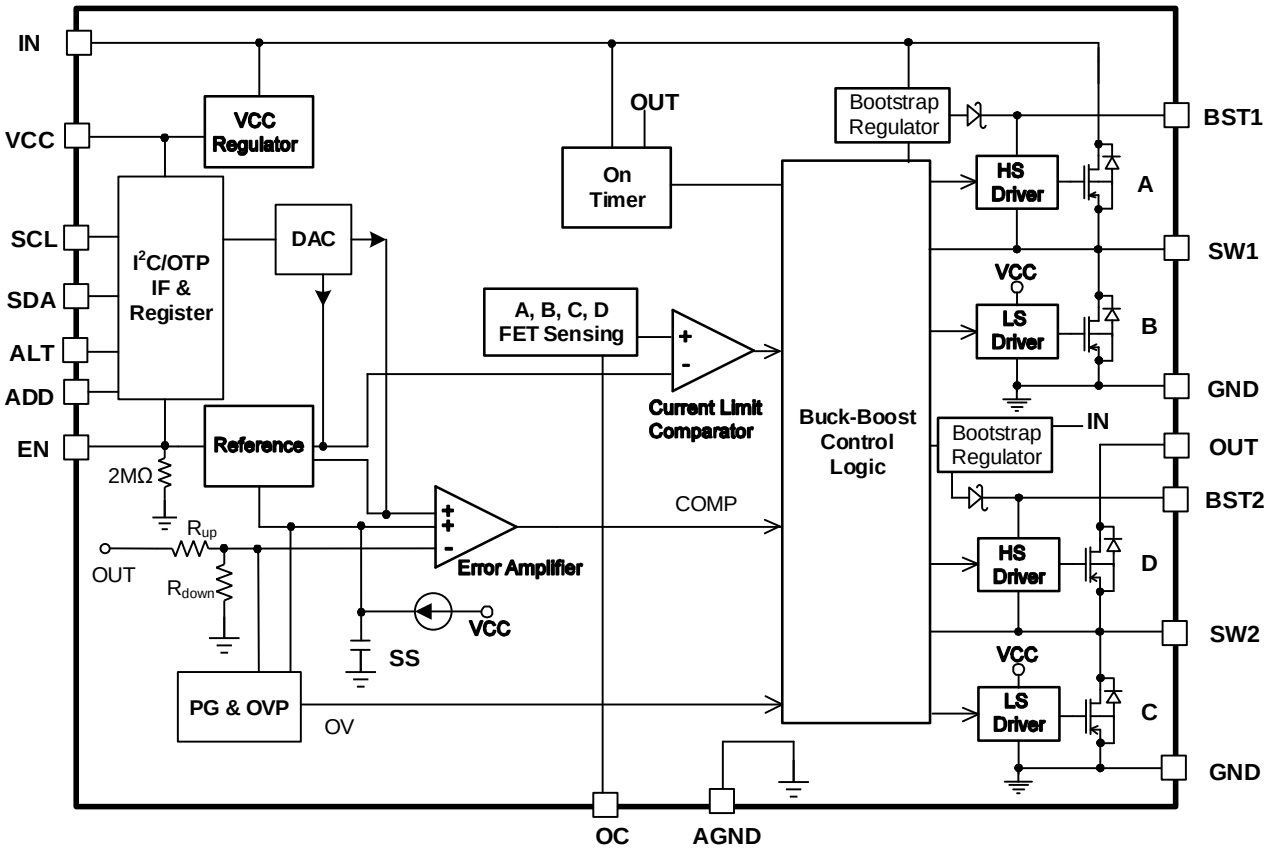


Figure 2: Functional Block Diagram

OPERATION

The MP8862 is a 4-switch, integrated buck-boost converter that works in constant-on-time (COT) mode with fixed frequency, which provides fast transient response for buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency over the full input range and smooth transient between different modes.

Buck-Boost Operation

The MP8862 can regulate the output to be above, equal to, or below the input voltage. Figure 3 shows that the 1-inductor, 4-switch power structure can operate in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 4).

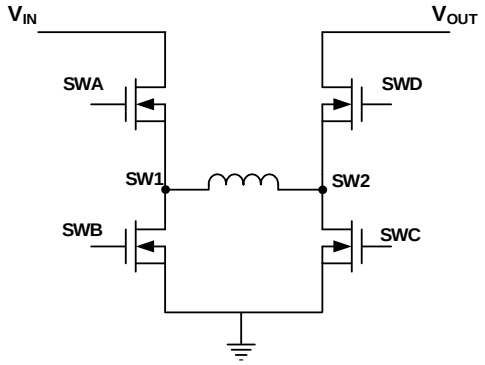


Figure 3: Buck-Boost Topology

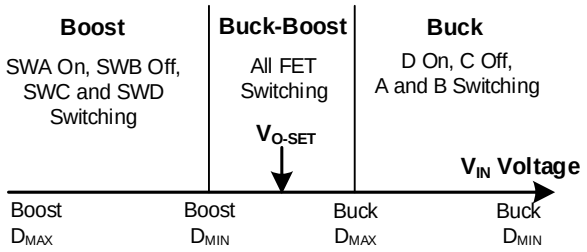


Figure 4: Buck-Boost Operation Range

Buck Mode (V_{IN} > V_{OUT})

When the input voltage is significantly higher than the output voltage, the MP8862 works in buck mode. In buck mode, SWA and SWB switch for buck regulation. SWC is off, and SWD remains on to conduct the inductor current.

SWA works with COT control logic, and SWB turns on as a complement to SWA. In each cycle, SWB turns on to conduct the inductor current. When the inductor current drops to the COMP voltage (V_{COMP}), SWB turns off, and SWA turns on. SWA turns on for a fixed on-time period before turning off. Then SWB turns on again, and the operation repeats. The COMP signal is the error amplifier (EA) output from the V_{OUT} feedback and internal FB reference voltage (see Figure 5).

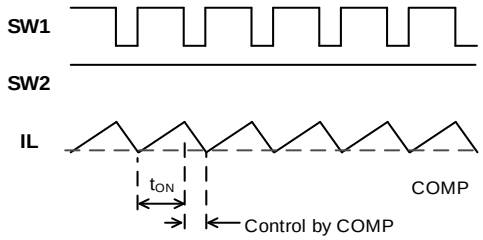


Figure 5: Buck Waveform

Boost Mode (V_{IN} < V_{OUT})

When the input voltage is significantly lower than the output voltage, the MP8862 works in boost mode. In boost mode, SWC and SWD switch for boost regulation. SWB is off, and SWA remains on to conduct the inductor current.

SWC remains off with COT control in each period, while SWD turns on as a complement to SWC to boost the inductor current to the output. In each cycle, SWC turns on to conduct the inductor current. When the inductor current rises and reaches V_{COMP}, SWC turns off and SWD turns on. SWC turns off with a fixed off-time before turning on again. During this period, SWD turns on for the current freewheel (see Figure 6).

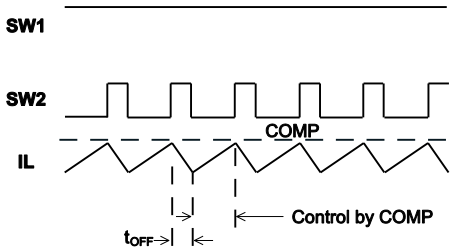


Figure 6: Boost Waveform

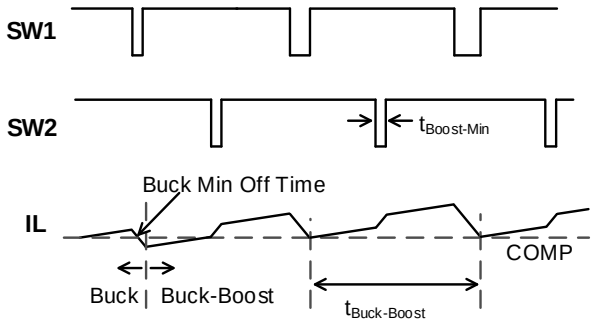
Buck-Boost Mode (V_{IN} ≈ V_{OUT})

When V_{IN} is close to V_{OUT}, the converter may be unable to provide enough energy to operate in buck mode due to SWA's minimum off time, or the converter may supply too much power to

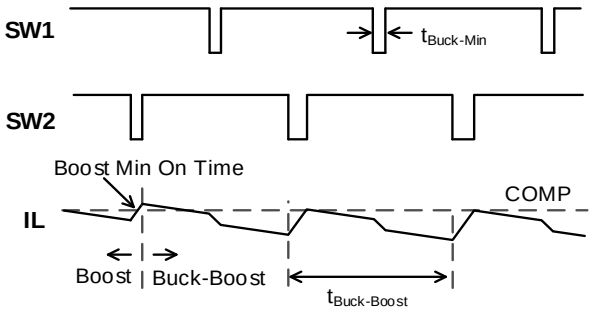
V_{OUT} in boost mode due to SWC's minimum on time. The MP8862 uses buck-boost control to regulate the output in these conditions.

In buck mode, if V_{IN} falls and the SWA off period is close to the buck minimum off time, buck-boost mode is engaged. When the next cycle starts after the SWA and SWD on period (buck high-side MOSFET (HS-FET) on period), boost starts with SWA and SWC on (boost low-side MOSFET (LS-FET) on). SWA and SWD turn on again for the rest of the boost period (boost HS-FET on). After the boost period elapses, the buck period starts, and SWB and SWD remain on until the inductor current drops to V_{COMP}. Then SWA and SWD turn on until the next boost period begins. Buck and boost switching work with a one-interval period. This is called buck-boost mode.

In boost mode, if V_{IN} rises and the SWC on period is close to the boost minimum on time, buck-boost mode is engaged. After the boost constant-off-time period (SWA and SWD on), SWB and SWD remain on until the inductor current signal drops to V_{COMP}, just like a buck off period control. After the inductor current signal triggers V_{COMP}, SWA and SWD turn on for the buck on time, which is followed by a boost switching (SWA and SWC on). Buck and boost switching work with a one-interval period. Figure 7 shows the buck-boost waveform for both $V_{IN} > V_{OUT}$ and $V_{IN} < V_{OUT}$.



Buck to Buck-Boost Transient



Boost to Buck-Boost Transient

Figure 7: Buck-Boost Waveform

In buck-boost mode, if V_{IN} exceeds 130% of V_{OUT}, the MP8862 switches from buck-boost mode to buck mode. If V_{IN} is below 20% of V_{IN}, it switches from buck-boost mode to boost mode.

Working Mode Selection

The MP8862 works with a fixed frequency in heavy-load condition. When the load current decreases, the MP8862 can work in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

FCCM (or Forced PWM)

In FCCM condition, the buck on time and boost off time are determined by the internal circuit to achieve a fixed frequency based on the V_{IN}/V_{OUT} ratio. When the load decreases, the average input current drops, and the inductor current may go negative from V_{OUT} to V_{IN} during the off time (SWD on). This forces the inductor current to work in continuous mode with a fixed frequency, producing a lower V_{OUT} ripple than in PSM mode.

PSM (Auto PFM/PWM Mode)

In PSM condition, once the inductor current drops to 0A, SWD turns off to prevent the current from flowing from V_{OUT} to V_{IN}, forcing the inductor current to work in discontinuous conduction mode (DCM). Simultaneously, the internal off-time clock stretches once the MP8862 enters DCM mode. The frequency drops when the inductor current conduction period decreases, helping to save power loss and reduce the V_{OUT} ripple.

If V_{COMP} drops to the PSM threshold, even if the IC stretches the frequency, the MP8862 stops switching to decrease switching power loss.

The MP8862 recovers switching once V_{COMP} rises above the PSM threshold. The switching pulse skips based on V_{COMP} in very light-load condition. PSM has a much higher efficiency than FCCM mode in light load, but the V_{OUT} ripple may be higher due to the group switching pulse.

Internal VCC Regulator

The 3.65V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 3.65V, the output of the regulator is in full regulation. If V_{IN} is less than 3.65V, the output decreases with V_{IN}. VCC requires an external 1µF ceramic capacitor for decoupling.

Enable Control (EN)

The MP8862 has an enable control pin (EN). Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.

If EN is pulled down when the output discharge function is enabled, the MP8862 completely shuts down after 55ms. The MP8862's I^2C register value is reset to default only after the MP8862 completely shuts down. If EN is pulled high within 55ms, the I^2C register is not reset, and the MP8862 enables the output with previous register setting.

If the output discharge function is disabled, the MP8862 completely shuts down once EN is pulled down for more than 100µs, and the MP8862 I^2C register is reset after a 100µs delay.

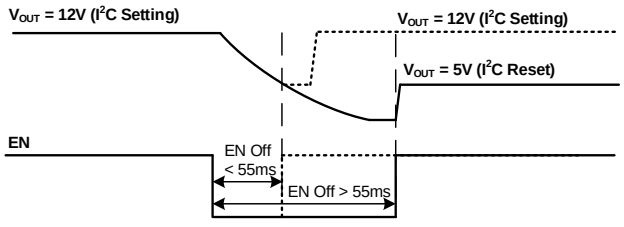


Figure 8: EN On/Off Logic for I^2C Register Reset

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage and enables or disables the entire IC.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 3.6V. When SS is lower than V_{REF}, the error amplifier uses SS as the reference. When SS is higher than V_{REF}, the error amplifier uses V_{REF} as the reference.

If the output of the MP8862 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage (see Figure 9).

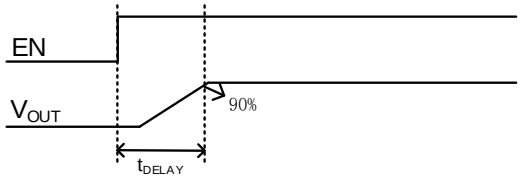


Figure 9: EN On to V_{OUT} > 90% Delay

Output Constant Current Limit (OCP)

The MP8862 has a constant-current limit control loop to limit the output average current. The current information is sensed from switches A, B, C, and D. Then an average algorithm is used to calculate the output current.

When the output current exceeds the current-limit threshold, the output voltage starts to drop. If V_{OUT} drops below the under-voltage (UV) threshold (typically 50% below the reference), the MP8862 enters hiccup mode or latch-off mode, according to the I^2C setting.

In hiccup mode, the MP8862 stops switching and recovers automatically with 12.5% duty cycles. In latch-off mode, the MP8862 stops switching until the IC restarts (V_{IN}, EN, or EN bit toggle).

Over-Voltage Protection (OVP)

The MP8862 monitors a resistor-divided feedback voltage to detect output over-voltage. When the feedback voltage exceeds 160% of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the output-to-ground discharge resistor turns on.

The OUT pin has an absolute OVP function. Once V_{OUT} is higher than the absolute OVP threshold (23V), the MP8862 stops switching and turns on the OUT-to-ground discharge resistor.

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge

The MP8862 has an output discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (input voltage is under UVLO or EN is off), and the discharge path is turned off when V_{OUT} < 50mV or the 50ms maximum timer passes. This function can also be disabled via the I^2C.

Over-Temperature Warning (OTW) and Thermal Shutdown (TSD)

Thermal warning and thermal shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MP8862 sets the OTW bit[D5] to 1. When the temperature falls below its lower threshold (typically 100°C), the OTW bit[D5] is 0.

When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled. This is a non-latch protection.

I^2C INTERFACE

I^2C Serial Interface Description

The I^2C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MP8862 interface is an I^2C slave that supports fast mode (400kHz) and high-speed mode (3.4MHz). The I^2C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled via the I^2C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation.

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and end of an I^2C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10). The master then generates the SCL clocks and transmits the device address and read/write direction bit (R/W) on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by an SDA line. Each byte is followed by an acknowledge bit.

I^2C Update Sequence

The MP8862 requires a start condition, a valid I^2C address, a register address byte, and a data byte for a single data update. The MP8862 acknowledges the receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I^2C address selects the part. It performs an update on the falling edge of the LSB byte. Page 23 shows examples of an I^2C write and read sequence.

I^2C Start-Up Timing

The I^2C function is enabled when V_{IN} > UVLO and EN is active. The function continues to work during OCP, OVP, and thermal shutdown.

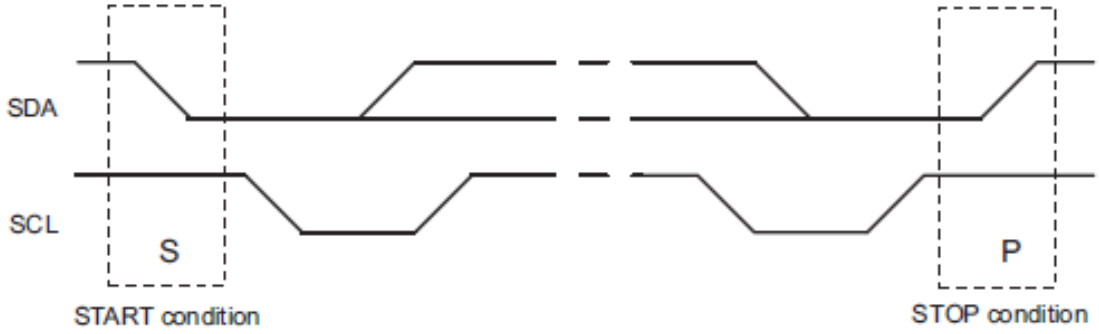
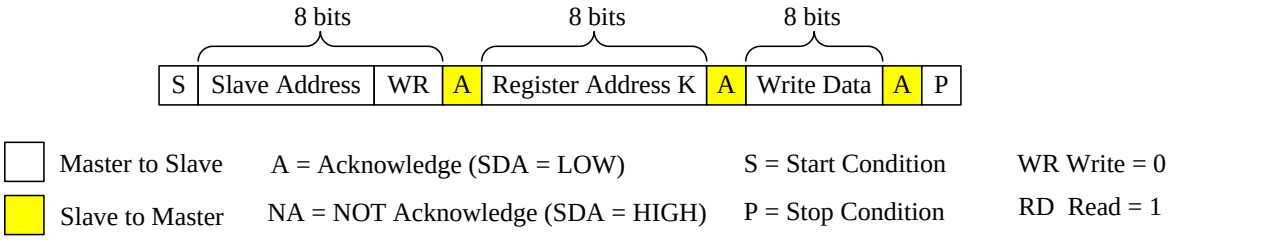
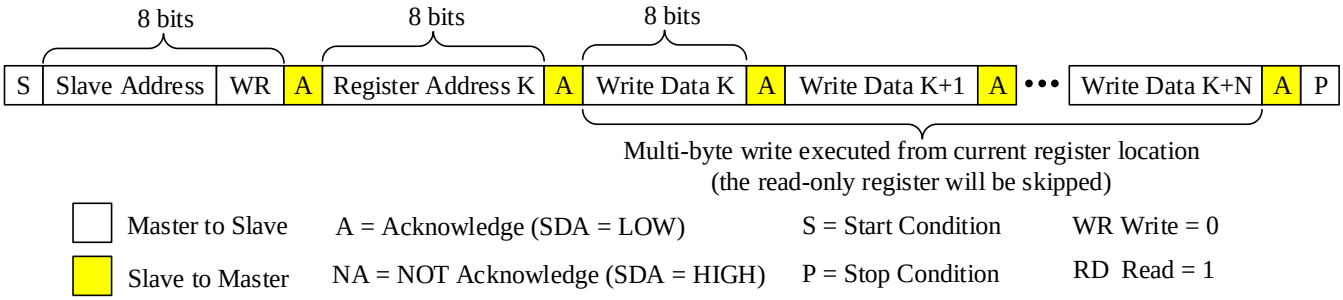


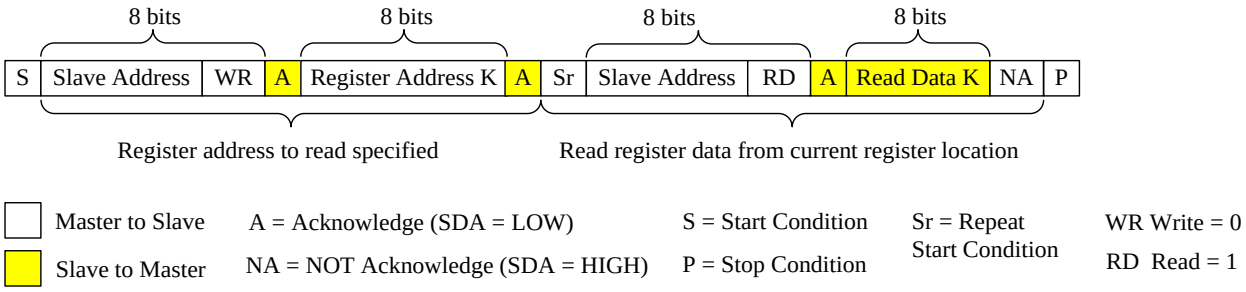
Figure 10: Start and Stop Condition



I^2C Write Example – Write Single Register



I^2C Write Example – Write Multi Register



I^2C Read Example – Read Single Register

I^2C REGISTER MAP

ADD (HEX)	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VOUT_L	R/W	Reserved					VOUT DATA BIT LOW [2:0]*		
01	VOUT_H	R/W	VOUT DATA BIT HIGH [10:3]*							
02	VOUT_GO	R/W	RESERVED						PG_ DELAY_ EN*	GO_ BIT
03	IOUT_LIM	R/W	Reserved	OUTPUT CURRENT LIMIT THRESHOLD (0A-4A/50mA STEP FOR 21.5K OC RESISTOR)*						
04	CTL1	R/W	EN*	HICCUP OCP_OVP*	DISCHG _EN*	MODE*	FREQ		Reserved	
05	CTL2	R/W	LINE DROP COMP*		SS*		Reserved			
06	RESERVED	R	Reserved, ALL “0”						Reserved	
07	RESERVED	R	Reserved							
08	RESERVED	R	Reserved							
09	Status	R	PG	OTP	OTW	CC_CV	Reserved			
0A	Interrupt	W1C	OTEMPP_ ENTER	OT WARNING_ ENTER	OC_ ENTER	OC_ RECOVER	UVP_ FALLING	OTEMP P_EXIT	OT WARNING _EXIT	PG_ RISING
0B	Mask	R/W	RESERVED			OTPMSK*	OTWMSK*	OC_ MSK*	UVP_ MSK*	PG_ MSK*
0C	ID1	R	OTP configure code. "0x00" means standard MP8862, “0x01” means MP8862-0001 part number*							
27	MFR_ID	R	MANUFACTURER ID: b ‘0000 1001’							
28	DEV_ID	R	DEVICE ID: b ‘0101 1000’							
29	IC_REV	R	IC REVISION: b ‘0000 0001’							

Note:

* These items have one-time programmable (OTP) non-volatile memory. The OTP is reloaded to the I^2C register during V_{IN} > UVLO or EN shutdown.

REGISTER DESCRIPTION

I^2C Bus Slave Address

A resistor-divider from VCC to GND can achieve an accurate reference voltage. Connect ADD to this reference voltage to set different I^2C addresses. The internal circuit changes the I^2C address accordingly. Table 1 shows the four voltage thresholds for the four I^2C addresses, and recommended resistor settings.

Table 1: I^2C Address Setting via ADD Voltage

ADD Voltage	ADD Upper Resistor R4 (kΩ)	ADD Lower Resistor R5 (kΩ)	I^2C Address	
			Binary	Hex
<25%V_{CC}	No connection	No connection	1101 001	69H
25% to 50% V_{CC}	499	301	1101 011	6BH
50% to 75% V_{CC}	301	499	1101 101	6DH
>75% V_{CC}	100	No connection	1101 111	6FH

VOUT Setting

The registers VOUT_L and VOUT_H set the output voltage and follow the 11-bit direct format below.

Name	VOUT															
Format	Direct, unsigned binary integer															
Register Name	N/A					VOUT_H D[7:0]								VOUT_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N/A					Data bit high								Data bit low		
Default Value (5V)	N/A					500 integer										

The output voltage can be calculated with Equation (1):

$$V_{OUT}\ (V) = V / 100 \quad (1)$$

Where V is an 11-bit unsigned binary integer of VOUT[10:0], and V ranges from 0 to 2047. The V_{OUT} resolution is 10mV/LSB.

Inside the MP8862, there is a feedback resistor network from OUT to the internal FB reference voltage. The feedback resistor ratio is V_{OUT} / V_{FB} = 12.5. The output voltage change slew rate is fixed at 1mV/μs. Refer to the GO_BIT bit when implementing the output voltage change.

VOUT_GO Register

GO_BIT D[0]

The MP8862 can be controlled when to V_{OUT} begins to change. Set GO_BIT to 1 to start the output change based on the V_{OUT} register. When the V_{OUT} change is complete (internal V_{REF} steps to the goal of V_{REF}), GO_BIT auto-resets to 0. This prevents a false operation of the V_{OUT} scaling.

Write the output voltage (0x00 and 0x01 registers) first, and then write GO_BIT = 1. V_{OUT} changes based on the new register setting. GO_BIT resets to 0 when V_{OUT} reaches a new value. The host can read GO_BIT to determine if the V_{OUT} scaling is finished or not.

The V_{OUT}-to-ground discharge function is enabled when GO_BIT is 1. This can help ramp V_{OUT} from high to low in light-load condition.

When GO_BIT is 0, V_{OUT} will not change. When GO_BIT is 1, V_{OUT} changes based on the V_{OUT} register setting. After V_{OUT} scaling finishes, GO_BIT is reset to 0 automatically.

PG_DELAY_EN D[1]

When PG_DELAY_EN D[1] is 0, there is no delay on PG. When PG_DELAY_EN D[1] is 1, PG experiences a 100μs rising delay. The default value is 0.

IOUT_LIM Register

Set the output current limit threshold.

Name	IOUT_LIM							
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	N/A	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value (3A)	N/A	60 integer						

IOUT_OC can be calculated with Equation (2):

$$IOUT\_OC\ (A) = IOUT\_LIM * 0.05 \quad (2)$$

Where IOUT_LIM is a 7-bit unsigned binary integer of IOUT_LIM D[6:0]. The IOUT_OC resolution is 50mA/LSB (maximum value is 4A or 0x50).

The OC pin-to-ground resistor should be 21.5kΩ when using the above IOUT_LIM register. A 22nF (C6) filter capacitor should be added on OC to keep the CC loop stable. The MP8862 directly supports the I^2C setting IOUT_LIM. If the CC threshold needs to be changed dynamically after the MP8862 has already entered the CC limit operation state, it is recommended to change the CC threshold step-by-step (e.g. 50mA per step) instead of changing the current value directly to the final value.

CTL1 Register

NAME	BITS	DEFAULT	DESCRIPTION
EN	D[7]	1	I^2C-controlled, turns the part on or off. When the external EN pin is low, the converter is off, and the I^2C shuts down. When EN is high, the EN bit takes over. **1: Part is turned on. Default** 0: Part is turned off. I^2C register does not reset
HICCUP OCP_OVP	D[6]	1	Over-current and over-voltage protection mode selection. **1: Hiccup mode** 0: Latch-off mode
DISCHG_EN	D[5]	1	Output discharge enable bit. **1: Output discharge function during EN or V_{IN} shutdown** 0: No discharge output during shutdown
MODE	D[4]	1	Default is PWM mode for light load. 0: Enables auto PFM/PWM mode **1: Sets forced PWM mode**
FREQ	D[3:2]	00	Sets the switching frequency. **00: 500kHz** 01, 10, 11: Reserved

CTL2 Register

NAME	BITS	DEFAULT	DESCRIPTION
LINE DROP COMP	D[7:6]	00	Sets the output voltage compensation vs. the load feature. **00: No compensation** 01: V_{OUT} compensates 100mV @ 2A I_{OUT} 10: V_{OUT} compensates 200mV @ 2A I_{OUT} 11: V_{OUT} compensates 400mV @ 2A I_{OUT} The above compensation amplitude is fixed for any output voltage. Line drop compensation is only enabled for V_{OUT} ≥ 5V.
SS	D[5:4]	11	Sets the output start-up soft-start timer (from 0 to 100%). For 5V output voltage: 00: 300µs 01: 500µs 10: 700µs **11: 900µs** The SS slew rate is constant, but changes for different V_{OUT} values.

Status Register

NAME	BITS	DEFAULT	DESCRIPTION	
PG	D[7]	X	Output power good indication. 0: Output power is not good 1: Output power is good	These status bits indicate instantaneous value.
OTP	D[6]	X	Over-temperature protection indication. 0: Normal state 1: Chip is in over-temperature protection state	
OTW	D[5]	X	Over-temperature warning indication. 0: Normal state 1: Chip is in-over temperature warning state	
CC_CV	D[4]	X	The chip works in constant-current output mode or constant-voltage output mode. 0: CV mode 1: CC mode	

Interrupt Register

NAME	BITS	DESCRIPTION	
OTEMPP_ENTER	D[7]	Over-temperature protection entry indication. When this bit is high, the IC enters thermal shutdown. This bit is not masked, even if OTPMSK = 1. OTPMSK = 1 only masks the interrupt pin's output (ALT).	This bit is latched once triggered. Write 0xFF to this register to reset the interrupt (ALT) pin's state.
OTWARNING_ENTER	D[6]	Die temperature early warning entry bit. When this bit is high, the die temperature is above 120˚C. This bit is not masked, even if OTWMSK = 1. OTWMSK = 1 only masks the interrupt pin's output (ALT).	
OC_ENTER	D[5]	Entry of OC or CC current-limit mode. The OC_MSK bit can enable or disable OC_ENTER and OC_RECOVER alert output.	
OC_RECOVER	D[4]	Recovery from CC current-limit mode. Recovering from a hiccup will not trigger this interrupt signal.	
UVP_FALLING	D[3]	Output voltage is in under-voltage protection.	
OTEMPP_EXIT	D[2]	Over-temperature protection exit. OTPMSK can mask off the ALT of this bit.	
OTWARNING_EXIT	D[1]	Die temperature early warning exit bit. When the die temperature is lower than 100°C, this bit is set to 1. This bit is not masked, even if OTWMSK = 1. OTWMSK = 1 only masks the interrupt pin's output (ALT).	
PG_RISING	D[0]	Output power good rising edge.	

MSK Register

NAME	BITS	DEFAULT	DESCRIPTION
OTPMSK	D[4]	0	SET OTPMSK = 1 to mask off the OTP alert. OTPMSK = 1 only masks the interrupt pin's output (ALT). This is not the interrupt register, but is similar for other mask bits.
OTWMSK	D[3]	0	Masks off the over-temperature warning.
OC_MSK	D[2]	0	Masks off both OC/CC entry and recovery.
UVP_MSK	D[1]	0	Masks off the output UVP interrupt.
PG_MSK	D[0]	0	Masks off the PG indication function on ALT. 1: ALT pin does not indicate a PG event 0: ALT indicates a PG rising event

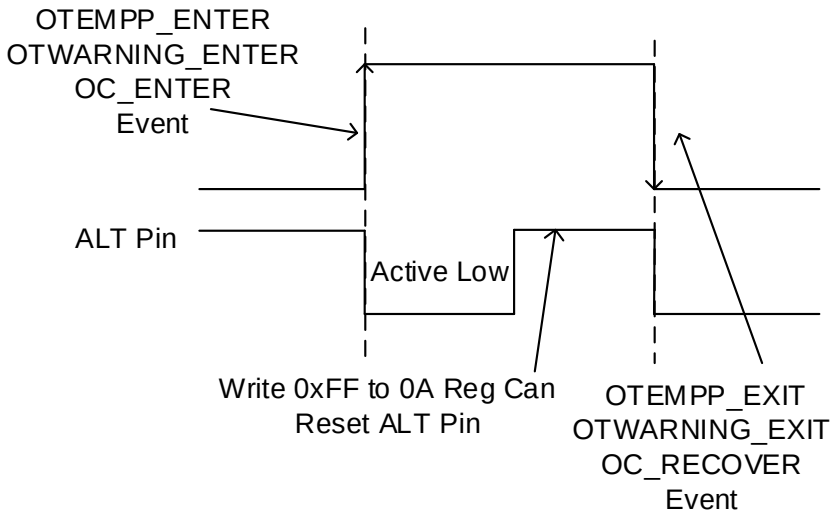


Figure 11: ALT Behavior of OTP, OT Warning, and OC Recovery

APPLICATION INFORMATION

Component Selection

Selecting the Inductor

In a buck-boost topology circuit, the inductor must support buck applications with the maximum input voltage, and boost applications with the minimum input voltage. Two critical inductance values can be determined according to the buck mode and boost mode current ripple using Equation (2) and Equation (3):

$$L_{MIN-BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{REQ} \times \Delta I_L} \quad (2)$$

$$L_{MIN-BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times f_{REQ} \times \Delta I_L} \quad (3)$$

Where f_{REQ} is the switching frequency, and ΔI_L is the peak-to-peak inductor current ripple. As a rule of thumb, the peak-to-peak ripple can be set as 0.5A to 1.5A of the inductor current. The minimum inductor value for the application must be higher than both the Equation (2) and Equation (3) results.

In addition to the inductance value, to avoid saturation, the inductor must support the peak current based on Equation (4) and Equation (5):

$$I_{PEAK-BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times f_{REQ} \times L} \quad (4)$$

$$I_{PEAK-BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times f_{REQ} \times L} \quad (5)$$

Where η is the estimated efficiency of the MP8862.

Input and Output Capacitor Selection

It is recommended to use ceramic capacitors plus an electrolytic capacitor for input and output capacitors, to filter the input and output ripple current and achieve stable operation.

Since the input capacitor absorbs the input switching current, it requires sufficient capacitance. For most applications, a 100µF electrolytic capacitor plus a 22µF ceramic capacitor are sufficient.

The output capacitor stabilizes the DC output voltage. Low-ESR capacitors and a sufficient capacitor value are recommended to limit the output voltage ripple. Considering the ceramic DC voltage derating, if the output voltage is less than 12V, the minimum C_{OUT} should be 22µFx5 ceramic. If the output voltage is greater than 12V, use a 100µF low-ESR (≤80mΩ) aluminum electrolytic or polymer capacitor and two 10µF ceramic capacitors.

The input and output ceramic capacitors must be placed as close as possible to the device.

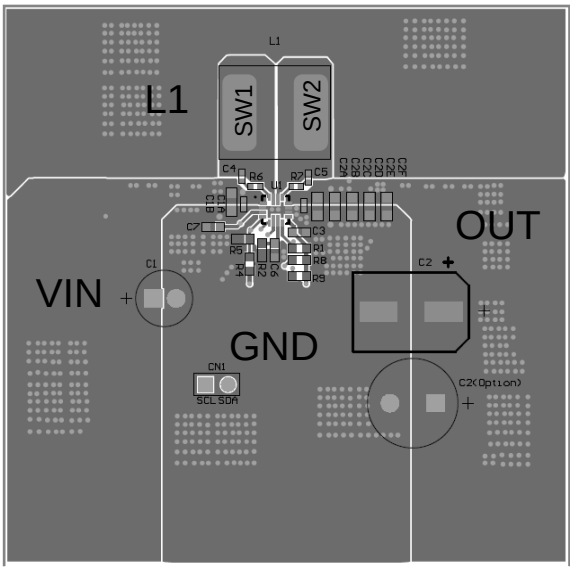
PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 12 and follow the guidelines below:

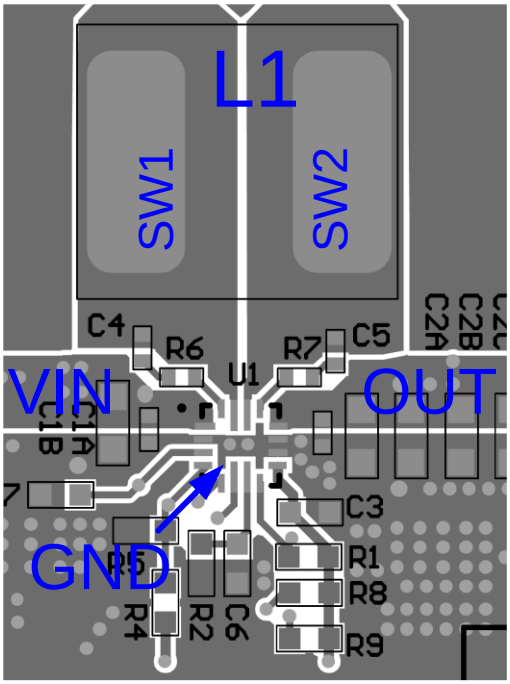
1. Place the ceramic C_{IN} and C_{OUT} capacitors close to the IC's VIN-to-GND and OUT-to-GND pins, respectively.
2. Use a large copper plane for PGND.
3. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. Use short, direct, and wide traces to connect OUT.
6. Add vias under the IC and routing the OUT trace on both PCB layers (highly recommended).
7. Use a large copper plane for SW1 and SW2.
8. Place the VCC decoupling capacitor as close to VCC as possible.

Notes:

9) The recommended layout is based on the Typical Application Circuits on page 31.



Top Layer



Close-Up of Layout

Figure 12: Recommended Layout

TYPICAL APPLICATION CIRCUITS

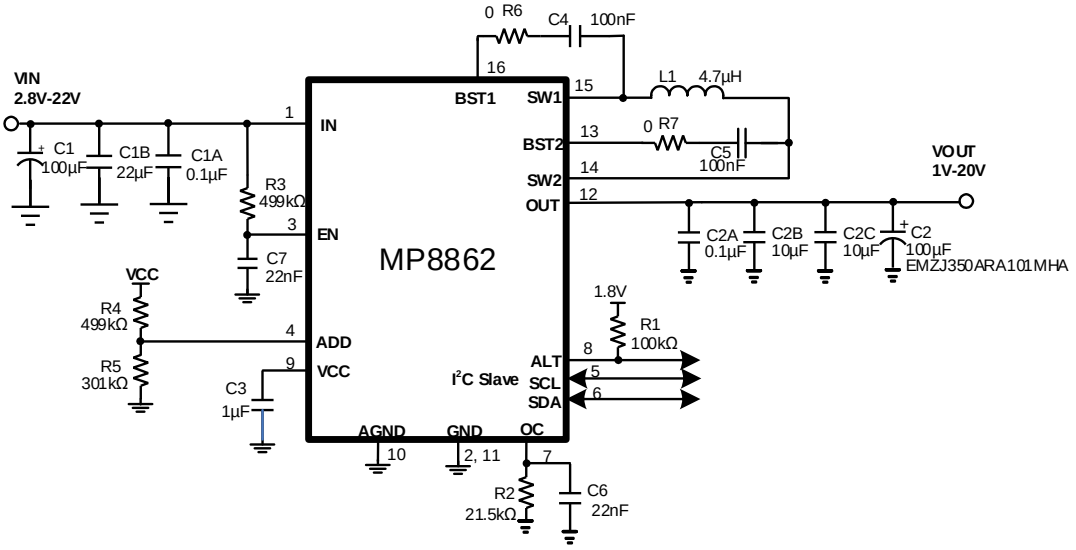


Figure 13: Typical Application Circuit for 1V-20V$_{OUT}$

Note: Refer to the recommended maximum I_{OUT} vs. V_{IN} and V_{OUT} with 120µF low-ESR C_{OUT} capacitor curve on page 9.

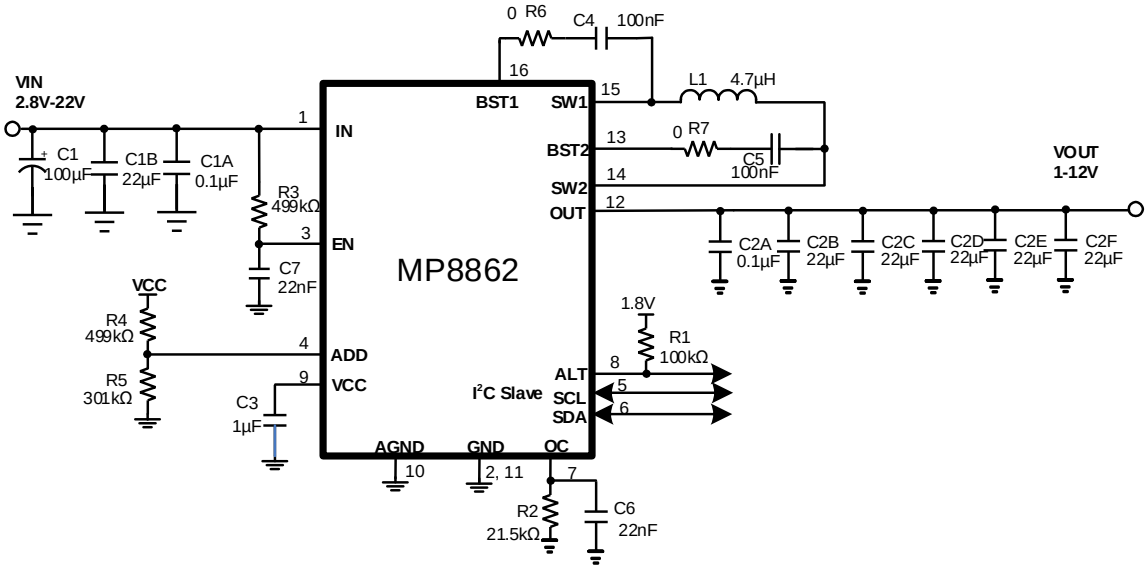
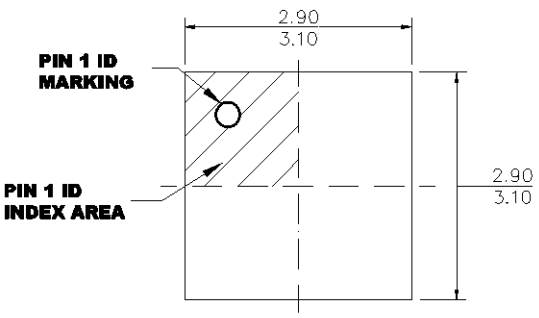


Figure 14: Typical Application Circuit for 1V-12V$_{OUT}$

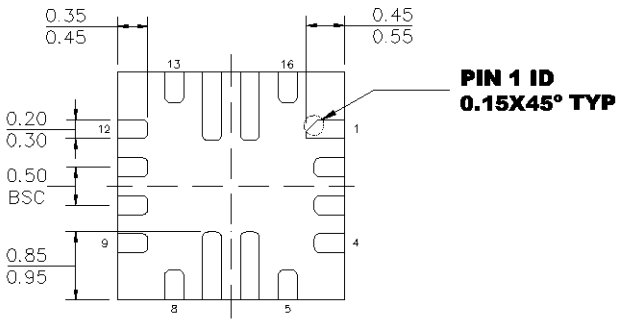
Note: Refer to the recommended maximum I_{OUT} vs. V_{IN} and V_{OUT} with 22µFx5 ceramic C_{OUT} capacitor curve on page 9.

PACKAGE INFORMATION

QFN-16 (3mmx3mm)

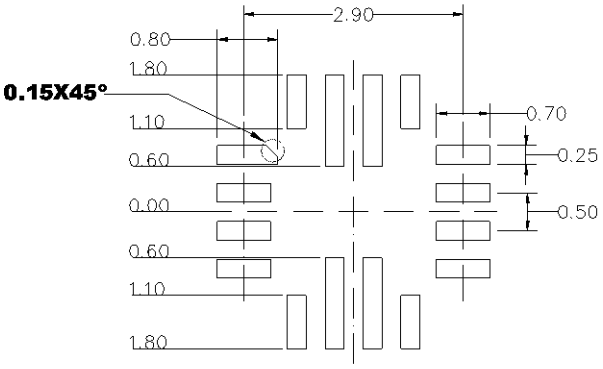


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.