

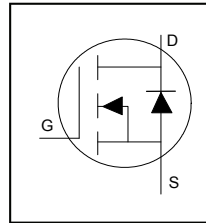
### Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

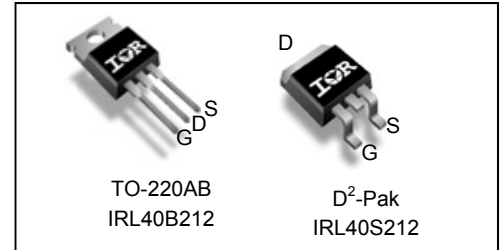
### Benefits

- Optimized for Logic Level Drive
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- RoHS Compliant, Halogen-Free

HEXFET® Power MOSFET



$V_{DSS}$	<b>40V</b>
$R_{DS(on)}$ typ.	<b>1.5mΩ</b>
$R_{DS(on)}$ max	<b>1.9mΩ</b>
$I_D$ (Silicon Limited)	<b>254A</b> ①
$I_D$ (Package Limited)	<b>195A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRL40B212	TO-220	Tube	50	IRL40B212
IRL40S212	D²-Pak	Tape and Reel	800	IRL40S212

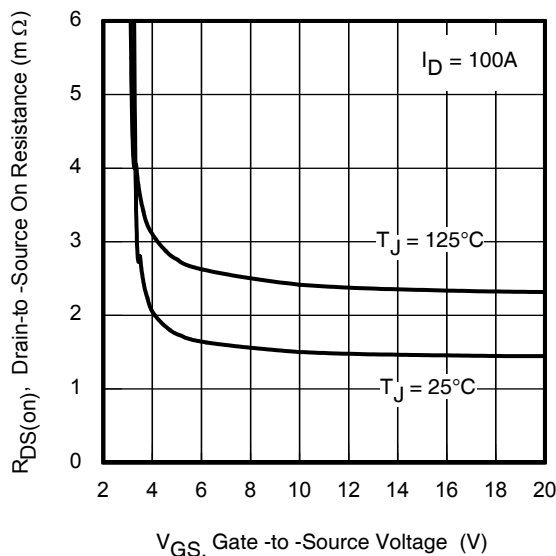


Fig 1. Typical On-Resistance vs. Gate Voltage

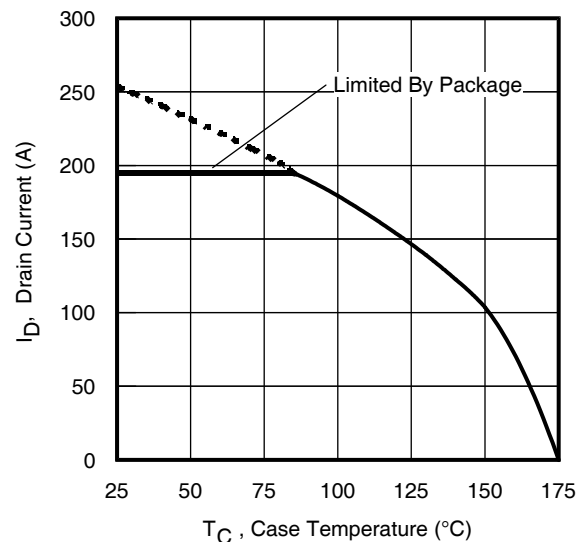


Fig 2. Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	254 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	179 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	195	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	990 *	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	231	W
	Linear Derating Factor	1.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	342	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>④</sup>	790	
$I_{AR}$	Avalanche Current <sup>②</sup>	See Fig 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>②</sup>		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>⑤</sup>	—	0.65	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) <sup>⑥</sup>	—	40	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.03	—	V/°C	Reference to $25^\circ\text{C}, I_D = 2\text{mA}$ <sup>②</sup>
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.5	1.9	mΩ	$V_{GS} = 10\text{V}, I_D = 100\text{A}$ <sup>⑤</sup>
		—	1.9	2.4		$V_{GS} = 4.5\text{V}, I_D = 50\text{A}$ <sup>⑤</sup>
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.4	V	$V_{DS} = V_{GS}, I_D = 150\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	1.6	—	Ω	

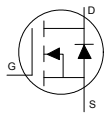
**Notes:**

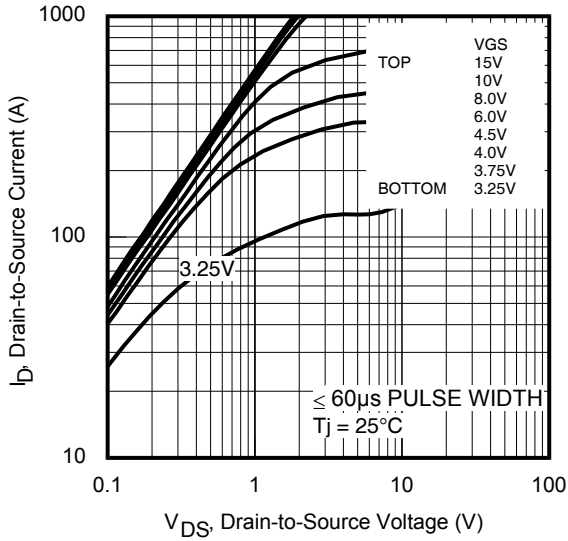
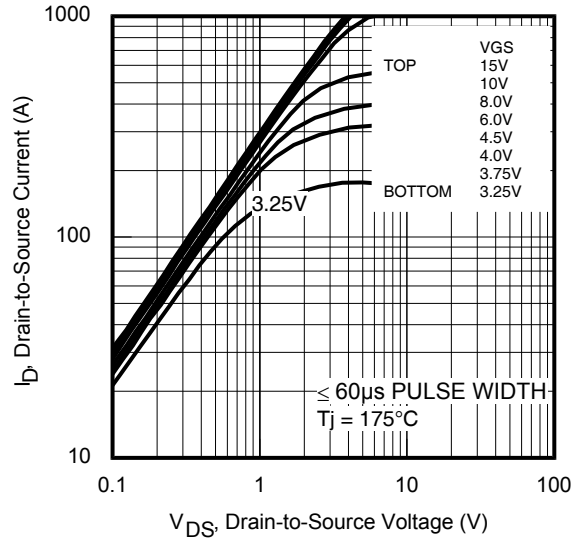
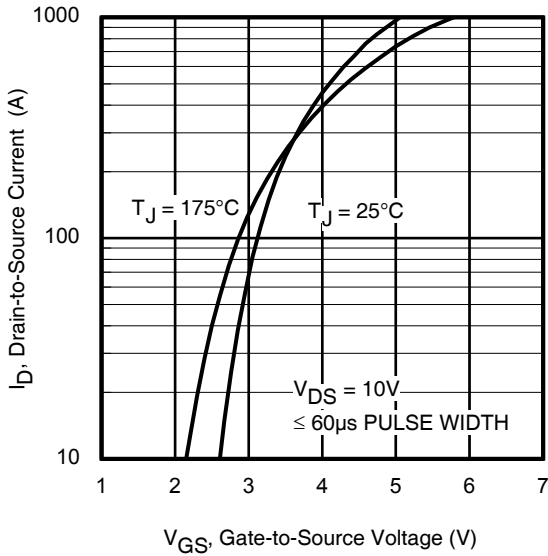
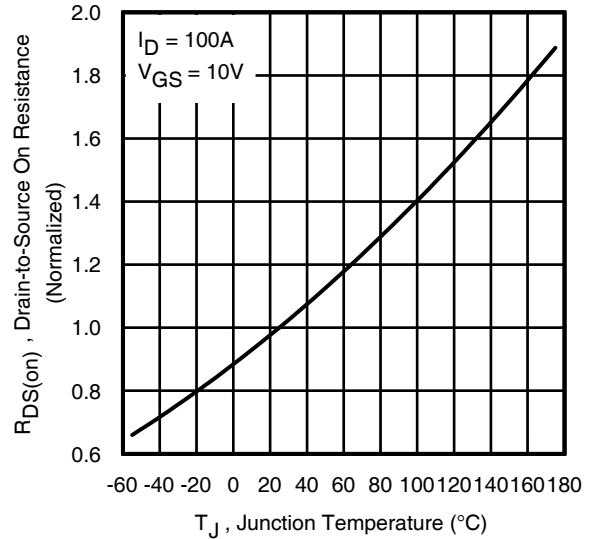
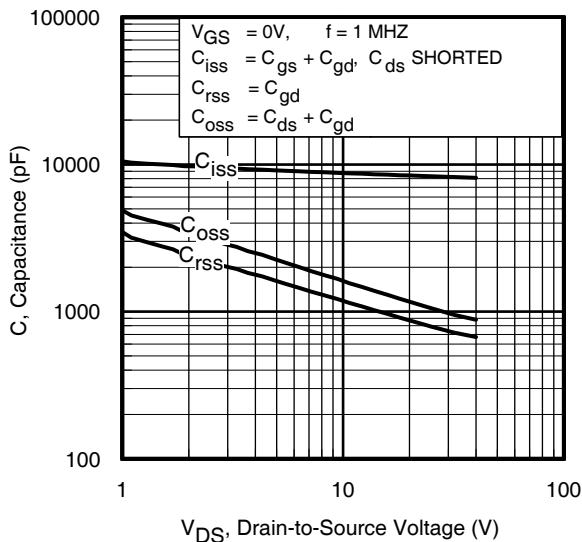
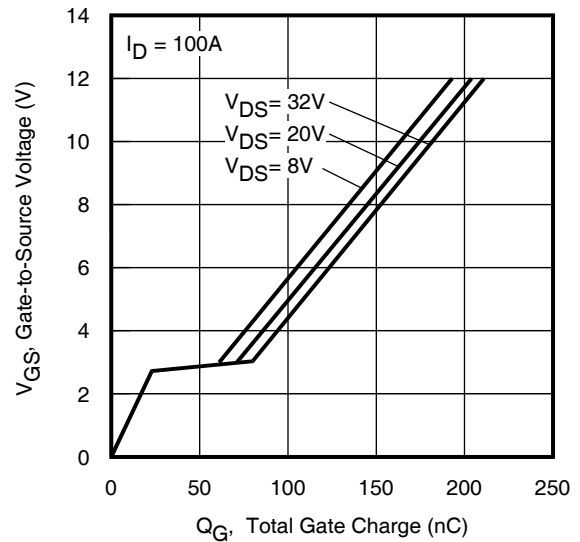
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
  - ② Repetitive rating; pulse width limited by max. junction temperature.
  - ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.07\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 100\text{A}$ ,  $V_{GS} = 10\text{V}$ .
  - ④  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 950\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
  - ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
  - ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
  - ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
  - ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
  - ⑨ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:  
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
  - ⑩ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 40\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- \* Pulse drain current is limited at 780A by source bonding technology.

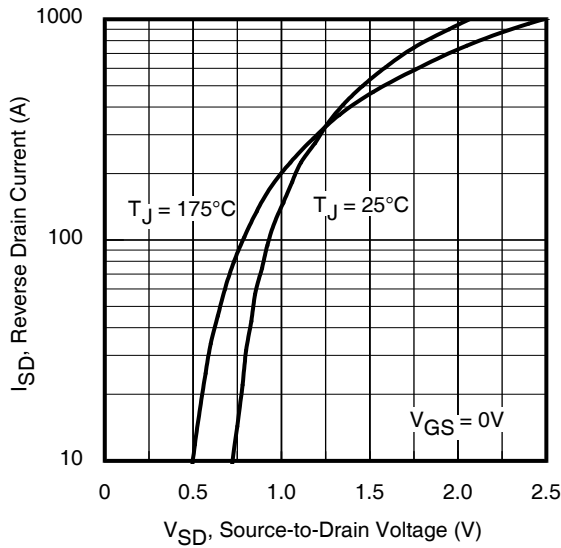
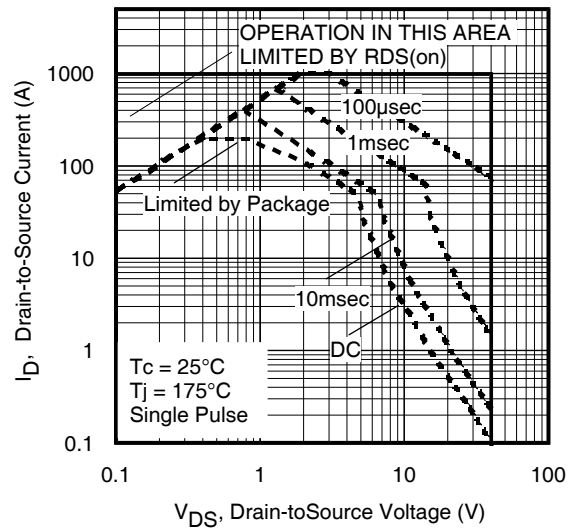
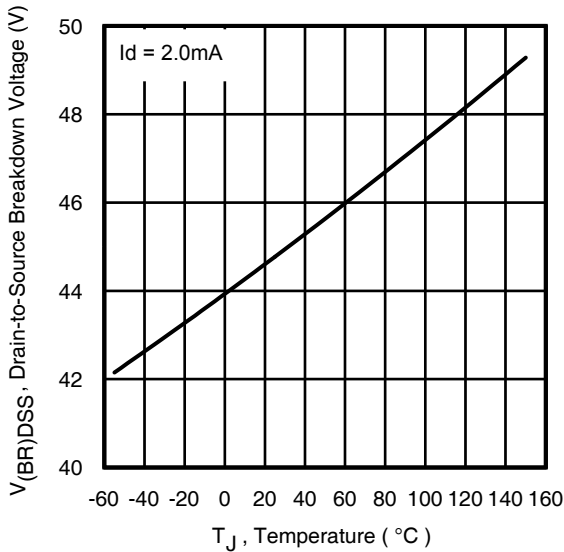
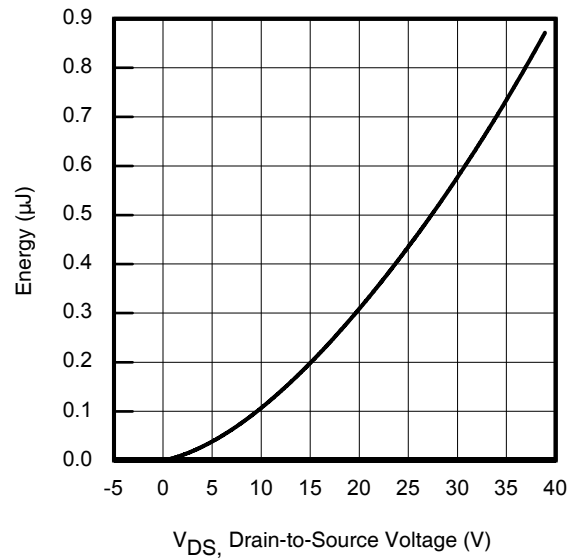
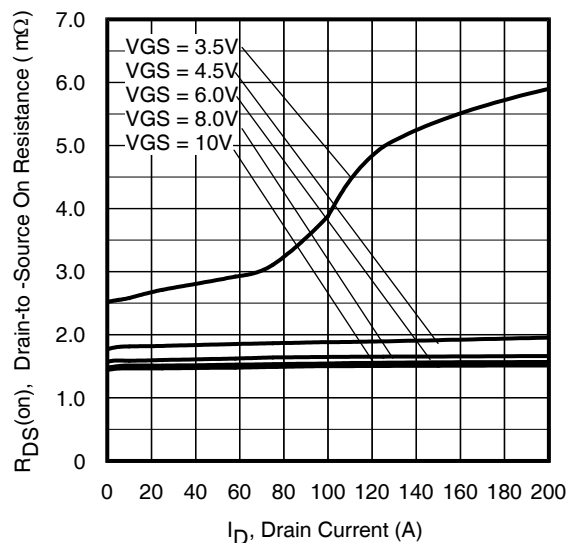
**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

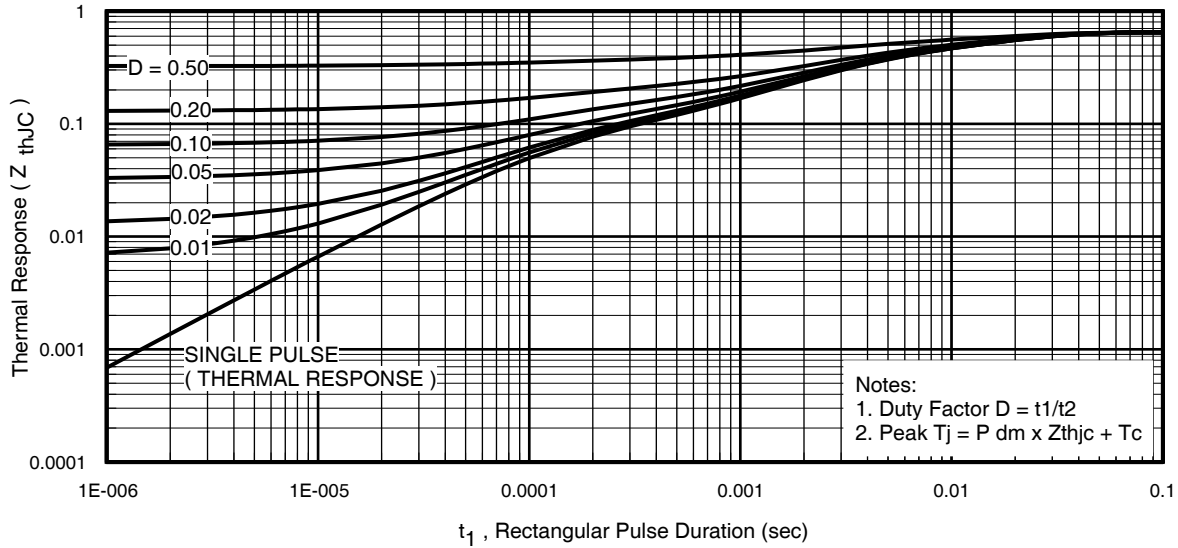
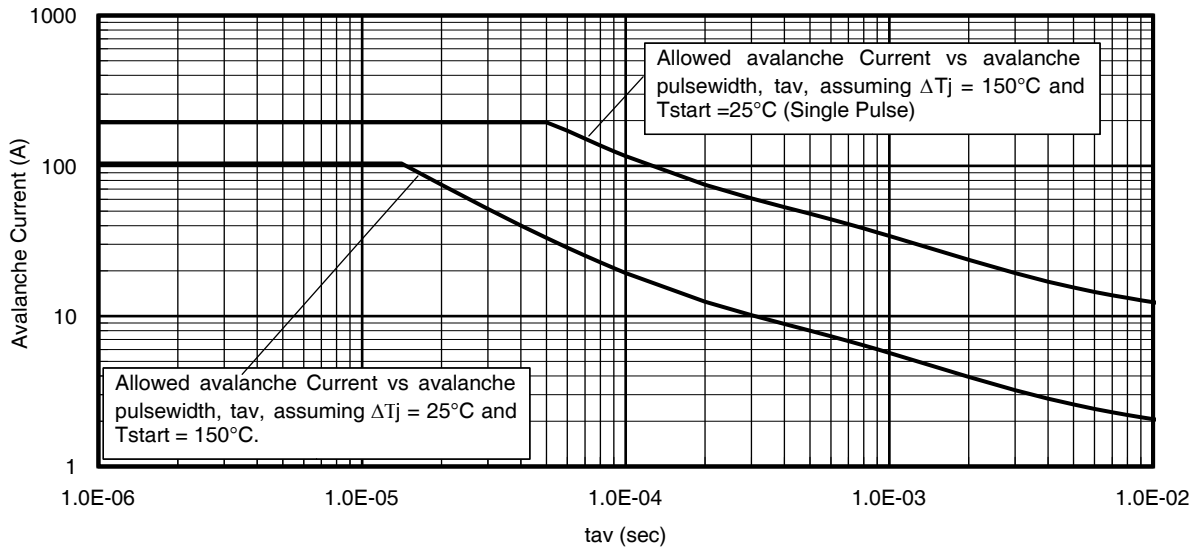
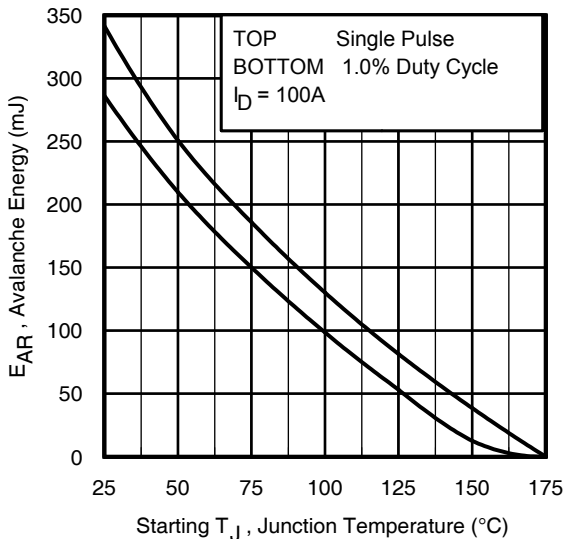
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	256	—	—	S	$V_{DS} = 10\text{V}, I_D = 100\text{A}$
$Q_g$	Total Gate Charge	—	91	137	nC	$I_D = 100\text{A}$ $V_{DS} = 20\text{V}$ $V_{GS} = 4.5\text{V}^{\text{⑤}}$
$Q_{gs}$	Gate-to-Source Charge	—	25	—		
$Q_{gd}$	Gate-to-Drain Charge	—	46	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	45	—		
$t_{d(on)}$	Turn-On Delay Time	—	39	—	ns	$V_{DD} = 20\text{V}$ $I_D = 30\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 4.5\text{V}^{\text{⑤}}$
$t_r$	Rise Time	—	154	—		
$t_{d(off)}$	Turn-Off Delay Time	—	88	—		
$t_f$	Fall Time	—	84	—		
$C_{iss}$	Input Capacitance	—	8320	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$ , See Fig.7
$C_{oss}$	Output Capacitance	—	1050	—		
$C_{rssi}$	Reverse Transfer Capacitance	—	790	—		
$C_{oss\text{ eff.}(ER)}$	Effective Output Capacitance (Energy Related)	—	1250	—		
$C_{oss\text{ eff.}(TR)}$	Output Capacitance (Time Related)	—	1580	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	254 <sup>①</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	990*		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 100\text{A}, V_{GS} = 0\text{V}^{\text{⑤}}$
$dv/dt$	Peak Diode Recovery $dv/dt$ <sup>④</sup>	—	6.0	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 100\text{A}, V_{DS} = 40\text{V}$
$t_{rr}$	Reverse Recovery Time	—	30	—	ns	$V_{DD} = 34\text{V}$ $I_F = 100\text{A}$ , $di/dt = 100\text{A}/\mu\text{s}^{\text{⑤}}$
		—	32	—		
$Q_{rr}$	Reverse Recovery Charge	—	26	—	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
		—	28	—		
$I_{RRM}$	Reverse Recovery Current	—	1.4	—	A	$T_J = 25^\circ\text{C}$

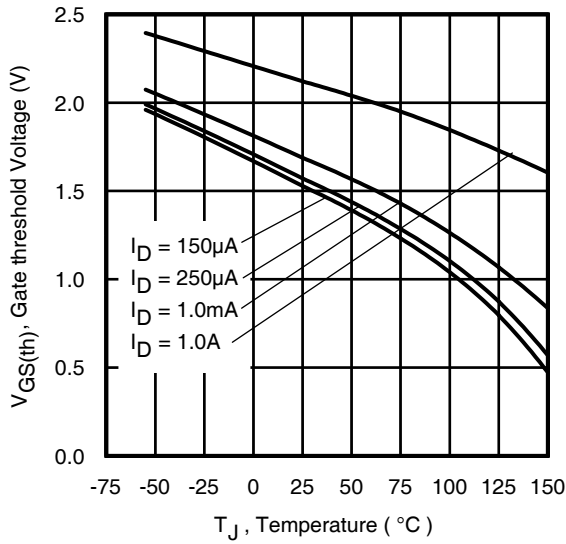
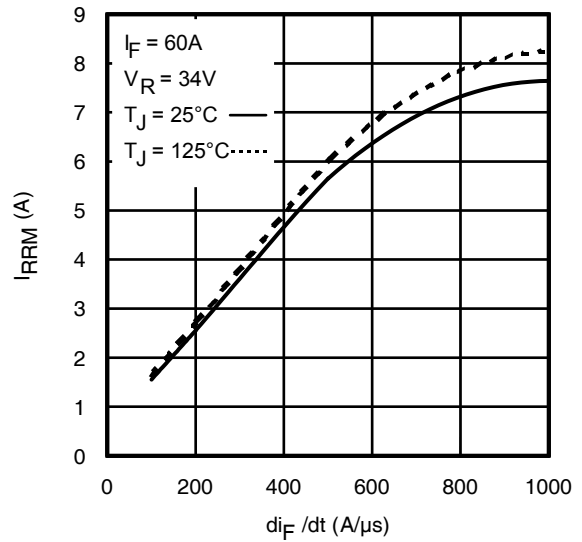
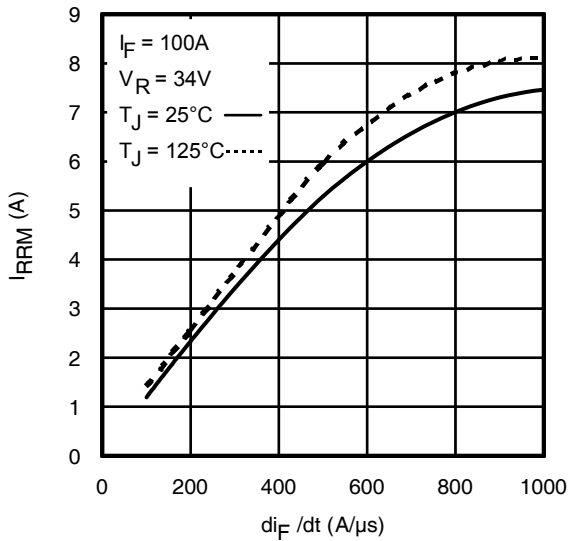
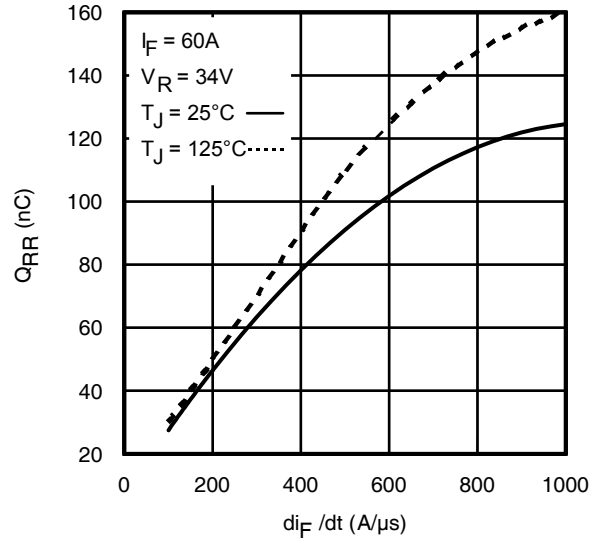
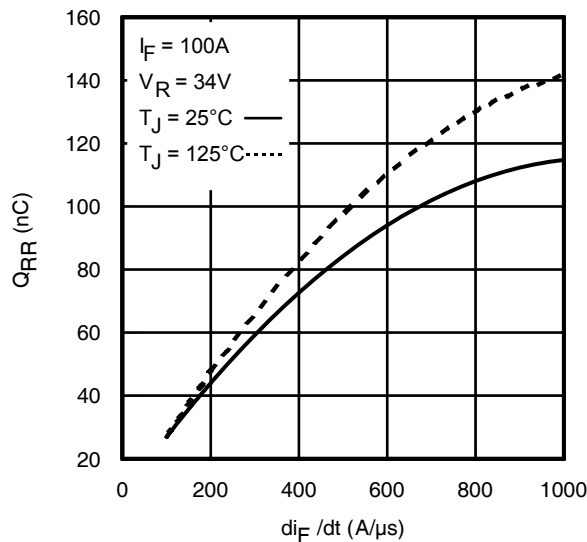

**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**

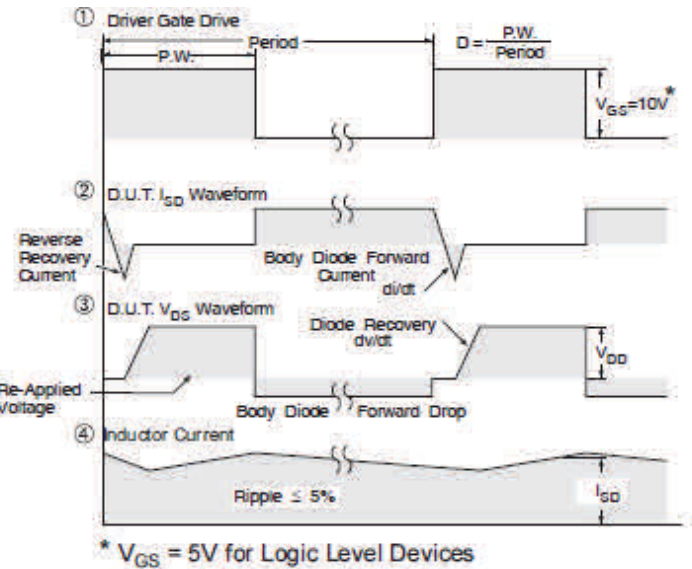
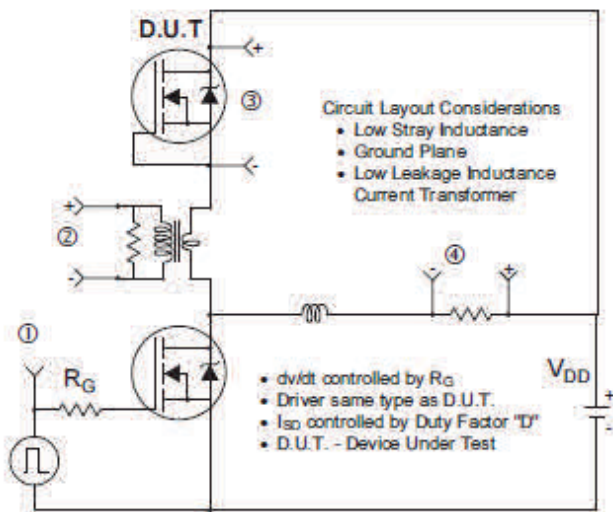
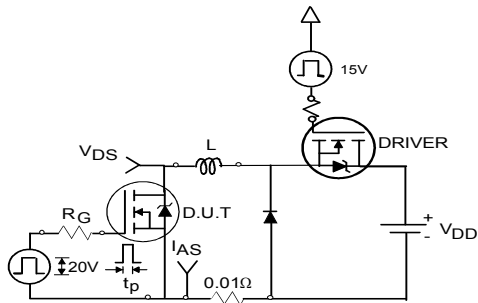
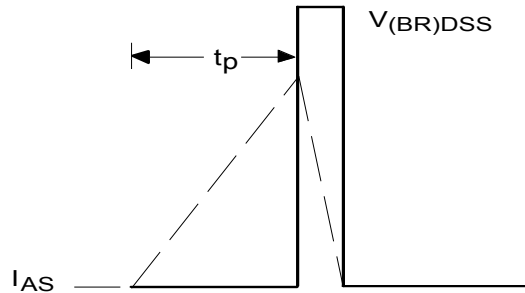
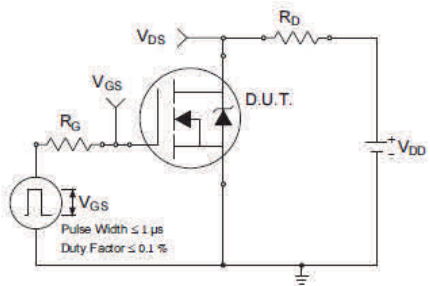
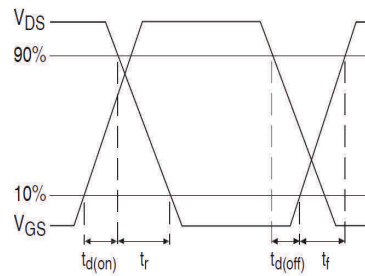
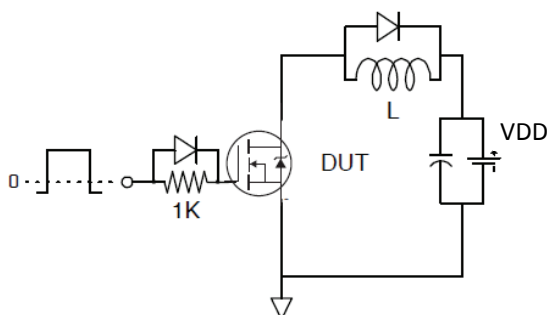
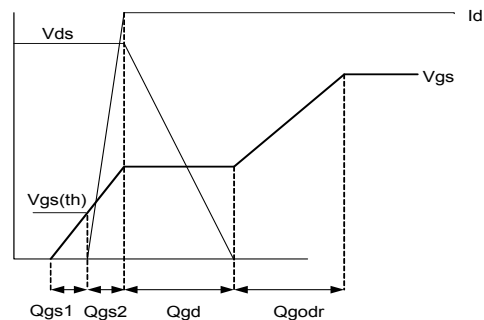

**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current


**Fig 14.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Fig 15.** Avalanche Current vs. Pulse Width

**Fig 16.** Maximum Avalanche Energy vs. Temperature

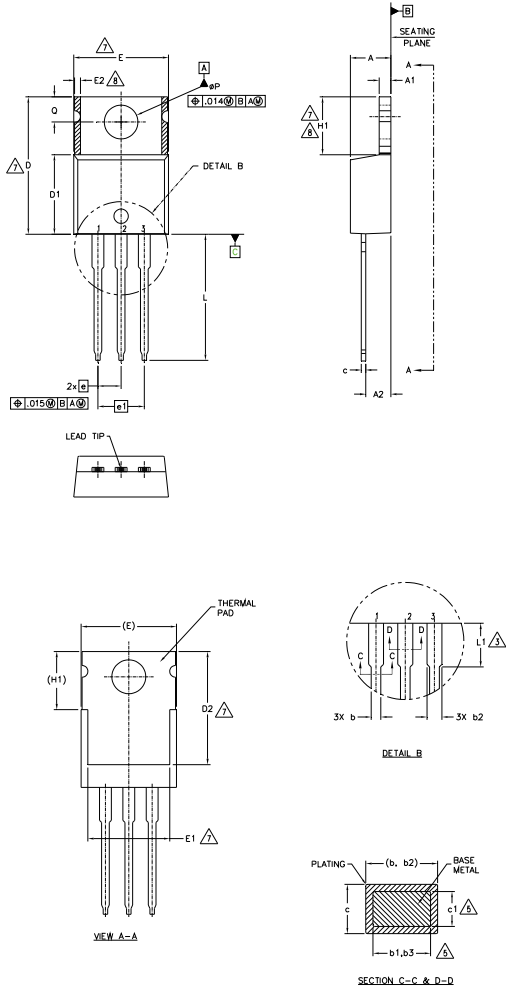
**Notes on Repetitive Avalanche Curves, Figures 15, 16:**  
 (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^\circ\text{C}$  in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figure 14)  
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


**Fig 17.** Threshold Voltage vs. Temperature

**Fig 18.** Typical Recovery Current vs.  $di/dt$ 

**Fig 19.** Typical Recovery Current vs.  $di/dt$ 

**Fig 20.** Typical Stored Charge vs.  $di/dt$ 

**Fig 21.** Typical Stored Charge vs.  $di/dt$


**Fig 22. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**

**Fig 23a. Unclamped Inductive Test Circuit**

**Fig 23b. Unclamped Inductive Waveforms**

**Fig 24a. Switching Time Test Circuit**

**Fig 24b. Switching Time Waveforms**

**Fig 25a. Gate Charge Test Circuit**

**Fig 25b. Gate Charge Waveform**



**TO-220AB Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

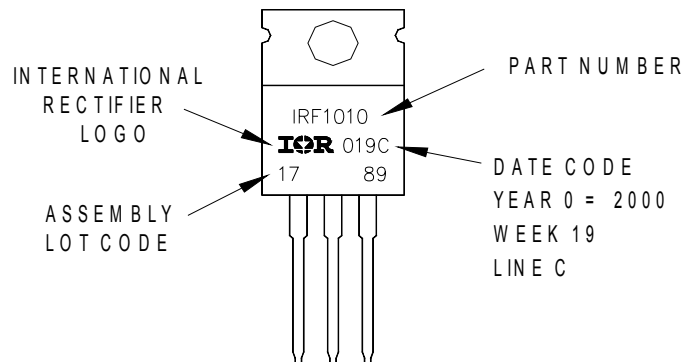
**DIODES**

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

**TO-220AB Part Marking Information**

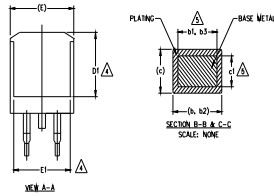
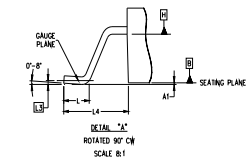
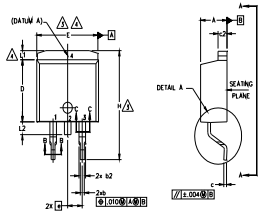
EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 2000  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))**


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [ .005" ] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  7. CONTROLLING DIMENSION: INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBO L	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	4
L2	1.27	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

**DIODES**

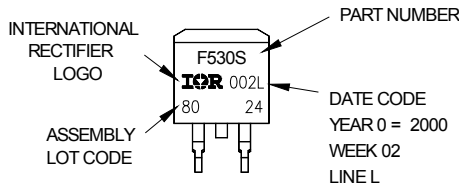
- 1.- ANODE \*
- 2, 4.- CATHODE
- 3.- ANODE

\* PART DEPENDENT.

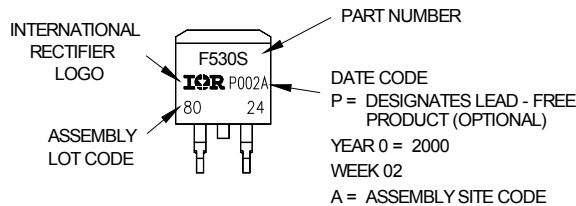
**D<sup>2</sup>Pak (TO-263AB) Part Marking Information**

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024 ASSEMBLED ON VW02, 2000 IN THE ASSEMBLY LINE "L"

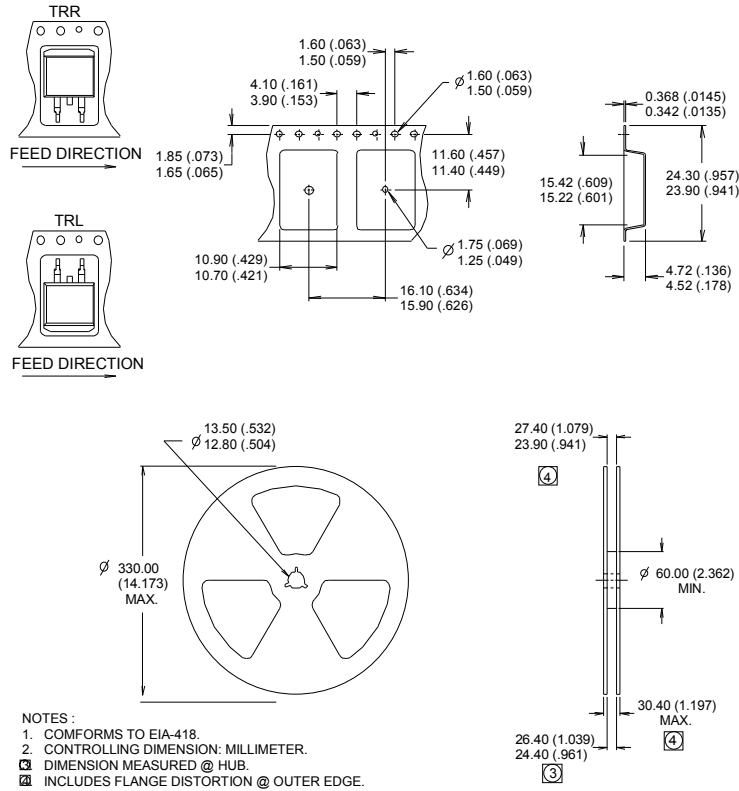
Note: "P" in assembly line position indicates "Lead - Free"



OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	TO-220	N/A
	D <sup>2</sup> Pak	MSL1
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

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